

GLOSSARY

Access time – The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example symbology:

Classified	Unclassified	Description
$t_{a(A)}$	t_{AVQV}	Access time from address
$t_{a(S)}$, $t_{a(CS)}$	t_{SLQV}	Access time from chip select (low)

Address – Any given memory location in which data can be stored or from which it can be retrieved.

Automatic chip select/power down – See chip-enable input.

Bit – Contraction of *binary digit* (i.e., a 1 or a 0). In electrical terms, the value of a bit can be represented by the presence or absence of charge, voltage, or current.

Byte – A word of eight bits (see word)

Capacitance —The property of a circuit element that permits it to store charge. Capacitance can vary with various inputs and outputs.

Example symbology:

C_i	Input capacitance
C_o	Output capacitance
$C_{i(D)}$	Input capacitance, data input

CAS – Column-address strobe. A clock used in dynamic random-access memories (DRAMs) to control the input of column addresses. It can be active high (CAS) or active low (\overline{CAS}).

CDIP – Ceramic dual in-line package

CERPAC – Ceramic flat pack (hermetic)

Chip-enable input – A control input to an integrated circuit that, when active, permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and, when inactive, causes the integrated circuit to be in a reduced-power standby mode.

Chip-select input – Chip-select inputs are gating inputs that control the input to, and output from, the memory. They may be of two kinds:

- Synchronous – Clocked/latched with the memory clock. Affects the inputs and outputs for the duration of that memory cycle.
- Asynchronous – Has direct asynchronous control of inputs and outputs. In the read mode, an asynchronous chip select functions like an output enable.

Classified time intervals – See time intervals.

CMOS – Complementary metal-oxide semiconductor. Technology that uses transistors with electron (N-channel) and hole (P-channel) conduction.

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Current

High-level input current, I_{IH}

The current into an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}

I_{OH} is defined by product specifications and is controlled by input conditions and output loading that establish a high-level current at the output. Current out of a terminal is given as a negative value.

Low-level input current, I_{IL}

The current into an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}

I_{OL} is defined by product specifications and is controlled by input conditions and output loading that establish a low-level current at the output. Current out of a terminal is given as a positive value.

Off-state (high-impedance state) output current (of a three-state output), I_{OZ}

The current into an output having 3-state capability with input conditions applied that, according to the product specification, establishes the high-impedance state at the output. Current out of a terminal is given as a negative value.

Short-circuit output current, I_{OS}

The current into an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential). Current out of a terminal is given as a negative value.

Supply current, I_{BB} , I_{CC} , I_{DD} , I_{PP}

The current into, respectively, the V_{BB} , V_{CC} , V_{DD} , and V_{PP} supply terminals.

Cycle time – The time interval between the start and end of a cycle. The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

Example symbology:

Classified	Unclassified	Description
$t_{c(R)}$, $t_{c(rd)}$	$t_{AVAV(R)}$	Read cycle time
$t_{c(W)}$	$t_{AVAV(W)}$	Write cycle time

R is usually used as the abbreviation for “read”; however, in the case of dynamic memories, “rd” is used to permit R to stand for \overline{RAS} .

Data – Any information stored or retrieved from a memory device

Die – Unpackaged semiconductor

DIMM – Dual In-line memory module

DIP – Dual in-line package



Disable time (of a 3-state output) – The time interval between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Example symbology:

Classified	Unclassified	Description
$t_{dis(S)}$	t_{SHQZ}	Output disable time after chip select (high)
$t_{dis(W)}$	t_{WLQZ}	Output disable time after write enable (low)

These symbols supersede the older forms t_{PVZ} or t_{PXZ} .

DRAM – Dynamic random-access memory. A memory in which the cells require the repetitive application of control signals to retain the stored data.

EDO – Extended-data out. Extended-data out allows for data output rates of up to 40 MHz for 60-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP} , the maximum RAS low time.

EEPROM – Electrically erasable programmable read-only memory. A memory chip that holds its data content without power and can be erased one address at a time, either within the system or externally.

Enable time (of a 3-state output) – The time interval between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). For memories, these intervals are often classified as access times.

Example symbology:

Classified	Unclassified	Description
$t_{en(SL)}$	t_{SLQV}	Output-enable time after chip select low

These symbols supersede the older form t_{PZV} .

EPROM – Erasable programmable read-only memory. A field-programmable read-only memory that can have the data content of each memory cell altered more than once. EPROMs are erased by exposure to ultraviolet (UV) light.

Erase – The procedure whereby data is removed from electronic media and the device returns to its unprogrammed state.

ESD – Electrostatic discharge.

Field-programmable read-only memory – See one-time programmable (OTP) read-only memory.

FIFO – First in, first out. A storage method that first retrieves the item that has been stored for the longest time.

Flash memory – A memory chip that holds its data content without power, but must be erased in fixed blocks rather than in single bytes.

FMEM – Field memory. A serial-access memory that performs high-speed, asynchronous read/write operations.

Fully static RAM – In a fully static RAM, the periphery as well as the memory array is fully static. The periphery is thus always active and ready to respond to input changes without the need of clocks. No precharge is required for static periphery.

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Hold time – The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. The hold time can have a negative value — in which case, the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is ensured.

Example symbology:

Classified	Unclassified	Description
$t_{h(D)}$	t_{WHDX}	Data hold time (after write high)
$t_{h(RHrd)}$	t_{RHWH}	Read (write enable high) hold time after \overline{RAS} high
$t_{h(CHrd)}$	t_{CHWH}	Read (write enable high) hold time after \overline{CAS} high
$t_{h(CLCA)}$	t_{CL-CAX}	Column address hold time after \overline{CAS} low
$t_{h(RLCA)}$	t_{RL-CAX}	Column address hold time after \overline{RAS} low
$t_{h(RA)}$	t_{RL-RAX}	Row address hold time (after \overline{RAS} low)

These last three symbols supersede the older forms:

New Form	Old Form
$t_{h(CLCA)}$	$t_{h(AC)}$
$t_{h(RLCA)}$	$t_{h(ARL)}$
$t_{h(RA)}$	$t_{h(AR)}$

The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

JEDEC – Solid State Products Engineering Council (formerly called the Joint Electronic Device Engineering Council) of the Electronic Industries Association (EIA). This council operates under EIA administrative and legal procedures and publishes JEDEC standards and publications. This council also continuously develops and maintains these standards as required by the industry.

JTAG – Joint Test Action Group that wrote the IEEE Standard 1149.1. With acceptance of the standard, the group was dissolved and no longer exists.

K – When used in the context of specifying a given number of bits of information, $1K = 2^{10} = 1024$ bits. Therefore, $64K = 64 \times 1024 = 65\,536$ bits.

Latency – Number of clock cycles until a command takes effect. The state of the device changes after the latency period.

Mask-programmed read-only memory – A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask. Thereafter, the data content cannot be altered.

Memory – A medium capable of storing information that can be retrieved.

Memory cell – The smallest subdivision of a memory into which a unit of data can be entered, stored, and retrieved.

Metal-oxide semiconductor (MOS) – The technology involving photolithographic layering of metal and oxide to produce a semiconductor device.

Micro BGA – Small Ball-Grid Array package.

MIL-M-38510 – A military controlling specification pertaining mainly to Joint Army/Navy (JAN)-qualified devices (microcircuits).



MIL-PRF-38535 (QML) – The QML (Qualified Manufacturers List) program was initiated to ease the process of qualifying devices for military use. QML encourages process control to “build in” reliability as opposed to end-of-line screening and inspection. QML also encourages Best Commercial Practices by allowing elimination of process steps that statistically add no reliability to military integrated circuits (ICs).

MRS – Mode register set. The command process by which the programmable features of the memory device are defined. Such features include serial or interleave burst type, defining system read latency, and defining burst length.

NMOS – A type of MOS technology in which the basic conduction mechanism is governed by electrons. (Short for N-channel MOS.)

Nonvolatile memory – A memory in which the data content is maintained whether the power supply is connected or not.

OTP – One-time programmable. A read-only memory that, after being manufactured, can have the data content of each memory cell altered once.

Output enable – A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select.)

Parallel access – A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

PDIP – Plastic dual in-line package

PLCC – Plastic leaded chip carrier

PMOS – A type of MOS technology in which the basic conduction mechanism is governed by holes. (Short for P-channel MOS.)

Power down – A mode of a memory during which the device is operating in a low-power or standby mode. Normally, read or write operations of the memory are not possible under this condition.

Printed wiring board (PWB) – A substrate of epoxy glass, clad material, or other material upon which a pattern of conductive traces is formed to interconnect the components that are mounted upon it.

Program – Typically associated with nonvolatile memories, the procedure whereby logical 0s are stored into various desired locations in a previously erased device.

Program enable – An input signal that, when true, puts a programmable memory device into the program mode.

PROM – Programmable read-only memory. A memory chip that can have the data content of each memory cell altered only once, and cannot be erased.

PSOP – Plastic small-outline package

Pulse duration (width) – The time interval between the specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

Classified	Unclassified	Description
$t_w(W)$	t_{WLWH}	Write pulse duration
$t_w(RL)$	t_{RLRH}	Pulse duration, \overline{RAS} low

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RAM – Random-access memory. A memory chip that permits access to any of its address locations in any desired sequence with similar access time to each location. RAM usually denotes read/write memory.

RAS – Row-address strobe. A clock used in DRAMs to control the input of the row addresses. It can be active high (RAS) or active low ($\overline{\text{RAS}}$).

Read – A memory operation whereby data is output from a desired address location.

Read/write memory – A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electrical input signals.

Refresh – DRAM or SDRAM operation by which data is retained in the memory.

Refresh time interval – The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates.

Example symbology:

Classified	Unclassified	Description
t_{rf}		Refresh time interval

ROM – Read-only memory. A memory chip that permanently stores instructions and data. Its contents are created at the time of manufacture and cannot be altered. ROM chips are used to store control routines in personal computers, peripheral controllers, and other electronic equipment.

Scaled MOS (SMOS) – MOS technology under which the device is scaled down in size in three dimensions and in operating voltages allowing for improved performance.

SDRAM – Synchronous dynamic random-access memory. SDRAM synchronizes all address, data, and control signals with the system clock. This makes the data transfer rates much higher than can be attained with asynchronous data. System design will be made easier with timing relationships now similar to other system operations.

Semi-static (quasi-static, pseudo-static) RAM – In a semi-static RAM, the periphery is clock-activated (i.e., dynamic). Thus, the periphery is inactive until clocked, and only one memory cycle is permitted per clock. The peripheral circuitry must be allowed to reset after each active memory cycle for a minimum precharge time. No refresh is required.

Serial access – A feature of a memory by which all the bits are entered sequentially at a single input or retrieved sequentially from a single output.

Setup time – The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. The setup time can have a negative value — in which case, the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is ensured.

Example symbology:

Classified	Unclassified	Description
$t_{\text{su}}(\text{D})$	t_{DVWH}	Data setup time (before write high)
$t_{\text{su}}(\text{CA})$	$t_{\text{CAV-CL}}$	Column address setup time (before $\overline{\text{CAS}}$ low)
$t_{\text{su}}(\text{RA})$	$t_{\text{RAV-RL}}$	Row address setup time (before $\overline{\text{RAS}}$ low)



SIMM – Single in-line memory module

SMD – Standard Military Drawing

SODIMM – Small-outline dual in-line memory module

SOIC – Small outline integrated circuit. A package in which an integrated circuit chip can be mounted to form a surface-mounted component. It is made of a plastic material that can withstand high temperatures and has leads formed in a gull-wing shape along its two longer sides for connection to a PWB footprint.

SOJ – Small-outline J-lead package

SOLCC – Small-outline leadless ceramic chip carrier

SOP – Small-outline package

SQFP – Small quad flatpack

SRAM – Static RAM. A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of periphery circuitry sub-categorizes static RAMs.

Temperature ranges – The temperature range over which the device operates and the range which meets the specified electrical characteristics. Ranges may be expressed as ambient, operating free-air, or case temperature.

Ambient temperature (T_A)

The temperature in the surrounding area.

Operating free-air temperature (T_A)

The temperature near the device, which may include movement of the air by a fan or other causes.

Case temperature (T_C)

The temperature of the case enclosing the device.

Time intervals – New or revised data sheets use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms are used. The first (classified) form is usually used when intervals can be easily classified as access, cycle, disable, enable, hold, refresh, setup, transition, or valid times and for pulse durations. The second (unclassified) form can be used generally for time intervals that are not easily classifiable. The second form is described first in the following paragraphs since some manufacturers use this form for all time intervals. Symbols in the unclassified form are given with the examples when applicable.

Unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definitions. Symbols for unclassified time intervals identify two signal events listed in from-to sequence using the format:

t_{AB-CD}

Subscripts A and C indicate the names of the signals for which changes of state or level, or establishment of state or level, constitute signal events assumed to occur first and last, respectively (that is, at the beginning and end of the time interval). Every effort is made to keep the A and C subscript length down to one letter, if possible (e.g., R for \overline{RAS} and C for \overline{CAS}).

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Time intervals (continued)

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

- H = high or transition to high
- L = low or transition to low
- V = a valid steady-state level
- X = unknown, changing, or “don’t care” level
- Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

Classified time intervals

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be significantly shortened compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained. See access, cycle, disable, enable, hold, refresh, setup, transition, and valid times for specific definitions. See also pulse duration.

Timing diagram conventions – Figure 1 shows the timing diagram symbols and definitions.




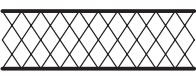

Timing Diagram Symbol	Meaning	
	Input Forcing Functions	Output Response Functions
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated intervals
	Low-to-high changes permitted	Will be changing from low to high sometime during designated intervals
	Don't care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state.

Figure 1. Timing Diagram Symbols

Transition times (also called rise and fall times) – The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classified	Unclassified	Description
t_t		Transition time (general)
$t_{t(CH)}$	t_{CHCH}	Low-to-high transition time of \overline{CAS}
$t_{r(C)}$	t_{CHCH}	\overline{CAS} rise time
$t_{f(C)}$	t_{CLCL}	\overline{CAS} fall time

TSOJ – Thin small-outline J-lead package

TSOP – Thin small-outline package

Unclassified time intervals – See time intervals.

Valid time – Valid time is defined as follows.

- General: The time interval during which a signal is (or should be) valid.
- Output data-valid time: The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Unclassified	Description
$t_v(A)$	t_{AXQX}	Output data valid time after change of address

This supersedes the older form t_{PVX} .

VLSI – Very-large-scale integration. The description of an IC technology that is much more complex than large-scale integration (LSI) and involves a much higher equivalent gate count. At this time, an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

Volatile memory – A memory in which the data content is lost when the power supply is disconnected.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum is specified that is the least positive value of high-level input voltage for which the logic element within specification limits is ensured.

High-level output voltage, V_{OH}

V_{OH} is defined by product specifications and controlled by input conditions and output loading that establish a high-level voltage condition at the output.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values is used to represent the binary variables.

The most positive value of low-level input voltage is specified for which operation of the logic element within specification limits is ensured.

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Voltage (continued)

Low-level output voltage, V_{OL}

V_{OL} is defined by product specifications and controlled by input conditions and output loading that establish a low-level voltage condition at the output.

Supply voltages, V_{BB} , V_{CC} , V_{DD} , V_{PP}

The voltages supplied to the corresponding voltage pins that are required for the device to function. From one to four of these supplies may be necessary, along with ground (V_{SS}).

Word – A series of one or more bits that occupy a given address location and then can be stored and retrieved in parallel.

Write – A memory operation whereby data is written into a desired address location.

Write enable – A control signal that, when true, causes the memory to assume the write mode, and, when false, causes it to assume the read mode.

ZIP – Zig-zag in-line package.

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