



Literature Number: SNAP004

PLL Fundamentals

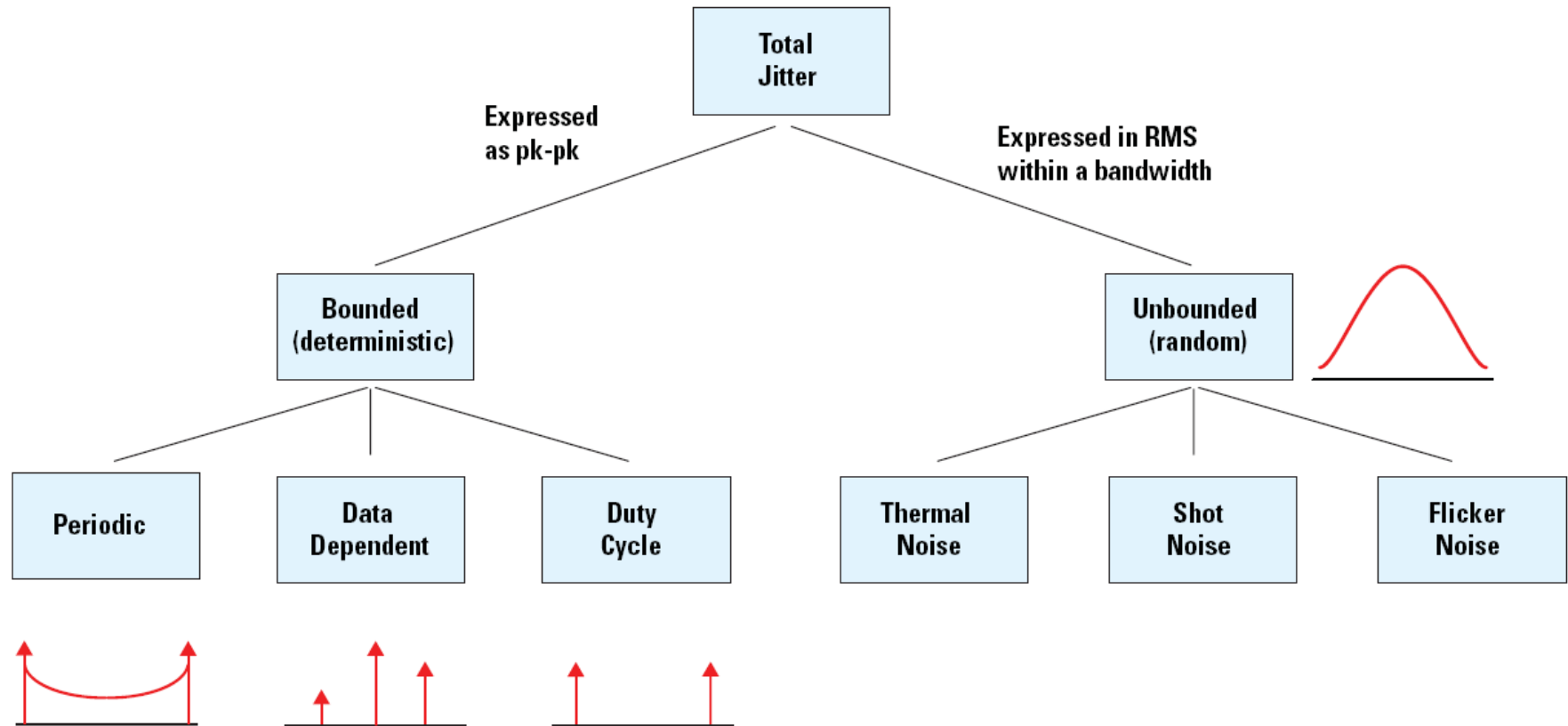
Part 4: PLL Clocking Applications

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Overview

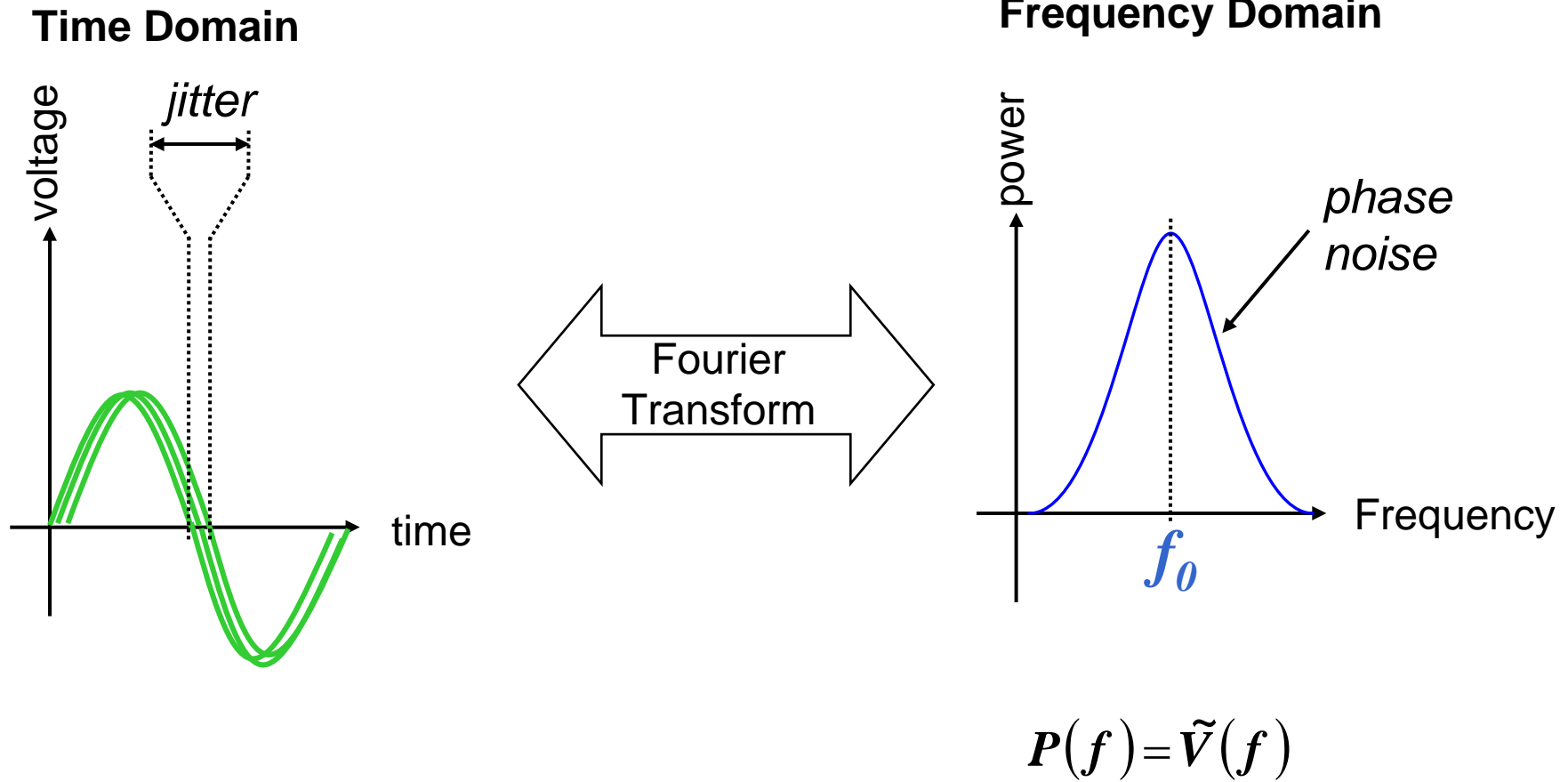
- Understanding Jitter
- Clock Cleaning Applications
- A/D Clocking Applications

The Jitter Family Tree



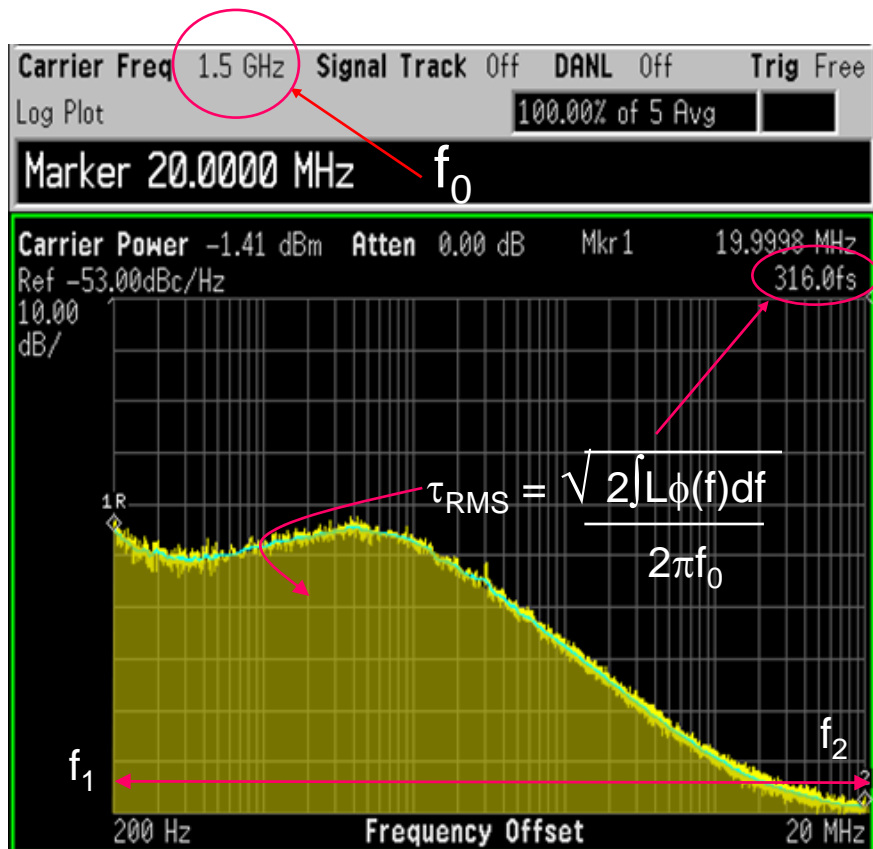


Gaussian Phase Noise Jitter

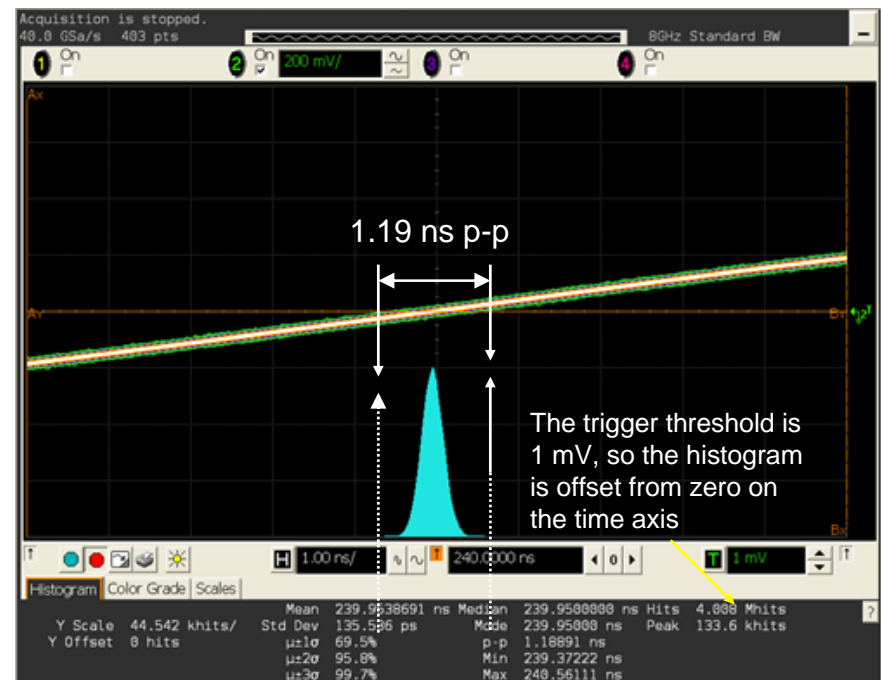


Measuring Phase Noise and Jitter

Frequency Domain Jitter Measurement

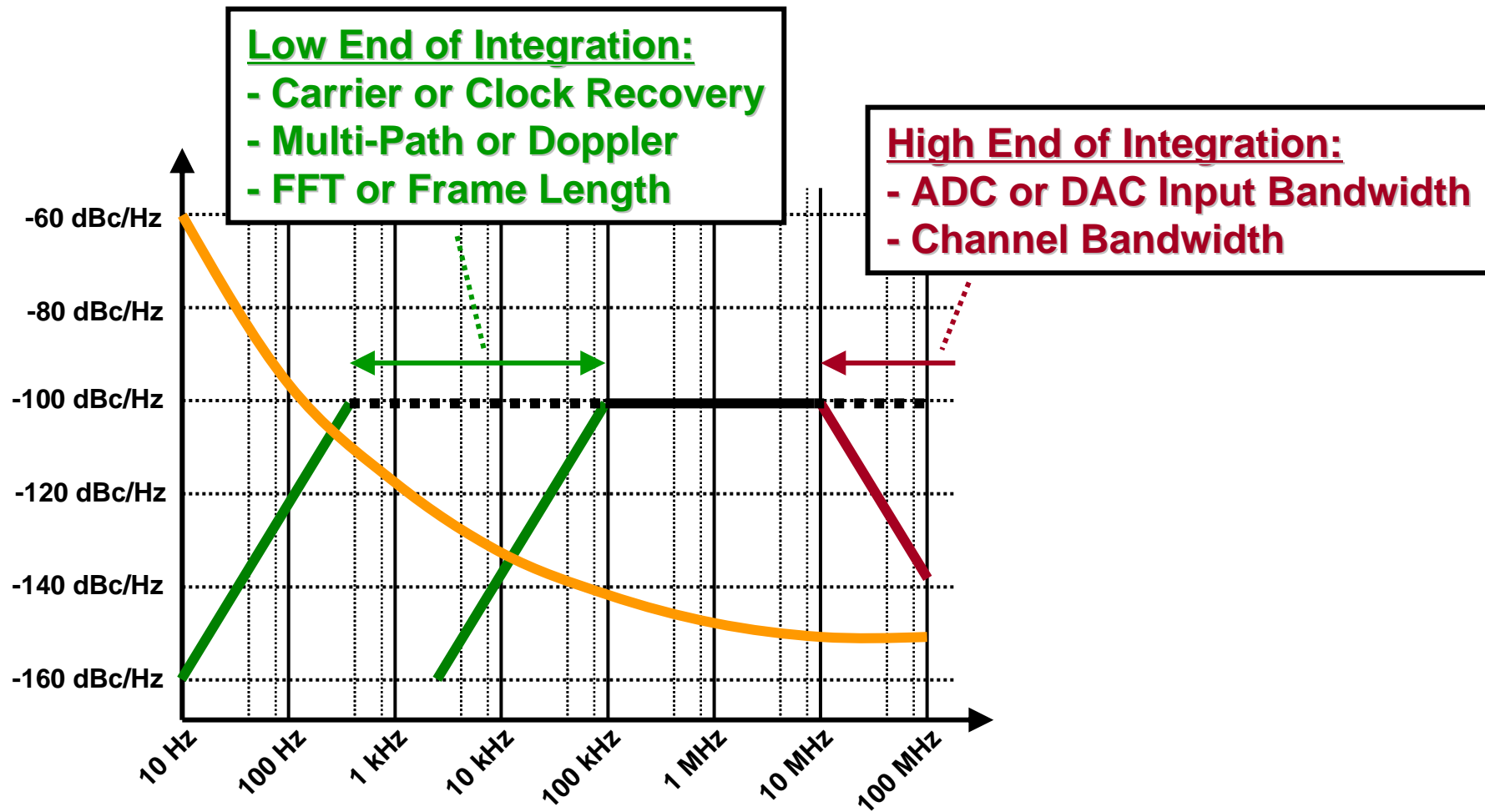


Time Domain Jitter Measurement



Even 40 GS oscilloscope is not recommended for measuring 316 fs of random jitter!

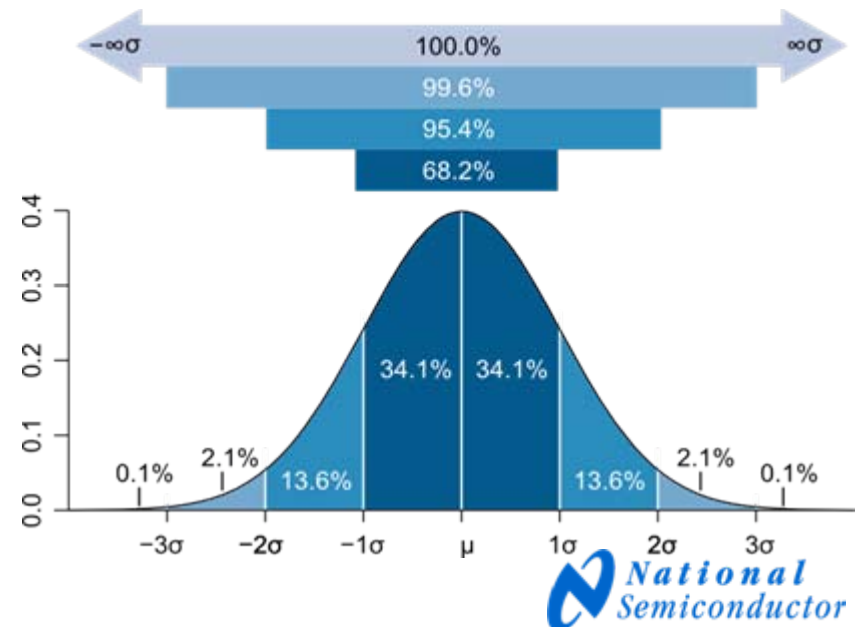
Jitter Integration Bandwidth



Converting from peak to peak jitter to RMS jitter or vice-versa

- **Multiplier is how many standard deviations are included on a standard distribution**
- **$(400 \text{ fs RMS}) \cdot (14.059) = 5.6 \text{ ps p-p jitter}$**
 - with 1 bit error in every 10^{12} bits.
- **$(10 \text{ ps p-p jitter}) / (15.883) = 630 \text{ fs RMS jitter}$**
 - with 1 bit error in every 10^{15} bits.

BER	Multiplier
$1:10^4$	7.438
$1:10^6$	9.507
$1:10^9$	11.996
$1:10^{11}$	13.412
$1:10^{12}$	14.069
$1:10^{15}$	15.883



Overview

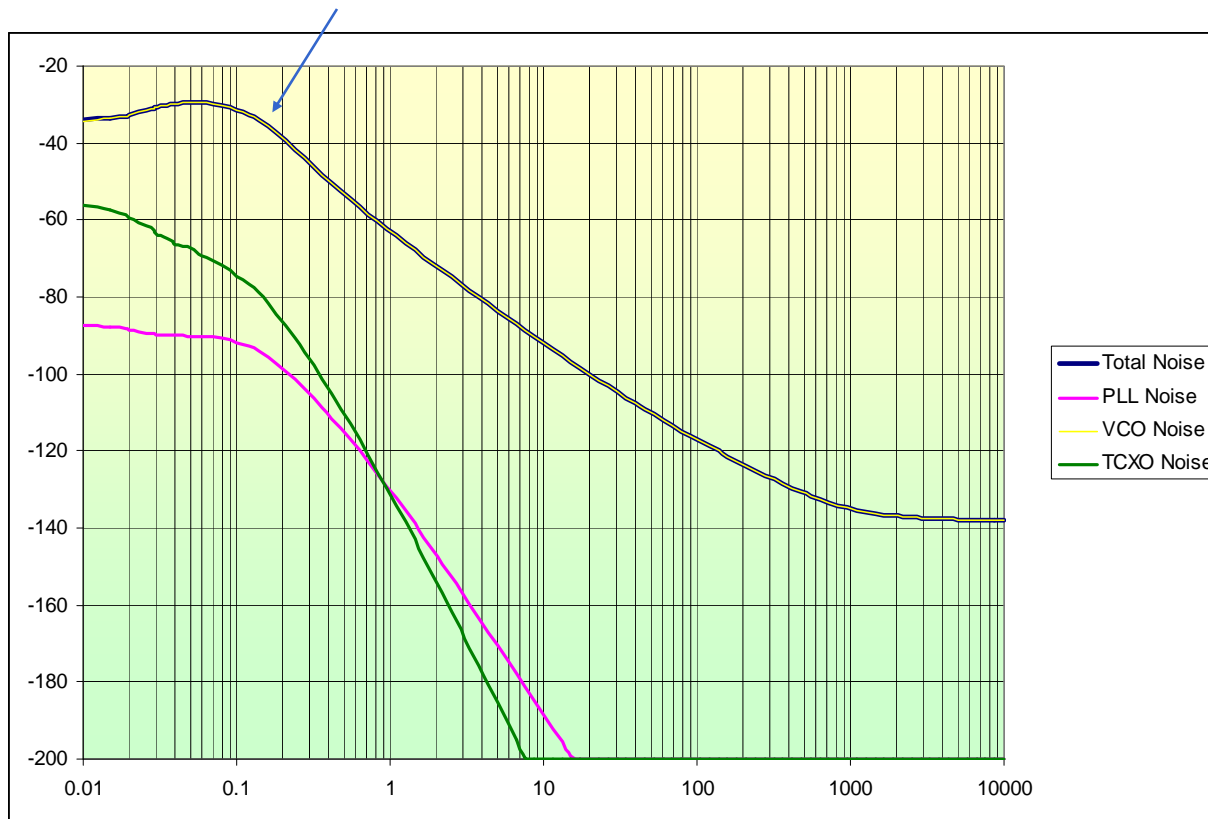
- Understanding Jitter
- **Clock Cleaning Applications**
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Clock Cleaners

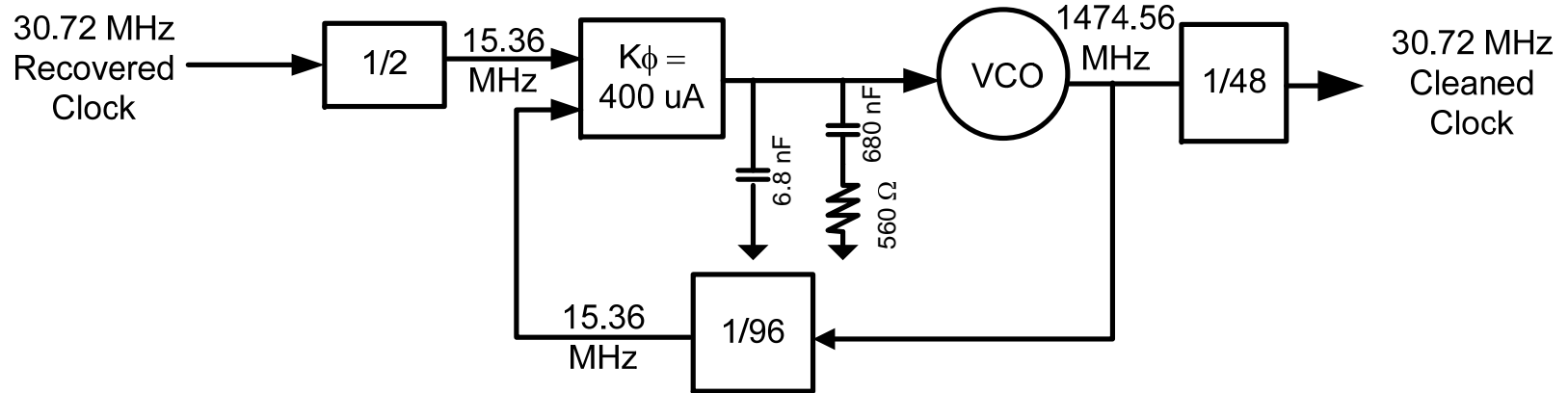
- Takes a dirty clock and a PLL with a narrow loop bandwidth to clean this up
- A PLL with a narrow loop bandwidth can be thought of as a tunable filter with a very narrow passband
 - How else could you filter noise at 10 kHz offset from a 400 MHz carrier?
- VCO noise is important for this kind of application

Narrow loop band width example

Total noise closely follows the VCO profile



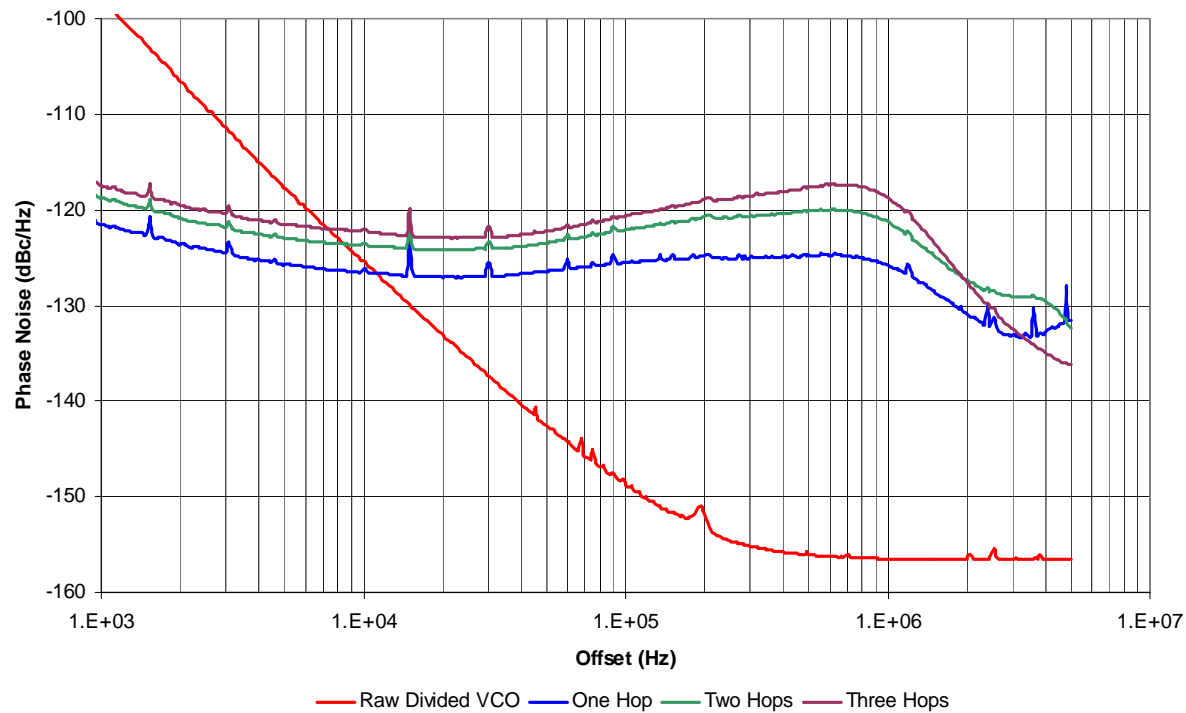
SCAN25100 + LMK03000 Setup



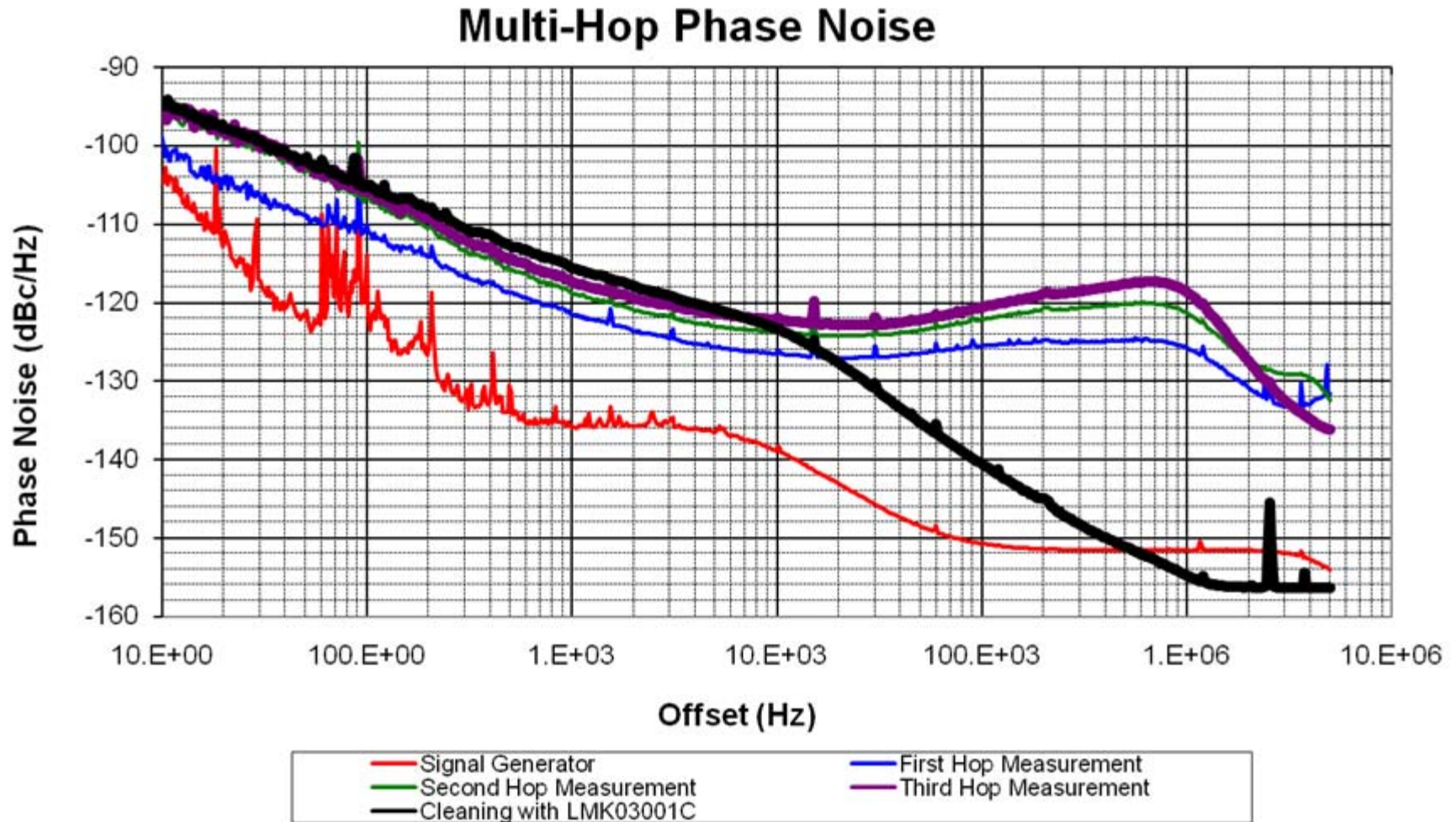
This example is taken from application note 1734



Clock Cleaning Example with LMK03000



SERDES – Recovered Clock Cleaning

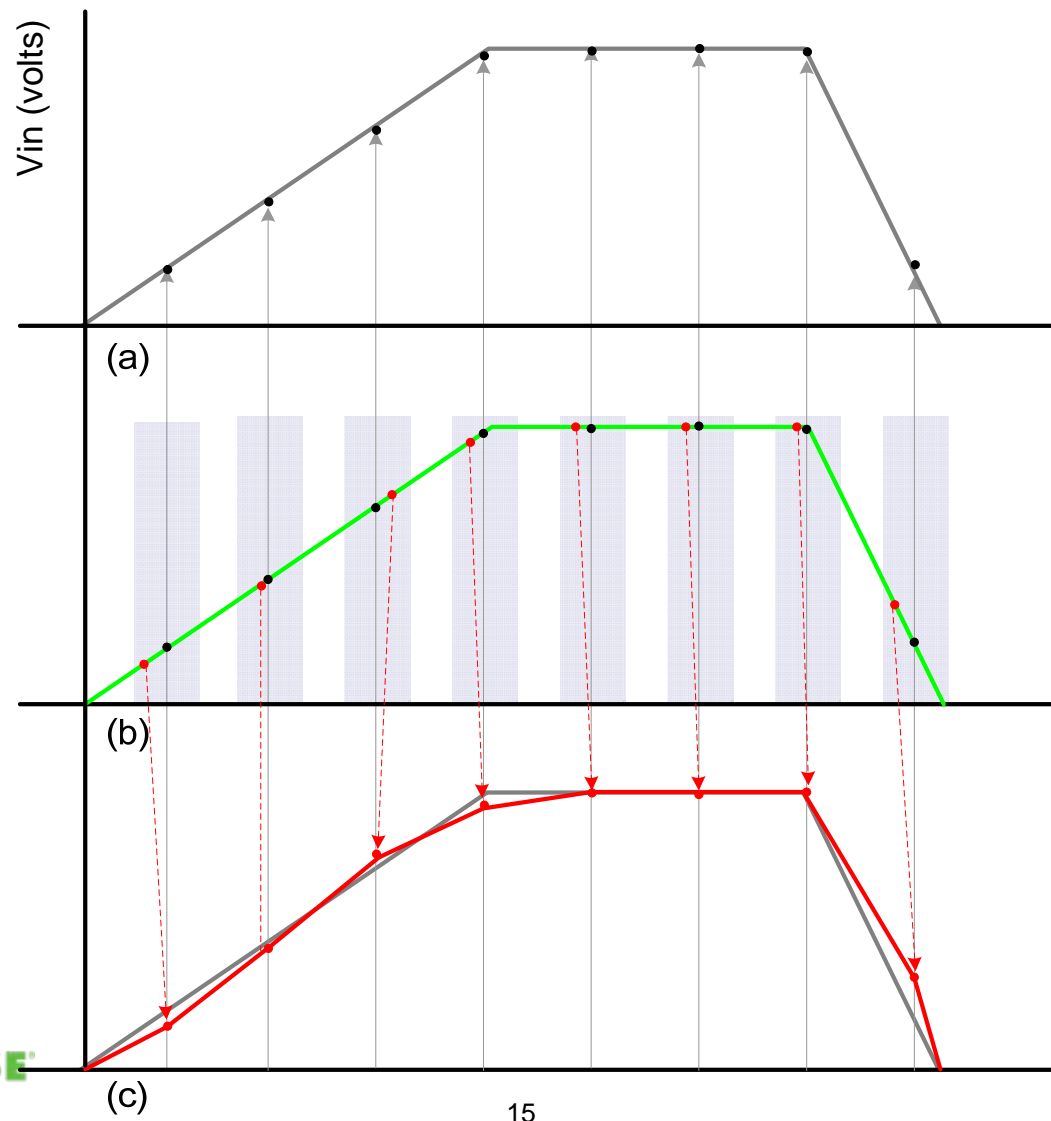


Overview

- Understanding Jitter
- Clock Cleaning Applications
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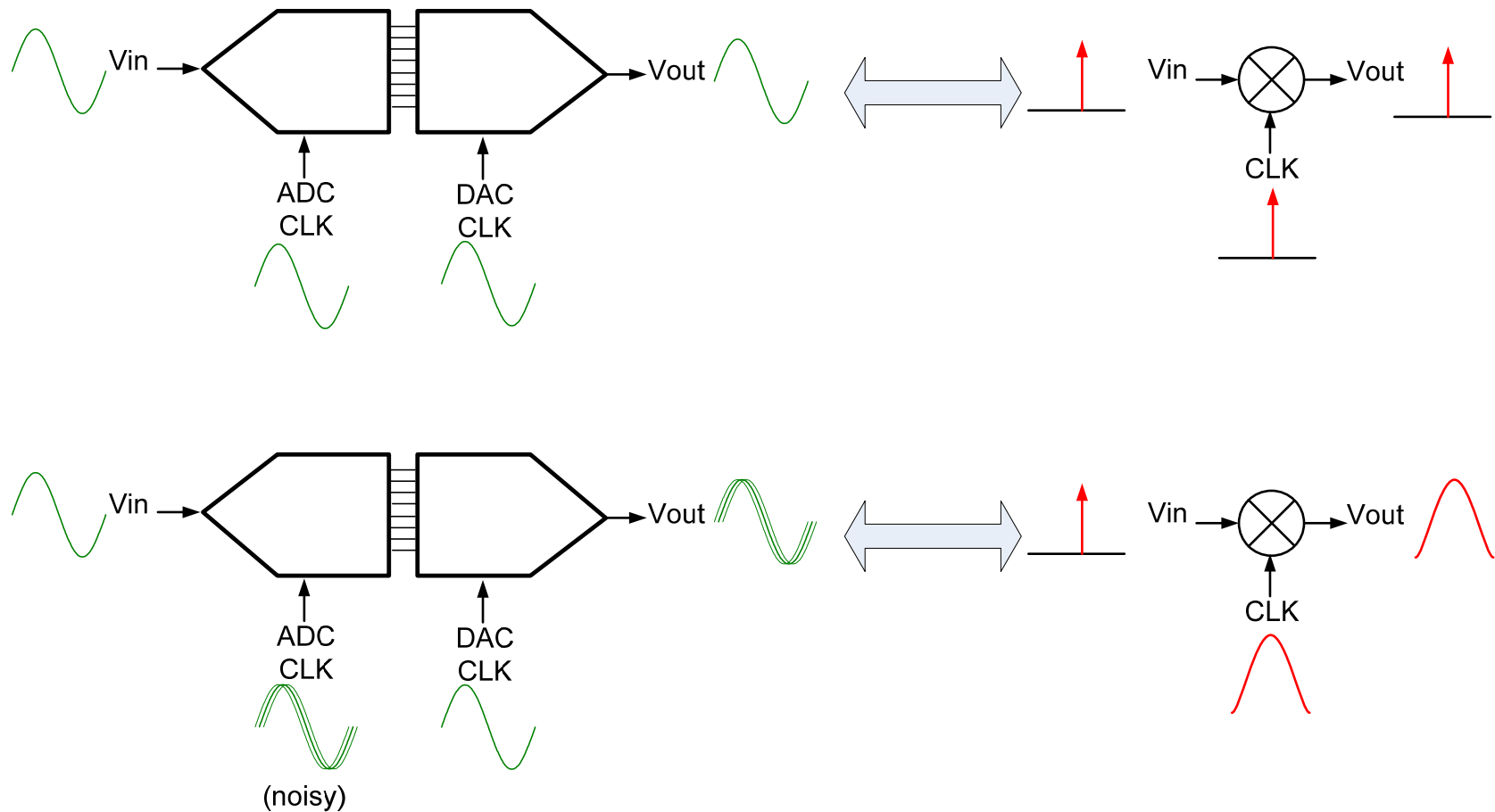


Distortion in a sampled waveform

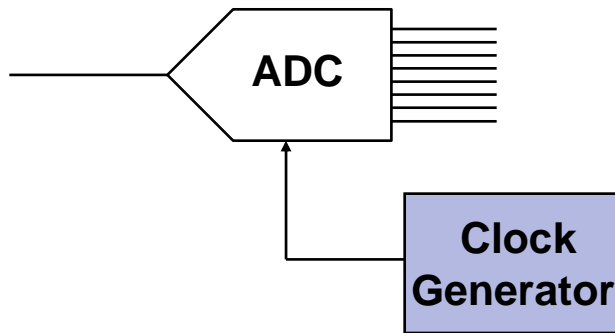




Sampling is analogous to mixing



Sampling jitter



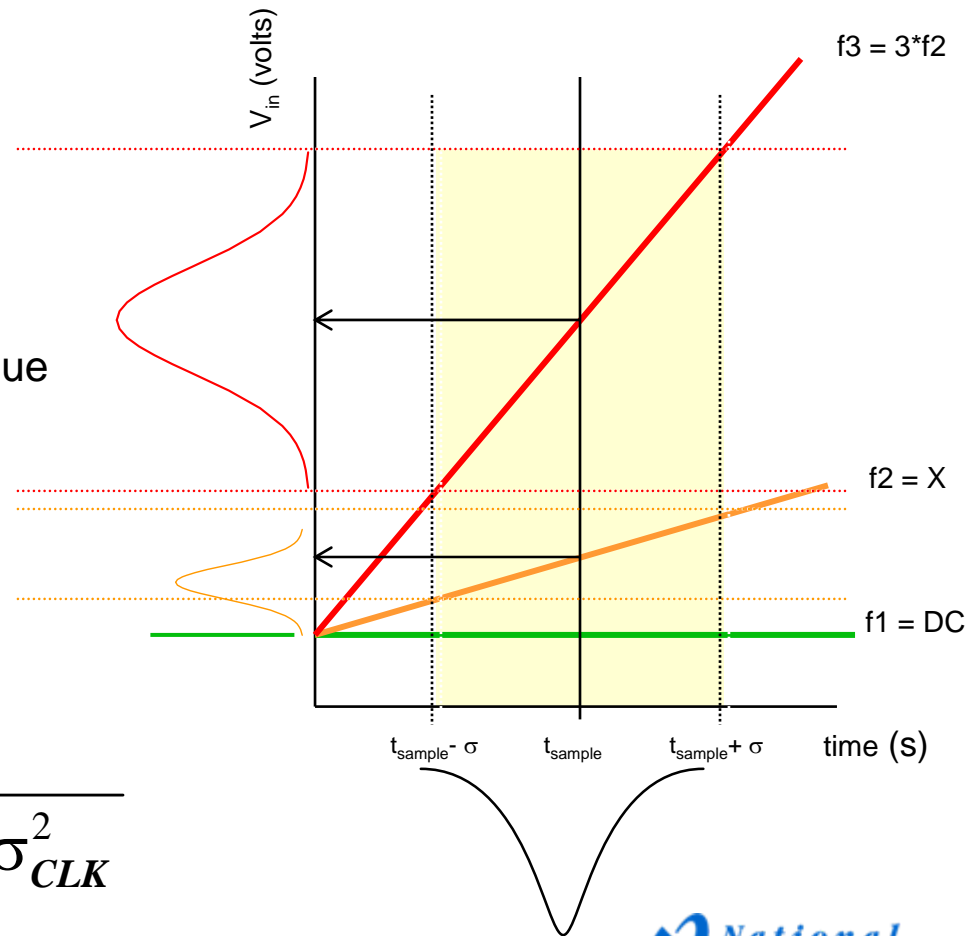
Distribution of the sampled voltage value due to sampling jitter.

Sampling jitter has two components:

1. Jitter on the sampling clock
2. Aperture jitter from the ADC.

Because they are uncorrelated, these jitters are combined as the root sum square:

$$\sigma = \sqrt{\sigma_{ADC}^2 + \sigma_{CLK}^2}$$





SNR as a function of Sample clock jitter

Assuming a sinusoidal input for V_{in} we have,

$$v(t) = V_o \sin 2\pi f t$$

Differentiating with respect to time yields the signal slope,

$$\frac{dv}{dt} = 2\pi f V_o \cos 2\pi f t$$

Taking the RMS value,

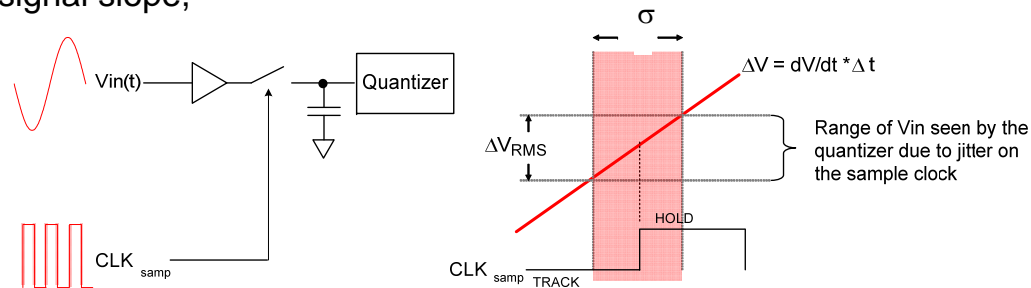
$$\frac{dv}{dt}_{rms} = \frac{2\pi f V_o}{\sqrt{2}} = \frac{\Delta V_{RMS}}{\sigma}$$

Therefore, the RMS error voltage due to jitter is

$$\Delta V_{RMS} = \frac{2\pi f V_o \sigma}{\sqrt{2}}$$

Signal to noise ratio (SNR) is defined by,

$$SNR = 20 \log_{10} \left[\frac{\text{signal}}{\text{noise}} \right] = 20 \log_{10} \left[\frac{V_o / \sqrt{2}}{\Delta V_{rms}} \right]$$



Therefore, the SNR component due to jitter is:

$$SNR_{jitter} = 20 \log_{10} \left[\frac{1}{2\pi f_{max} \sigma} \right]$$

Why do we care about SNR?

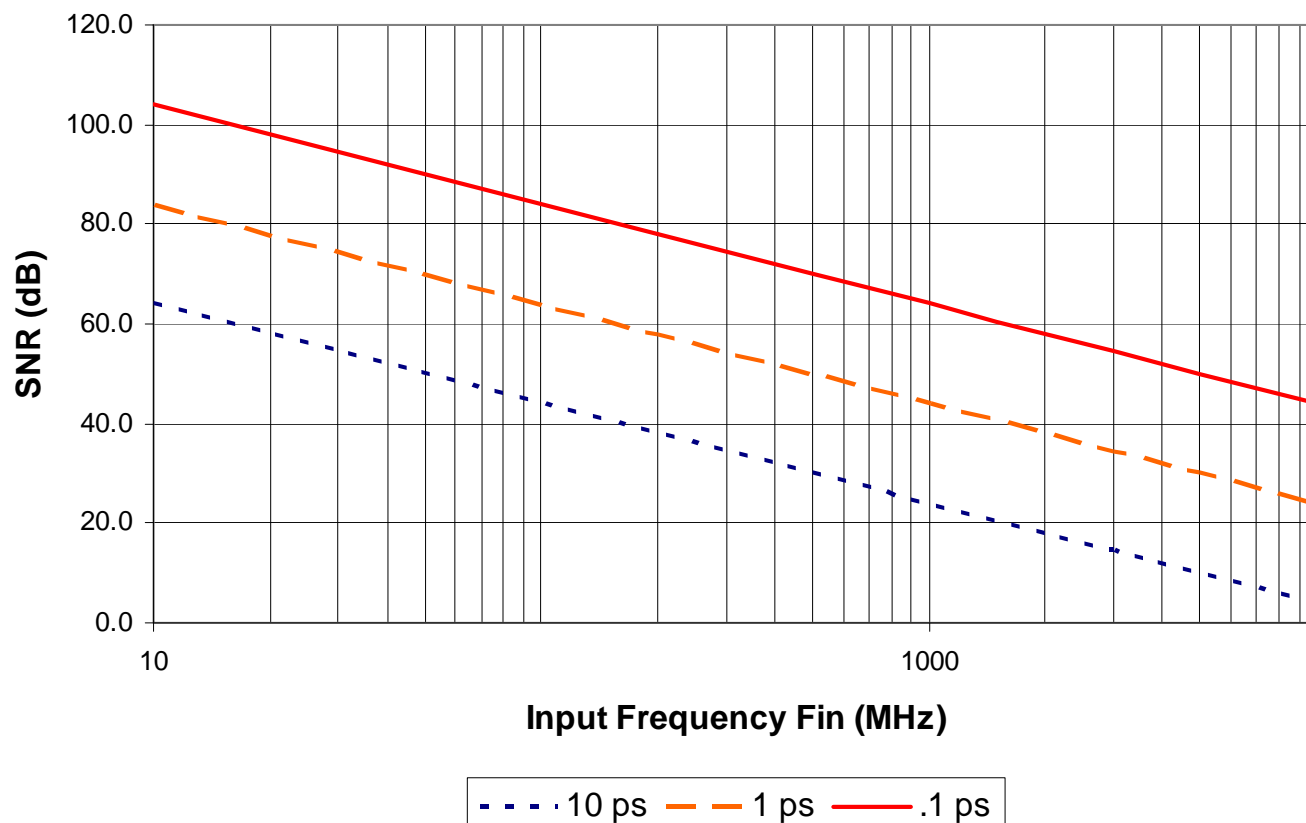
$$C = B \cdot \log_2 (1 + SNR)$$



Applications Example

Data Converter Clocking (5)

SNR vs. F_{in} for Different Jitter Values



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