AN-1898 LVDS Repeaters and Crosspoints Extend the Reach of FPD-Link II Interfaces

ABSTRACT

This application note introduces Texas Instrument's LVDS devices with built-in pre-emphasis and equalization circuits, recommends when it makes sense to employ them with the FPD-Link II SER/DES, shows how to optimally interface them to the SER/DES, and discusses distance gains that may be realized with their signal enhancing functions.

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1   Introduction

Lower cost, increased performance, and smaller size are attributes of many systems that employ SER/DES devices (Serializers and Deserializers). The same holds true for systems utilizing TI's family of embedded clock LVDS SER/DES (FPD-Link II) devices. These SER/DES devices provide a 2-wire serial interface for display applications. One of the limitations these and other SER/DES devices have is the transmission distance between a serializer and a deserializer. One way to extend the reach of SER/DES devices is by using discrete signal buffers with integrated pre-emphasis and equalization circuits.

2   LVDS Signal Conditioners

Transmission line losses are a problem that many system designers dealing with high-speed signals (above 1 MHz) face regularly. In response to a need for devices that mitigate the transmission line losses, Texas Instruments™ has developed a family of LVDS devices with built-in pre-emphasis and equalization circuits. Table 1 shows selected LVDS devices featuring signal enhancing circuits that are most suitable for use with the FPD-Link II SER/DES.

Table 1. Selected LVDS Devices with Integrated Pre-emphasis and Equalization Circuits

NSID	Function	Pre-emphasis (PE)	Equalization (EQ)
DS25BR100	LVDS Buffer / Repeater	0 dB ~6 dB at 1.56 GHz	~4 dB at 1.56 GHz ~8 dB at 1.56 GHz
DS25BR110	LVDS Buffer / Repeater	N/A	0 dB ~4 dB at 1.56 GHz ~8 dB at 1.56 GHz ~16 dB at 1.56 GHz
DS25BR120	LVDS Buffer / Repeater	0 dB ~3 dB at 1.56 GHz ~6 dB at 1.56 GHz ~9 dB at 1.56 GHz	N/A
DS25CP102	LVDS 2×2 Crosspoint Switch	0 dB ~6 dB at 1.56 GHz	0 dB ~4 dB at 1.56 GHz
DS25CP104A	LVDS 4×4 Crosspoint Switch	0 dB ~3 dB at 1.56 GHz ~6 dB at 1.56 GHz ~9 dB at 1.56 GHz	0 dB ~4 dB at 1.56 GHz ~8 dB at 1.56 GHz ~16 dB at 1.56 GHz

Both, pre-emphasis and equalization functions compensate for transmission line losses. Knowing basic principles of their operation is critical when deciding how, when, and where to use them. The following two sections provide an overview of the two functions.

2.1   Pre-Emphasis Feature

Pre-emphasis is a feature of a circuit that boosts the magnitudes of high frequency components of a signal with respect to the magnitudes of low frequency components of the signal. The idea is that the frequency response of the pre-emphasis circuit when combined with the response of a transmission medium will ideally yield a flat response. A network with a flat frequency response does not cause inter symbol interference (ISI). The ISI causes so called ISI jitter, a type of signal jitter caused by cables, printed circuit board (PCB) traces or any other passive network with a similar frequency response.

For system designers, an important parameter of a pre-emphasis circuit is the boost or gain it provides. The higher the boost, the more attenuation the circuit can compensate for and ultimately transmit over a longer transmission medium. As an example, Figure 1 illustrates an output signal from a driver with four pre-emphasis boost levels and the signal's time domain characteristics. The signal is a pattern starting with one bit high (H), followed by one to N bits H, followed by one bit low (L), followed by one to N bits L, followed by an H and an L. Note the signal's nominal amplitude of VOD_L and three distinct boost amplitudes (VOD_H1-3). The boost is simply 20 times log of the ratio of the VOD_H and VOD_L expressed in dB. It is also important to note that the duration of the boost pulse (t_{VOD_H}) should optimally be about 75% of the unit interval (t_{UI}); shorter boost pulse duration will provide lower gain. LVDS devices from Table 1 feature pre-emphasis circuits that provide up to four pre-emphasis levels.
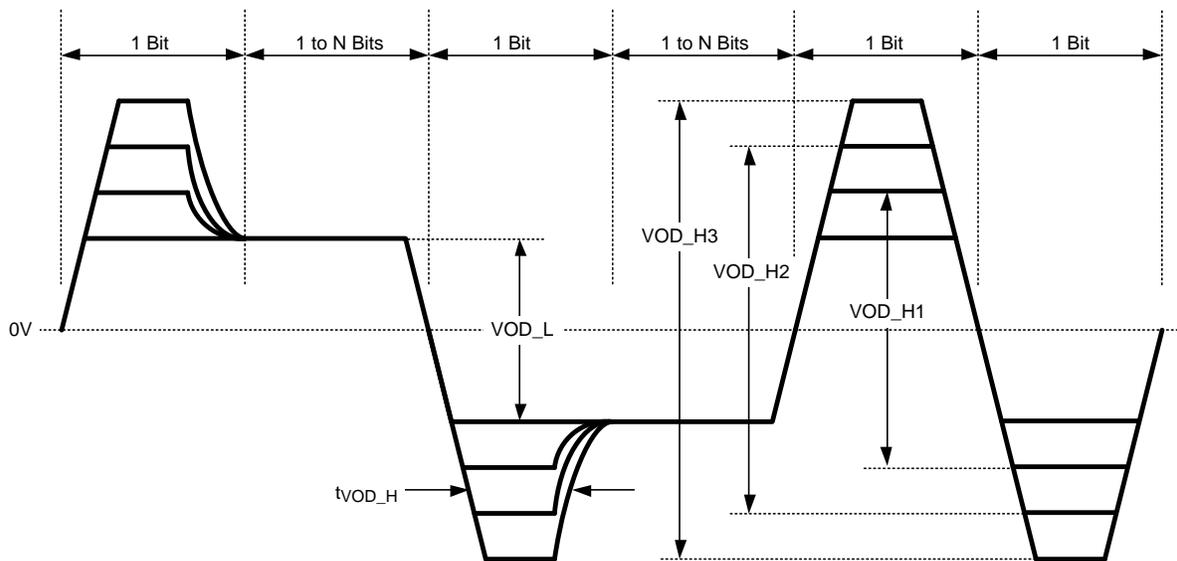
Figure 1. Pre-emphasis Circuit is Most Useful When the Boost Pulse Duration (t$_{VOD\_H}$) is about 75% of the UI

2.2   *Equalization*

The equalizers are typically devices with integrated peaking filters whose frequency response curve from the center frequency, f$_C$, to some lower frequency on the left from the f$_C$ is closely matched to the inverse of the transmission medium's frequency response. As an example, Figure 2 shows a frequency response of a peaking filter with a center frequency at 1 GHz and an inverse of a loss characteristic of a 10m 24 AWG (conductor diameter 0.511 mm) twisted pair cable. Both responses are closely matched up to about 600 MHz. At this frequency, the equalization gain is approximately 6 dB.
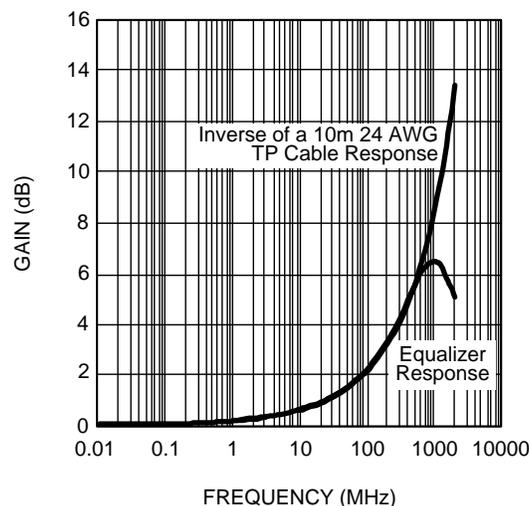

Figure 2. Response of a Peaking Equalizer with the Center Frequency at 1 GHz Closely Matches the Inverse of a 10m 24 AWG Twisted Pair Cable Response

Equalizers can be fixed, variable or adaptive. Fixed equalizers have fixed frequency response and may be employed in applications where transmission media have known fixed length. Variable equalizers may have several equalization boost settings, providing more flexibility with the interconnect length. The most flexible are adaptive equalizers that automatically determine the transmission media loss and apply optimal equalization boost. LVDS devices from Table 1 feature variable equalizers that provide up to four equalization levels.

When compared to pre-emphasis drivers, equalizers are less noisy as they don't require boosting of the signal amplitude, so an equalizer may be the preferred choice for EMI sensitive applications. On the other side, equalizers have to deal with attenuated signals that bring lower signal-to-noise ratio (SNR). With lower SNR, extra caution is recommended to keep the SNR at desired levels. The application note AN-1347 provides PCB design guidelines for high gain equalizers.

3   LVDS Signal Conditioners and FPD-Link II SER/DES

FPD-Link II SER/DES devices provide a 2-wire serial interface for Display applications. (For detailed information see application note AN-1807.) In the application example illustrated in Figure 3, the DS90UR241 is the SER device. It serializes the 18-bit RGB color information along with the three video control signals (VS, HS, and DE) and up to three additional General Purpose (GP0, GP1, and GP2) signals into a single high-speed FPD-Link II serial stream. The DS90UR241 also features an integrated pre-emphasis circuit which mitigates transmission line attenuation and extends the transmission distance. The benefits of the circuit are similar to those of the buffers with integrated pre-emphasis from Table 1; therefore, one may wonder why or when discrete buffers with integrated pre-emphasis may be needed. The explanation follows.
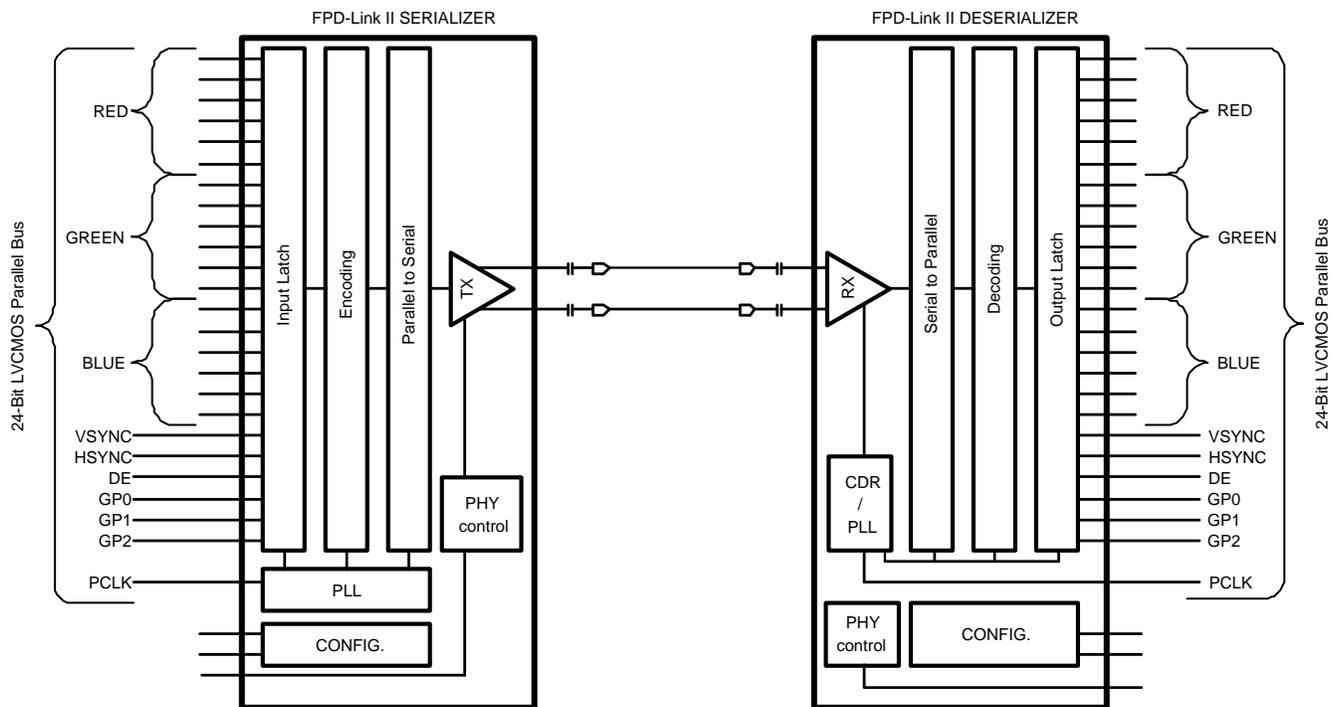

Figure 3. FPD-Link II SER/DES Application Example

One example where use of discrete buffers with pre-emphasis makes sense is applications with multiple image / video sources and displays. Such applications require either a fan-out buffer or a crosspoint switch inserted in the signal path. If the buffer is placed close to the serializer with built-in pre-emphasis circuit, the buffer will block the serializer's pre-emphasis circuit; so, an equivalent circuit in the buffer would be needed instead. Figure 4 is an example of such a scenario. The DS25CP102Q, a 3.125 Gbps 2x2

LVDS crosspoint switch with integrated pre-emphasis and equalization, switches high speed serial signals coming from the two different FPD-Link II SER devices and drives the signal to the remote displays. The transmission distance between the switch and the SER devices is relatively short, so the DS90UR241 pre-emphasis circuit is not needed; however, the distance to the FPD-Link II DES devices from the LVDS crosspoint switch may be significant, therefore, the crosspoint's pre-emphasis circuit may be needed.
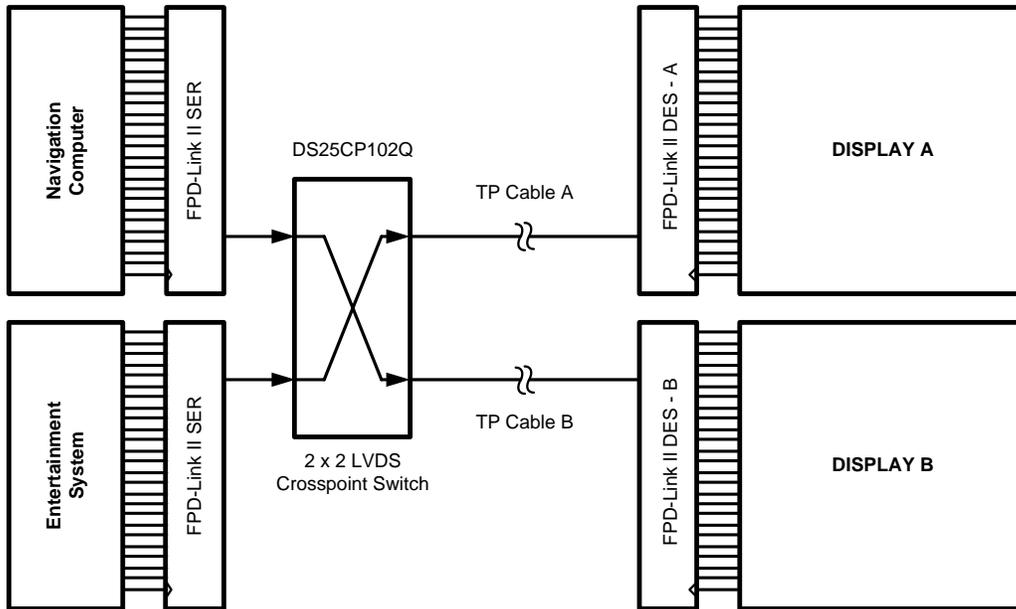
Figure 4. Automotive Infotainment System Example A

If the fan-out buffer or crosspoint switch is placed close to one of the displays, but the second display is remote from the first display, use of buffers with integrated pre-emphasis circuits would make sense again. Figure 5 illustrates the described scenario.
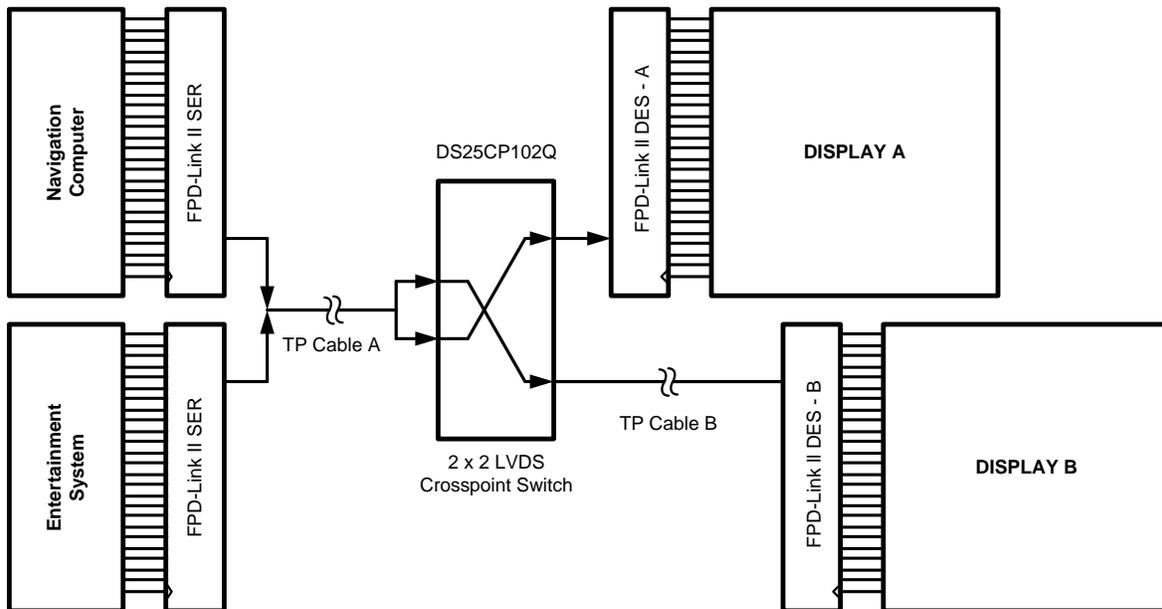
Figure 5. Automotive Infotainment System Example B

In the example illustrated in Figure 5, one can employ the pre-emphasis circuit of the FPD-Link II SER devices to compensate for the losses of the TP Cable A. The pre-emphasis circuit of the crosspoint switch can mitigate the TP Cable B losses. However, with topologies such as this, where more than a single pre-emphasis (or equalization) circuit is employed, one cannot count on the maximum transmission distance gains of both circuits. For example, if one circuit alone extends the distance by M meters and the other extends the distance by N meters, you cannot expect the distance extension of M+N meters if both circuits are employed. When the first circuit compensates for the losses of the first cable, it will only eliminate the ISI jitter (defined earlier in Section 1.1). The remaining residual jitter will be passed onto the second circuit which cannot "clean up" this type of jitter and as a result operate sub-optimally and provide a less than maximum distance extension. The residual jitter may be due to many factors including devices' random jitter components, reflections due to impedance discontinuities in the signal path, crosstalk, etc.

Use of buffers with integrated equalization circuits instead of using the built-in pre-emphasis circuits for the sake of lowering EMI would be the third reason why one would choose a discrete solution as the current FPD-Link II DES devices don't have integrated equalizer circuits.

4   Interface Details

This section provides interface details of two topologies employing the FPD-Link II SER/DES and LVDS Signal Conditioning buffers: one with the pre-emphasis buffer and the other with the equalizer buffer.

Connection diagram with a buffer with integrated pre-emphasis circuit is illustrated in Figure 6. The FPD-Link II SER requires a 100Ω load at the output and is DC coupled to the LVDS buffer. All devices from Table 1 feature integrated input and output 100Ω termination resistors, so no external components are required. The integrated termination resistors not only reduce component count but also save space and minimize the buffer's input and output return losses.

The twisted pair cable is AC coupled at both ends to provide maximum isolation of the source and sink ends due to cable faults. The link is also compatible with AC coupling due to the encoding provided to the data by the FPD-Link II SER. Coupling capacitors should be 0.1µF or greater (i.e. 1µF).

The twisted pair cable needs to be terminated with a 100Ω differential termination resistor. Termination should be placed as close to the DES inputs to minimize any resulting stub lengths.
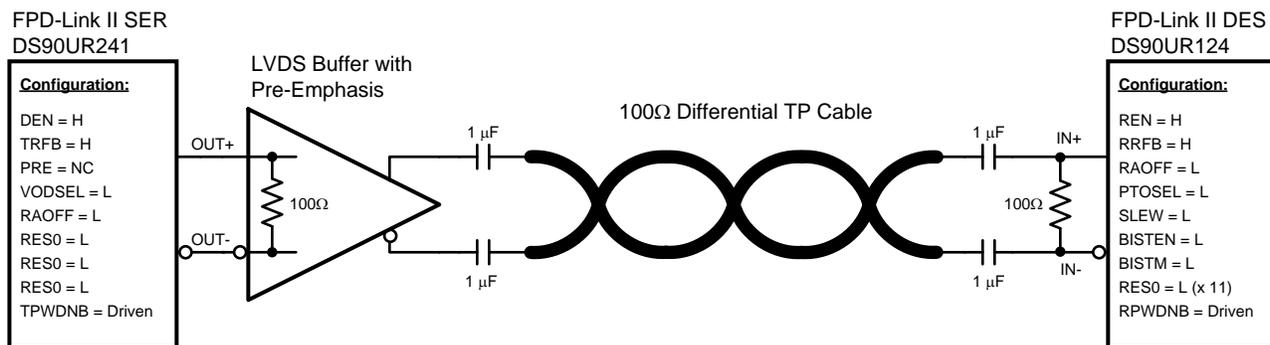

Figure 6. Connection Diagram with a Buffer with Integrated Pre-emphasis Circuit

Connection diagram with a buffer with integrated equalization circuit is illustrated in Figure 7. The FPD-Link II SER requires a 100Ω source termination when interfacing directly to a cable. The source termination minimizes SER output return losses and absorbs any reflections due to the cable and connectors. The SER output buffer provides enough current to maintain LVDS levels despite 50Ω load (100Ω source termination in parallel with 100Ω load termination).

Similar to the topology of Figure 6, the twisted pair cable is AC coupled at both ends to provide maximum isolation of the source and sink ends due to cable faults. The cable is terminated with the buffer's integrated input termination resistor.

The interface between the LVDS buffer output and DES input must be AC coupled due to compatibility reasons. While the LVDS output provides signals with 1.2V offset, the DES receiver expects a signal with 1.8V offset. The AC coupling capacitors will remove the buffer's output signal's DC component. The DES receiver has an input biasing network that will bias the signal to 1.8V. In noisy environments, an external biasing network may be needed as well. Refer to the DS90UR124 datasheet for more details. The transmission line between the LVDS buffer and the DES needs to be terminated as well. The termination resistor needs to be placed as close to the DES inputs as possible to minimize the stub length.
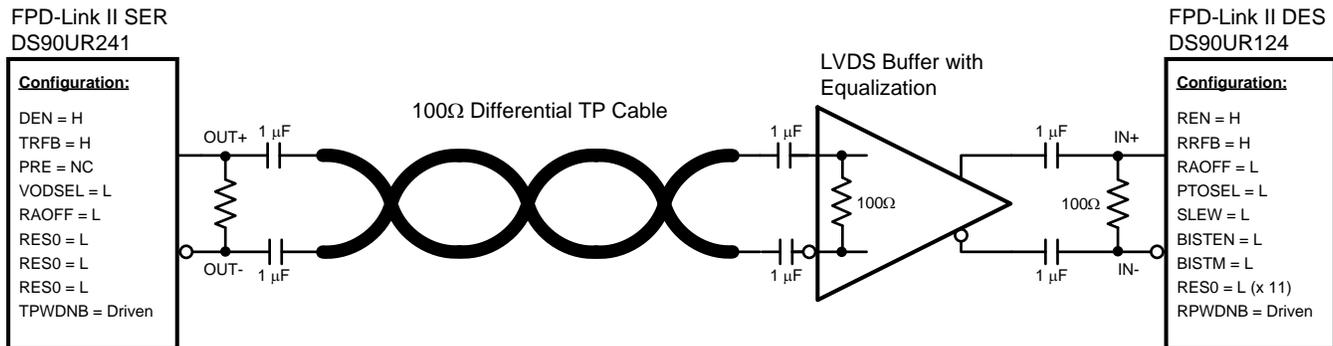
Figure 7. Connection Diagram with a Buffer with Integrated Equalizer Circuit

The link may be tested by either employing parallel BERT test equipment around this application or by using the on-chip BIST mode of the DS90UR241/124 chip set. The device is configured to output a PRBS stream that the DES detects and sets a status flag to indicate a PASS for error free transmission. Please refer to the DS90UR241/124 datasheet for details.

5   How Far, How Fast?

This section of the application note provides performance boundaries of the DS90UR241/124 chipset and distance gains realized with the LVDS buffers featuring built-in pre-emphasis and equalization circuits.

The test configuration illustrated in Figure 6 was implemented using the DS25BR120, an LVDS buffer with integrated pre-emphasis; the configuration of Figure 7 was implemented using the DS25BR110, a LVDS buffer with integrated equalizer circuit. The 24 AWG twisted pair cable of various lengths was used in the experiment. The maximum PCLK frequency as a function of cable length data was obtained from a bench test using external test equipment.

Figure 8 illustrates performance of the DS90UR241/124 chipset with and without the DS25BR120 when interconnected with various length twisted pair cables; Figure 9 illustrates the results with and without the DS25BR110. The shaded areas of the charts indicated the recommend operating PCLK range for the SER/DES chipset which is between 5 and 43 MHz.
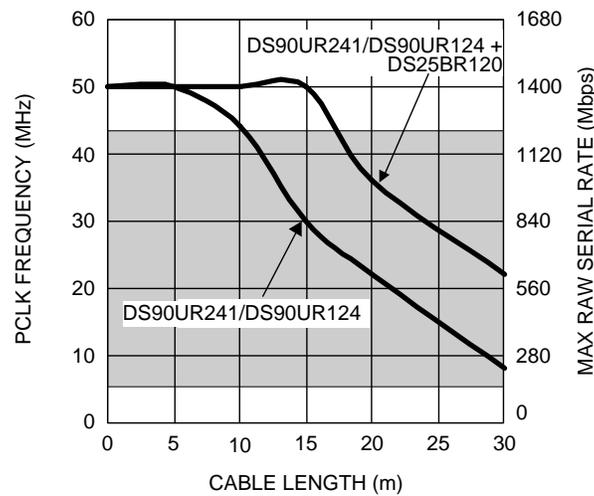
Figure 8. How Far, How Fast – with DS25BR120
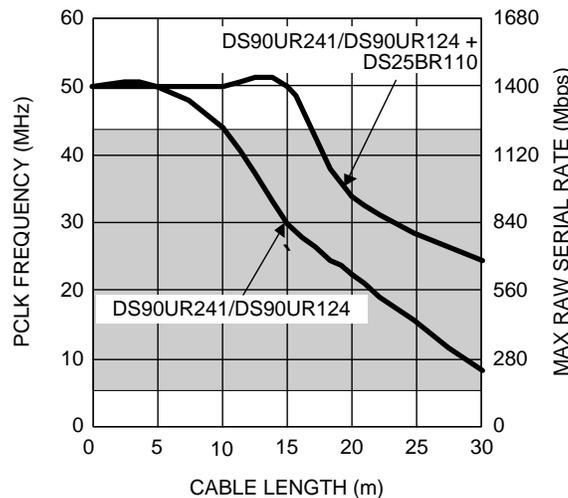
Figure 9. How Far, How Fast – with DS25BR110

Based on the results, DVGA applications (1280 x 480 resolution; at 60 fps and 10% blanking, the required PCLK is 40.55 MHz) are limited to about 10 meters distance between the SER and DES when using 24 AWG twisted pair cables under typical conditions. Given the fact that design margin would be necessary to accommodate device level and system level variations, a more realistic limit would be less than 10m. The use of LVDS devices with built-in pre-emphasis or equalization circuits enables distances that are 50% longer.

Similarly, for WVGA applications (854×480 resolution; at 60 fps and 10% blanking, the PCLK is about 27 MHz), lengths in excess of 10m are possible without the signal conditioning buffers. With the signal conditioners, the possible transmission distances are in the excess of 20m.

6   Conclusion

The FPD-Link II SER/DES have limited reach over twisted pair cables. TI's family of LVDS devices with integrated pre-emphasis and equalization circuits can increase the noise margin and extend the reach of the SER/DES by more than 50%.

For extending the transmission distance to tens, even a hundred of meters over twisted pair cables, refer to the application example described in *AN-1826 Extending the Reach of a FPD-Link II Interface with Cable Drive* ([SNLA103](#)).

7 References

*DS90UR241/DS90UR124 5-43 MHz DC-Balanced 24-Bit LVDS Serializer and Deserializer (*SNLS231*)*

*DS25BR110 3.125 Gbps LVDS Buffer with Receive Equalization (*SNLS255*)*

*DS25BR120 3.125 Gbps LVDS Buffer with Transmit Pre-emphasis (*SNLS256*)*

*AN-1807 FPD-Link II Display SerDes Overview (*SNLA102*)*

*AN-1826 Extending the Reach of a FPD-Link II Interface with Cable Drive (*SNLA103*).*

*AN-1347 – "PCB Layout Techniques for Adaptive Cable Equalizers (*SNLA069*)*

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