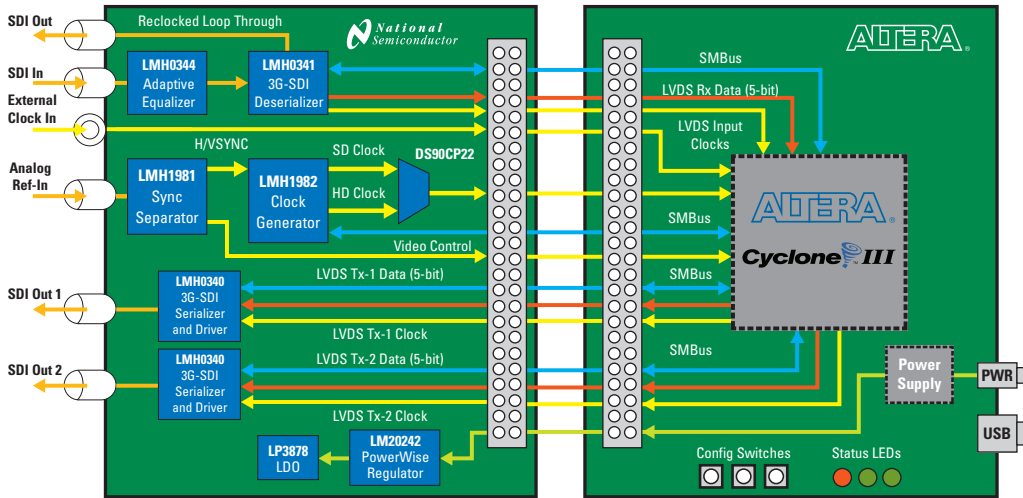


A Comprehensive High-Performance 3G-SDI Development Platform

National Semiconductor and Altera create the perfect balance between high performance analog and logic-rich digital processing



LMH0344: 3G-SDI Adaptive Cable Equalizer

- Equalized cable lengths:
 - 3G: Up to 120m at 0.3 UI max jitter
 - HD: Up to 140m at 0.25 UI max jitter
 - SD: Up to 400m at 0.2 UI max jitter

LMH1981: Multi-Format Video Sync Separator

- 50% sync slicing for superior HSync output jitter
- Horizontal sync output propagation delay <50 ns
- Bi-level & tri-level sync compatible
- Accepts video signals from 0.5 V_{p-p} to 2.0 V_{p-p}
- No external programming required
- 3.3V or 5V single supply operation

LMH1982: Multi-Rate Video Clock Generator

- Simultaneous SD and 3G/HD clock outputs
- No jitter cleaner needed to meet SMPTE specs
- Top of frame pulse with programmable timing
- Supports cross-locking of input-output timing
- Only one VCXO and passive loop filter required

LMH0340 and LMH0341: SDI Serializer and Deserializer

- 30 pS_{p-p} output alignment jitter (HD and 3G rates)
- 0.6 UI minimum input jitter tolerance
- No external VCOs required
- Integrated SMPTE cable drivers, PLL and active reclocked loopthrough

LP3878: Low Noise LDO

- 18 μV output noise for noise sensitive loads
- Stable with ceramic or tantalum capacitors
- Wide 2.5V to 16V input
- Adjustable 1V to 5.5V output
- Load currents up to 800 mA

■ Video
 ■ Clocks*
 ■ Parallel
 ■ Data Control
 ■ Power

*Four clocking options available

- Recovered clock
- Genlock (analog ref in with LMH1981 + LMH1982)
- Local generation (free run with LMH1982)
- External clock

National Semiconductor's FPGA-Attach 3G-SDI Solution

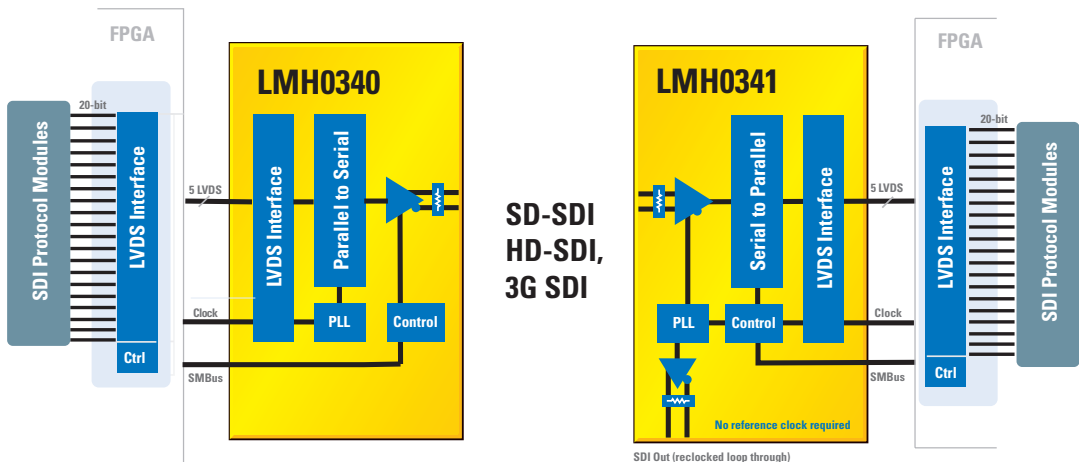
Fully Integrated Solution Delivers Industry-Leading Jitter Performance

LMH0340 and LMH0341 SDI Serializer and Deserializer:

- **Intelligent partitioning increases flexibility**
 - Support for triple rate SDI and DVB-ASI
 - Compatible with all non-transceiver FPGAs including Stratix-III or Cyclone-III devices
 - Leaves digital 'heavy lifting' to FPGA
- **5-bit LVDS replaces traditional 20-bit interface**
 - Reduces FPGA I/O demand and simplifies layout
 - Increases noise immunity and minimizes EMI
 - Decreases board area
- **Low power consumption**
 - Tx: 440 mW, Rx: 590 mW
 - Automatic power save mode when input signal is lost
- **Leading jitter performance**
 - Rx: 0.6 UI minimum input jitter tolerance
 - Tx: 30 ps_{p-p} output alignment jitter
 - No external VCO required
 - Integrated LC based PLL cleans FPGA P_{CLK} jitter
- **Fully featured**
 - Rx: Reclocked active loopthrough with SMPTE cable driver
 - Tx: Integrated SMPTE cable
- **FPGA IP with triple rate SDI support included**
 - Provided in easily augmented HDL source code for faster integration and shorter design time

The LMH0340 and LMH0341 allow for 3G-SDI serialization and deserialization by intelligently partitioning tasks between the analog and digital components of the 3G-SDI solution.

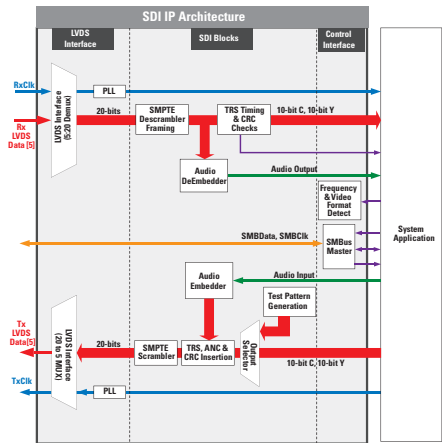
Available in tiny 7 mm x 7 mm LLP-48 packaging.



National's analog intensive SDI SerDes family combines with digital IP on FPGAs to form a complete intelligently partitioned solution. A full set of FPGA firmware is available from Altera as source code to enable quick system integration and faster time to market. This IP implements the SMPTE SDI framing and deframing protocols. A reference design using this IP is available for the Cyclone-III 3C120 host development kit and is compatible with other Cyclone-III devices, including the 3C25.

The IP architecture includes:

- Triple rate SDI support with automatic rate detect
- SMPTE scrambling, descrambling and framing
- Optional embedded audio support from third party IP
- Test pattern generation for development and validation
- 20:5 output muxing and 5:20 input demuxing to support the 5-bit LVDS interface bus
- SMBus management interface



SDI Products

Product	Description	Supported Data Rates	Typ. Power [mW]	Features	Packaging
SerDes Family					
LMH0340SQ	3G HD/SD Serializer	270-2970 Mbps	475	Integrated Cable Driver	LLP-48
LMH0040SQ	HD/SD Serializer	270-1485 Mbps	440	Integrated Cable Driver	LLP-48
LMH0050SQ	HD/SD Serializer	270-1485 Mbps	460	Integrated Cable Driver	LLP-48
LMH0070SQ	SD Serializer	270 Mbps	400	Integrated Cable Driver	LLP-48
LMH0341SQ	3G HD/SD Deserializer	270-2970 Mbps	590	Active Reclocked Loopthrough	LLP-48
LMH0041SQ	HD/SD Deserializer	270-1485 Mbps	550	Active Reclocked Loopthrough	LLP-48
LMH0051SQ	HD/SD Deserializer	270-1485 Mbps	550	Active Reclocked Loopthrough	LLP-48
LMH0071SQ	SD Deserializer	270 Mbps	525	Active Reclocked Loopthrough	LLP-48
Other Products for 3G-SDI					
LMH0344SQ	3G HD/SD Adaptive Cable Equalizer	143 - 2970 Mbps	280	Equalize 120m at 3G rates with <0.3 UI output jitter	LLP-16
LMH0346MH	3G HD/SD Reclocker	270, 1485, 2970 Mbps	370	Ultra-low jitter transfer, >0.6 UI jitter tolerance and 0.09 UI output jitter at 3G rates	TSSOP-20
LMH0356SQ	3G HD/SD Reclocker with 4:1 input mux and Dual Differential Outputs	270, 1485, 2970 Mbps	430	FR4 equalization, >0.6 UI jitter tolerance and 0.09 UI output jitter at 3G rates	LLP-48
LMH0302SQ	3G HD/SD Cable Driver	Up to 2970 Mbps	165	Enable feature, 20 ps additive jitter at 3G rates	LLP-16
LMH0303SQ	3G HD/SD Smart Cable Driver from the PowerWise® family	Up to 2970 Mbps	145	LOS detect, cable detect, 3 mW output power down mode, 20 ps additive jitter at 3G rates, selectable slew rate, SMBus	LLP-16
LMH0307SQ	3G HD/SD Smart Dual Cable Driver from the PowerWise family	Up to 2970 Mbps	270	LOS detect, cable detect, 3 mW output power down mode, 20 ps additive jitter at 3G rates, selectable slew rate, SMBus	LLP-16
DS25CP102TSQ	2x2 LVDS Crosspoint from the PowerWise family	Up to 3125 Mbps/ch	254	Transmit pre-emphasis and receive equalization	LLP-16
DS25CP104TSQ	4x4 LVDS Crosspoint from the PowerWise family	Up to 3125 Mbps/ch	518	Transmit pre-emphasis and receive equalization	LLP-40
DS25CP152TSQ	2x2 LVDS Crosspoint from the PowerWise family	Up to 3125 Mbps/ch	211	Transmit pre-emphasis and receive equalization	LLP-16
LMH1981MT	Multi-format Sync Separator	NTSC, PAL, SECAM, 480i/p, 576i/p, 720p, 1080i/p	31	Outputs: H-sync, V-sync, odd/even, burst/clamp, video format, Auto-video format detection	TSSOP-14
LMH1982SQ	Multi-rate Video Clock generator with Genlock	NTSC, PAL, SECAM, 480i/p, 576i/p, 720p, 1080i/p	250	Simultaneous SD/HD Clocks, exceeds SMPTE jitter spec, genlock and free-run modes, H/V sync and/or 27 MHz ref.	LLP-32

SDI Design Tools

For more information, including application notes and articles on SDI design see: www.national.com/sdi

AN-1113, Serial Digital Video and Interface RAPIDESIGNER Operation and Applications Guide

AN-905, Transmission Line RAPIDESIGNER Operation and Applications Guide

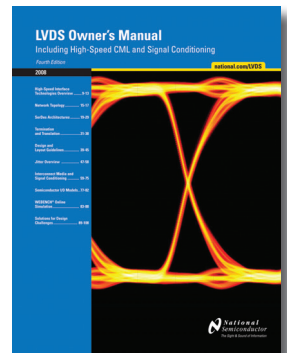
Signal Path Designer #106, Timing is Everything - The Broadcast Video Signal Path

Analog Edge, July 2006 article, Improving Video Clock Generation in Modern Broadcast Video Systems

Broadcast Video Owner's Manual



To download the LVDS Owner's Manual, visit: www.national.com/lvds



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