Programmer’s Guide

Linux Driver Programmer's Guide

ABSTRACT

This programming guide lists the device registers of the DS90UB971.

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

1 Register Maps

In the register definitions under the *TYPE* heading, the following definitions apply:

- RW = Read Write access
- RO = Read Only access
- SC = Register sets on event occurrence and Self-Clears when event ends
- RW/SC = Read Write access, Self-Clearing bit
- COR = Clear on Read
- RO/COR = Read Only, Clear on Read
- LL = Latched Low and held until read, based upon the occurrence of the corresponding event
- LH = Latched High and held until read, based upon the occurrence of the corresponding event
- S = Set based on condition of pin at power up

1.1 Main Registers

Table 1-1 lists the memory-mapped registers for the Main registers. All register offset addresses not listed in Table 1-1 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. MAIN Registers

Address	Acronym	Register Name	Section
0x0	I2C_DEVICE_ID	I2C_DEVICE_ID	Go
0x1	RESET_CTL	RESET_CTL	Go
0x2	GENERAL_CFG	GENERAL_CFG	Go
0x3	MODE_SEL	MODE_SEL	Go
0x6	CLKOUT_CTRL0	CLKOUT_CTRL0	Go
0x7	CLKOUT_CTRL1	CLKOUT_CTRL1	Go
0x8	BCC_WATCHDOG	BCC_WATCHDOG	Go
0x9	I2C_CONTROL1	I2C_CONTROL1	Go
0xA	I2C_CONTROL2	I2C_CONTROL2	Go
0xB	SCL_HIGH_TIME	SCL_HIGH_TIME	Go
0xC	SCL_LOW_TIME	SCL_LOW_TIME	Go
0xD	LOCAL_GPIO_DATA	LOCAL_GPIO_DATA	Go
0xE	GPIO_INPUT_CTL	GPIO_INPUT_CTL	Go
0xF	GPIO_ATP_CTL	GPIO_ATP_CTL	Go
0x11	INTERRUPT_CTL	INTERRUPT_CTL	Go
0x1C	ALARM_CSI_EN	ALARM_CSI_EN	Go
0x1E	ALARM_BC_EN	ALARM_BC_EN	Go
0x20	CSI_POL_SEL	CSI_POL_SEL	Go
0x21	CSI_LP_POLARITY	CSI_LP_POLARITY	Go
0x30	CSI_PKT_VCI_CTRL	CSI_PKT_VCI_CTRL	Go
0x31	CSI_PKT_HDR_TINIT_CTRL	CSI_PKT_HDR_TINIT_CTRL	Go
0x32	BCC_CONFIG	BCC_CONFIG	Go
0x33	DATAPATH_CTL1	DATAPATH_CTL1	Go
0x35	REMOTE_PAR_CAP1	REMOTE_PAR_CAP1	Go
0x37	DES_ID	DES_ID	Go
0x39	SLAVE_ID_0	SLAVE_ID_0	Go
0x3A	SLAVE_ID_1	SLAVE_ID_1	Go
0x3B	SLAVE_ID_2	SLAVE_ID_2	Go
0x3C	SLAVE_ID_3	SLAVE_ID_3	Go
0x3D	SLAVE_ID_4	SLAVE_ID_4	Go
0x3E	SLAVE_ID_5	SLAVE_ID_5	Go
0x3F	SLAVE_ID_6	SLAVE_ID_6	Go

Table 1-1. MAIN Registers (continued)

Address	Acronym	Register Name	Section
0x40	SLAVE_ID_7	SLAVE_ID_7	Go
0x41	SLAVE_ID_ALIAS_0	SLAVE_ID_ALIAS_0	Go
0x42	SLAVE_ID_ALIAS_1	SLAVE_ID_ALIAS_1	Go
0x43	SLAVE_ID_ALIAS_2	SLAVE_ID_ALIAS_2	Go
0x44	SLAVE_ID_ALIAS_3	SLAVE_ID_ALIAS_3	Go
0x45	SLAVE_ID_ALIAS_4	SLAVE_ID_ALIAS_4	Go
0x46	SLAVE_ID_ALIAS_5	SLAVE_ID_ALIAS_5	Go
0x47	SLAVE_ID_ALIAS_6	SLAVE_ID_ALIAS_6	Go
0x48	SLAVE_ID_ALIAS_7	SLAVE_ID_ALIAS_7	Go
0x49	BC_CTRL	BC_CTRL	Go
0x50	REV_MASK_ID	REV_MASK_ID	Go
0x51	DEVICE_STS	DEVICE_STS	Go
0x52	GENERAL_STATUS	GENERAL_STATUS	Go
0x53	GPIO_PIN_STS	GPIO_PIN_STS	Go
0x54	BIST_ERR_CNT	BIST_ERR_CNT	Go
0x55	CRC_ERR_CNT1	CRC_ERR_CNT1	Go
0x56	CRC_ERR_CNT2	CRC_ERR_CNT2	Go
0x57	INTERRUPT_STS	INTERRUPT_STS	Go
0x5C	CSI_ERR_CNT	CSI_ERR_CNT	Go
0x5D	CSI_ERR_STATUS	CSI_ERR_STATUS	Go
0x5E	CSI_ERR_DLANE01	CSI_ERR_DLANE01	Go
0x5F	CSI_ERR_DLANE23	CSI_ERR_DLANE23	Go
0x60	CSI_ERR_CLK_LANE	CSI_ERR_CLK_LANE	Go
0x61	CSI_PKT_HDR_VC_ID	CSI_PKT_HDR_VC_ID	Go
0x62	PKT_HDR_WC_LSB	PKT_HDR_WC_LSB	Go
0x63	PKT_HDR_WC_MSB	PKT_HDR_WC_MSB	Go
0x64	CSI_ECC	CSI_ECC	Go
0x6A	VC_ID0	VC_ID0	Go
0xB0	IND_ACC_CTL	IND_ACC_CTL	Go
0xB1	IND_ACC_ADDR	IND_ACC_ADDR	Go
0xB2	IND_ACC_DATA	IND_ACC_DATA	Go
0xF0	FPD_TX_ID0	FPD_TX_ID0	Go
0xF1	FPD_TX_ID1	FPD_TX_ID1	Go
0xF2	FPD_TX_ID2	FPD_TX_ID2	Go
0xF3	FPD_TX_ID3	FPD_TX_ID3	Go
0xF4	FPD_TX_ID4	FPD_TX_ID4	Go
0xF5	FPD_TX_ID5	FPD_TX_ID5	Go

Complex bit access types are encoded to fit into small table cells. Table 1-2 shows the codes that are used for access types in this section.

Table 1-2. Main Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear

Table 1-2. Main Access Type Codes (continued)

Access Type	Code	Description
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

1.1.1 I2C_DEVICE_ID Register (Address = 0x0) [Default = 0x30]

I2C_DEVICE_ID is shown in Table 1-3.

Return to the Summary Table.

Table 1-3. I2C_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	DEVICE_ID	R/W	0x18	7-bit I2C ID of Serializer. This field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and show the strapped ID. When bit 0 of this register is 1, this field is read/write and can be used to assign any valid I2C ID.
0	SER_ID_OVERRIDE	R/W	0x0	0: Device ID is from strap 1: Register I2C Device ID overrides strapped value

1.1.2 RESET_CTL Register (Address = 0x1) [Default = 0x00]

RESET_CTL is shown in Table 1-4.

Return to the Summary Table.

Table 1-4. RESET_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R/W	0x0	Reserved
2	RESTART_AUTOLOAD	RH/W1S	0x0	Restart ROM Auto-load Setting this bit to 1 causes a re-load of the ROM. This bit is self-clearing.
1	DIGITAL_RESET1	RH/W1S	0x0	Digital Reset1 Resets the entire digital block including registers. This bit is self-clearing. 0: Normal operation 1: Reset
0	DIGITAL_RESET0	RH/W1S	0x0	Digital Reset0 Resets the entire digital block except registers. This bit is self-clearing. 0: Normal operation 1: Reset

1.1.3 GENERAL_CFG Register (Address = 0x2) [Default = 0x32]

GENERAL_CFG is shown in Table 1-5.

Return to the Summary Table.

Table 1-5. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	CONTS_CLK	R/W	0x0	CSI Clock Lane Configuration 0: Non Continuous Clock 1: Continuous Clock
5:4	CSI_LANE_SEL	R/W	0x3	CSI Data lane configuration 00: 1-lane configuration 01: 2-lane configuration 11: 4 lane configuration
3:2	RESERVED	R	0x0	Reserved
1	CRC_TX_GEN_EN	R/W	0x1	Transmitter CRC Generator 0: Disable 1: Enable
0	RESERVED	R/W	0x0	Reserved

1.1.4 MODE_SEL Register (Address = 0x3) [Default = 0x00]

MODE_SEL is shown in Table 1-6.

Return to the Summary Table.

Table 1-6. MODE_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	MODE_OV	R/W	0x0	0: Serializer Mode from the strapped MODE pin 1: Register Mode overrides strapped value
3	MODE_DONE	R	0x0	Indicates MODE value has stabilized and been latched
2:0	MODE_VAL	R/W	0x0	This field always indicates the MODE setting of the device.When bit 4 of this register is 0, this field is read-only and shows the Mode Setting. When bit 4 of this register is 1, this field is read/write and can be used to assign MODE. Mode of operation 000: Synchronous Mode FPD4 001: Synchronous Mode FPD3 011: Non-synch Mode, Internal Clock, FPD3 100: Non-synch Mode, External Clock, FPD3 101: Non-synch Mode, Extrernal Clock FPD4 111: Synchronous Mode FPD3, BC Half-Rate

1.1.5 CLKOUT_CTRL0 Register (Address = 0x6) [Default = 0x01]

CLKOUT_CTRL0 is shown in Table 1-7.

Return to the Summary Table.

Table 1-7. CLKOUT_CTRL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R/W	0x0	Reserved
4:0	DIV_M_VAL	R/W	0x1	M Value for M/N divider for CLKOUT. In CSI Synchronous mode and EXT clock mode, CLKOUT can be programmed using M/N ratio of internal VCO clock to generate clock based on system camera requirement. Internal VCO clock for the M/N divider is derived by foward channel data rate div by 8. When selecting the M/N ratio, they must be set to yield the CLKOUT frequency less than 100MHz.M Value must be >=1. If set to 0 then device will internally set it to 1.

1.1.6 CLKOUT_CTRL1 Register (Address = 0x7) [Default = 0x28]

CLKOUT_CTRL1 is shown in Table 1-8.

Return to the Summary Table.

Table 1-8. CLKOUT_CTRL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DIV_N_VAL	R/W	0x28	N Value for M/N divider for CLKOUT. In CSI Synchronous mode and EXT clock mode, CLKOUT can be programmed by M/N ratio of internal VCO clock to generate clock based on system camera requirement. Internal VCO clock for the M/N divider is derived by foward channel data rate div by 8. When selecting the M/N ratio, they must be set to yield the CLKOUT frequency less than 100MHz.

1.1.7 BCC_WATCHDOG Register (Address = 0x8) [Default = 0xFE]

BCC_WATCHDOG is shown in Table 1-9.

Return to the Summary Table.

Table 1-9. BCC_WATCHDOG Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	BCC_WD_TIMER	R/W	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field must not be set to 0.
0	BCC_WD_TIMER_DISABLE	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

1.1.8 I2C_CONTROL1 Register (Address = 0x9) [Default = 0x1E]

I2C_CONTROL1 is shown in Table 1-10.

Return to the Summary Table.

Table 1-10. I2C_CONTROL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LCL_WRITE_DISABLE	R/W	0x0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C master attached to the DeSerializer. Setting this bit does not affect remote access to I2C slaves at the Serializer.
6:4	I2C_SDA_HOLD	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
3:0	I2C_FILTER_DEPTH	R/W	0xE	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

1.1.9 I2C_CONTROL2 Register (Address = 0xA) [Default = 0x11]

I2C_CONTROL2 is shown in Table 1-11.

Return to the Summary Table.

Table 1-11. I2C_CONTROL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	SDA_OUTPUT_SETUP	R/W	0x1	Remote Ack SDA Output Setup When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value will increase setup time in units of 640ns. The nominal output setup time value for SDA to SCL when this field is 0 is 80ns.
3:2	SDA_OUTPUT_DELAY	R/W	0x0	SDA Output Delay This field configures additional delay on the SDA output relative to the falling edge of SCL. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns 01: 280ns 10: 320ns 11: 360ns
1	I2C_BUS_TIMER_SPEEDUP	R/W	0x0	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
0	I2C_BUS_TIMER_DISABLE	R/W	0x1	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL

1.1.10 SCL_HIGH_TIME Register (Address = 0xB) [Default = 0x7F]

SCL_HIGH_TIME is shown in Table 1-12.

Return to the Summary Table.

Table 1-12. SCL_HIGH_TIME Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SCL_HIGH_TIME_VAL	R/W	0x7F	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional oscillator clock periods. Min_delay= 38.0952ns * (TX_SCL_HIGH + 5)

1.1.11 SCL_LOW_TIME Register (Address = 0xC) [Default = 0x7F]

SCL_LOW_TIME is shown in Table 1-13.

Return to the Summary Table.

Table 1-13. SCL_LOW_TIME Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SCL_LOW_TIME_VAL	R/W	0x7F	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional clock periods. Min_delay= 38.0952ns * (TX_SCL_LOW + 5)

1.1.12 LOCAL_GPIO_DATA Register (Address = 0xD) [Default = 0xF0]

LOCAL_GPIO_DATA is shown in Table 1-14.

Return to the Summary Table.

Table 1-14. LOCAL_GPIO_DATA Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	GPIO_RMTEN	R/W	0xF	Enable remote deserializer GPIO data on local GPIO
3:0	GPIO_OUT_SRC	R/W	0x0	GPIO Output Source This register will set the logical output of 4 GPIOs, GPIO_RMTEN must be disabled and GPIOx_OUT_EN must be enabled. Bit 3 write 0/1 on GPIO3 Bit 2 write 0/1 on GPIO2 Bit 1 write 0/1 on GPIO1 Bit 0 write 0/1 on GPIO0.

1.1.13 GPIO_INPUT_CTL Register (Address = 0xE) [Default = 0x0F]

GPIO_INPUT_CTL is shown in Table 1-15.

Return to the Summary Table.

Table 1-15. GPIO_INPUT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO3_OUT_EN	R/W	0x0	GPIO3 Output Enable 0: Disabled 1: Enabled
6	GPIO2_OUT_EN	R/W	0x0	GPIO2 Output Enable 0: Disabled 1: Enabled
5	GPIO1_OUT_EN	R/W	0x0	GPIO1 Output Enable 0: Disabled 1: Enabled
4	GPIO0_OUT_EN	R/W	0x0	GPIO0 Output Enable 0: Disabled 1: Enabled
3	GPIO3_INPUT_EN	R/W	0x1	GPIO3 Input Enable 0: Disabled 1: Enabled
2	GPIO2_INPUT_EN	R/W	0x1	GPIO2 Input Enable 0: Disabled 1: Enabled
1	GPIO1_INPUT_EN	R/W	0x1	GPIO1 Input Enable 0: Disabled 1: Enabled
0	GPIO0_INPUT_EN	R/W	0x1	GPIO0 Input Enable 0: Disabled 1: Enabled

1.1.14 GPIO_ATP_CTL Register (Address = 0xF) [Default = 0x00]

GPIO_ATP_CTL is shown in Table 1-16.

Return to the Summary Table.

Table 1-16. GPIO_ATP_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO3_PD_DIS	R/W	0x0	1: Disable GPIO internal pull-down resistor 0: Enable GPIO internal pull-down resistor

Table 1-16. GPIO_ATP_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	GPIO2_PD_DIS	R/W	0x0	1: Disable GPIO internal pull-down resistor 0: Enable GPIO internal pull-down resistor
5	GPIO1_PD_DIS	R/W	0x0	1: Disable GPIO internal pull-down resistor 0: Enable GPIO internal pull-down resistor
4	GPIO0_PD_DIS	R/W	0x0	1: Disable GPIO internal pull-down resistor 0: Enable GPIO internal pull-down resistor
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

1.1.15 INTERRUPT_CTL Register (Address = 0x11) [Default = 0x00]

INTERRUPT_CTL is shown in Table 1-17.

Return to the Summary Table.

Table 1-17. INTERRUPT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	INTERRUPT_EN	R/W	0x0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller
6	RESERVED	R/W	0x0	Reserved
5:0	RESERVED	R	0x0	Reserved

1.1.16 ALARM_CSI_EN Register (Address = 0x1C) [Default = 0x00]

ALARM_CSI_EN is shown in Table 1-18.

Return to the Summary Table.

Table 1-18. ALARM_CSI_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5	CSI_NO_FV_EN	R/W	0x0	Enable CSI No Frame Valid alarm
4	DPHY_SYNC_ERR_EN	R/W	0x0	Enable DPHY_SYNC_ERR alarm
3	DPHY_CTRL_ERR_EN	R/W	0x0	Enable DPHY_CTRL_ERR alarm
2	CSI_ECC_2_EN	R/W	0x0	Enable CSI_ECC2 alarm
1	CSI_CHKSUM_ERR_EN	R/W	0x0	Enable CSI checksum error alarm
0	CSI_LENGTH_ERR_EN	R/W	0x0	Enable CSI length error alarm

1.1.17 ALARM_BC_EN Register (Address = 0x1E) [Default = 0x00]

ALARM_BC_EN is shown in Table 1-19.

Return to the Summary Table.

Table 1-19. ALARM_BC_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved

Table 1-19. ALARM_BC_EN Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	RESERVED	R/W	0x0	Reserved
1	CRC_ERR_EN	R/W	0x0	Enable CRC_ERR alarm
0	LINK_DETECT_EN	R/W	0x0	Enable LINK_DETECT alarm

1.1.18 CSI_POL_SEL Register (Address = 0x20) [Default = 0x00]

CSI_POL_SEL is shown in Table 1-20.

Return to the Summary Table.

Table 1-20. CSI_POL_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	POLARITY_CLK0	R/W	0x0	CSI2 CLK lane Polarity. 1= polarity inverted 0= polarity default
3	POLARITY_D3	R/W	0x0	CSI2 Data lane 3 Polarity 1= polarity inverted 0= polarity default
2	POLARITY_D2	R/W	0x0	CSI2 Data lane 2 Polarity 1= polarity inverted 0= polarity default
1	POLARITY_D1	R/W	0x0	CSI2 Data lane 1 Polarity 1= polarity inverted 0= polarity default
0	POLARITY_D0	R/W	0x0	CSI2 Data lane 0 Polarity 1= polarity inverted 0= polarity default

1.1.19 CSI_LP_POLARITY Register (Address = 0x21) [Default = 0x80]

CSI_LP_POLARITY is shown in Table 1-21.

Return to the Summary Table.

Table 1-21. CSI_LP_POLARITY Register Field Descriptions

Bit	Field	Type	Default	Description
7	SUPPORT_16VC	R/W	0x1	1 indicates 16VC support, 0 indicates 4VC support.
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	POL_LP_CLK0	R/W	0x0	LP CSI Clock lane Polarity 1= polarity inverted 0= polarity default
3:0	POL_LP_DATA	R/W	0x0	LP CSI Data lane Polarity, bit[3] is for data lane 3, ..., bit[0] is for data lane 0 1= polarity inverted 0= polarity default

1.1.20 CSI_PKT_VCI_CTRL Register (Address = 0x30) [Default = 0x40]

CSI_PKT_VCI_CTRL is shown in Table 1-22.

Return to the Summary Table.

Table 1-22. CSI_PKT_VCI_CTRL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x1	Reserved
5	PKT_HDR_VCI_ENABLE	R/W	0x0	Enable the CSI packet header selection based on VC for interleaved mode. For interleaved VC packet set this bit to record the packet headers for each VC. For regular data packet ignore this bit.
4:0	RESERVED	R/W	0x0	Reserved

1.1.21 CSI_PKT_HDR_TINIT_CTRL Register (Address = 0x31) [Default = 0x00]

CSI_PKT_HDR_TINIT_CTRL is shown in Table 1-23.

Return to the Summary Table.

Table 1-23. CSI_PKT_HDR_TINIT_CTRL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	PKT_HDR_SEL_VC	R/W	0x0	For interleaved VC packet select the VC ID to display the packet header. This is effective only if reg0x30[5] is set high (PKT_HDR_VCI_ENABLE)
3	RESERVED	R/W	0x0	Reserved
2:0	TINIT_TIME	R/W	0x0	CSI Initial Time after power up. Any LP control data are ignored during this time for all CSI lanes. 000 - 100us, 001= 200us, 010= 300us ...111= 800us etc

1.1.22 BCC_CONFIG Register (Address = 0x32) [Default = 0x09]

BCC_CONFIG is shown in Table 1-24.

Return to the Summary Table.

Table 1-24. BCC_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7	I2C_PASS_ALL	R/W	0x0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
6	I2C_PASSTHROUGH	R/W	0x0	I2C Pass-Through to Deserializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled
5	AUTO_ACK	R/W	0x0	Automatically Acknowledge all I2C writes independent of the forward channel lock state or status of the remote Acknowledge 1: Enable 0: Disable
4	RESERVED	R/W	0x0	Reserved
3	RX_PARITY_CHECKER_ENABLE	R/W	0x1	Parity Checker Enable 0: Disable 1: Enable
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

1.1.23 DATAPATH_CTL1 Register (Address = 0x33) [Default = 0x04]

DATAPATH_CTL1 is shown in Table 1-25.

Return to the Summary Table.

Table 1-25. DATAPATH_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x1	Reserved
1:0	FC_GPIO_EN	R/W	0x0	Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs 00: GPIOs disabled 01: One GPIO 10: Two GPIOs 11: Four GPIOs

1.1.24 REMOTE_PAR_CAP1 Register (Address = 0x35) [Default = 0x00]

REMOTE_PAR_CAP1 is shown in Table 1-26.

Return to the Summary Table.

Table 1-26. REMOTE_PAR_CAP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	FREEZE_DES_CAP	R/W	0x0	Freeze Partner Capabilities Prevent auto-loading of the Partner Capabilities by the Bidirectional Control Channel. The Capabilities will be frozen at the values written in registers 0x1E and 0x1F.
6	RESERVED	R/W	0x0	Reserved
5	BIST_EN	R/W	0x0	Link BIST Enable This bit indicates the remote partner is requesting BIST operation over the FPD-Link III interface. This field is automatically configured by the Bidirectional Control Channel once back channel link has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
4	MPORT	R/W	0x0	Remote Partner Multi-Port capable 0: Remote partner is a single-port device 1: Remote partner is a multi-port device This field is automatically configured by the Bidirectional Control Channel once back channel link has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
3:0	PORT_NUM	R/W	0x0	Remote Partner port number When connected to a multi-port device, this field indicates the port number to which the Serializer is connected. This field is automatically configured by the Bidirectional Control Channel once back channel link has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.

1.1.25 DES_ID Register (Address = 0x37) [Default = 0x7A]

DES_ID is shown in Table 1-27.

Return to the Summary Table.

Table 1-27. DES_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	DESER_ID	R/W	0x3D	Remote Deserializer ID This field is normally loaded automatically from the remote Deserializer.
0	FREEZE_DEVICE_ID	R/W	0x0	Freeze Deserializer Device ID Prevent auto-loading of the Deserializer Device ID from the Back Channel. The ID will be frozen at the value written.

1.1.26 SLAVE_ID_0 Register (Address = 0x39) [Default = 0x00]

SLAVE_ID_0 is shown in Table 1-28.

Return to the Summary Table.

Table 1-28. SLAVE_ID_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_0	R/W	0x0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

1.1.27 SLAVE_ID_1 Register (Address = 0x3A) [Default = 0x00]

SLAVE_ID_1 is shown in Table 1-29.

Return to the Summary Table.

Table 1-29. SLAVE_ID_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_1	R/W	0x0	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

1.1.28 SLAVE_ID_2 Register (Address = 0x3B) [Default = 0x00]

SLAVE_ID_2 is shown in Table 1-30.

Return to the Summary Table.

Table 1-30. SLAVE_ID_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_2	R/W	0x0	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

1.1.29 SLAVE_ID_3 Register (Address = 0x3C) [Default = 0x00]

SLAVE_ID_3 is shown in Table 1-31.

Return to the Summary Table.

Table 1-31. SLAVE_ID_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_3	R/W	0x0	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.

Table 1-31. SLAVE_ID_3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	RESERVED	R	0x0	RESERVED.

1.1.30 SLAVE_ID_4 Register (Address = 0x3D) [Default = 0x00]

SLAVE_ID_4 is shown in Table 1-32.

Return to the Summary Table.

Table 1-32. SLAVE_ID_4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_4	R/W	0x0	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

1.1.31 SLAVE_ID_5 Register (Address = 0x3E) [Default = 0x00]

SLAVE_ID_5 is shown in Table 1-33.

Return to the Summary Table.

Table 1-33. SLAVE_ID_5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_5	R/W	0x0	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

1.1.32 SLAVE_ID_6 Register (Address = 0x3F) [Default = 0x00]

SLAVE_ID_6 is shown in Table 1-34.

Return to the Summary Table.

Table 1-34. SLAVE_ID_6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_6	R/W	0x0	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

1.1.33 SLAVE_ID_7 Register (Address = 0x40) [Default = 0x00]

SLAVE_ID_7 is shown in Table 1-35.

Return to the Summary Table.

Table 1-35. SLAVE_ID_7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_7	R/W	0x0	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

1.1.34 SLAVE_ID_ALIAS_0 Register (Address = 0x41) [Default = 0x00]

SLAVE_ID_ALIAS_0 is shown in Table 1-36.

Return to the Summary Table.

Table 1-36. SLAVE_ID_ALIAS_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_ALIAS_0	R/W	0x0	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_0	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 0 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

1.1.35 SLAVE_ID_ALIAS_1 Register (Address = 0x42) [Default = 0x00]

SLAVE_ID_ALIAS_1 is shown in Table 1-37.

Return to the Summary Table.

Table 1-37. SLAVE_ID_ALIAS_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_ALIAS_1	R/W	0x0	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_1	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 1 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

1.1.36 SLAVE_ID_ALIAS_2 Register (Address = 0x43) [Default = 0x00]

SLAVE_ID_ALIAS_2 is shown in Table 1-38.

Return to the Summary Table.

Table 1-38. SLAVE_ID_ALIAS_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_ALIAS_2	R/W	0x0	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_2	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 2 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

1.1.37 SLAVE_ID_ALIAS_3 Register (Address = 0x44) [Default = 0x00]

SLAVE_ID_ALIAS_3 is shown in Table 1-39.

Return to the Summary Table.

Table 1-39. SLAVE_ID_ALIAS_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_ALIAS_3	R/W	0x0	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_3	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 3 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

1.1.38 SLAVE_ID_ALIAS_4 Register (Address = 0x45) [Default = 0x00]

SLAVE_ID_ALIAS_4 is shown in Table 1-40.

Return to the Summary Table.

Table 1-40. SLAVE_ID_ALIAS_4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_ALIAS_4	R/W	0x0	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_4	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 4 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

1.1.39 SLAVE_ID_ALIAS_5 Register (Address = 0x46) [Default = 0x00]

SLAVE_ID_ALIAS_5 is shown in Table 1-41.

Return to the Summary Table.

Table 1-41. SLAVE_ID_ALIAS_5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_ALIAS_5	R/W	0x0	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_5	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 5 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

1.1.40 SLAVE_ID_ALIAS_6 Register (Address = 0x47) [Default = 0x00]

SLAVE_ID_ALIAS_6 is shown in Table 1-42.

Return to the Summary Table.

Table 1-42. SLAVE_ID_ALIAS_6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_ALIAS_6	R/W	0x0	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_6	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 6 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

1.1.41 SLAVE_ID_ALIAS_7 Register (Address = 0x48) [Default = 0x00]

SLAVE_ID_ALIAS_7 is shown in Table 1-43.

Return to the Summary Table.

Table 1-43. SLAVE_ID_ALIAS_7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SLAVE_ID_ALIAS_7	R/W	0x0	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_7	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 7 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

1.1.42 BC_CTRL Register (Address = 0x49) [Default = 0x00]

BC_CTRL is shown in Table 1-44.

Return to the Summary Table.

Table 1-44. BC_CTRL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	BIST_CRC_ERR_CLR	RH/W1S	0x0	Clear BIST CRC error counter 1: Enable Clear
4	RESERVED	R/W	0x0	Reserved
3	CRC_ERR_CLR	RH/W1S	0x0	Clear CRC error 0: Disable clear 1: Enable clear
2:0	RESERVED	R/W	0x0	Reserved

1.1.43 REV_MASK_ID Register (Address = 0x50) [Default = 0x10]

REV_MASK_ID is shown in Table 1-45.

Return to the Summary Table.

Table 1-45. REV_MASK_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	REVISION_ID	R	0x1	Revision ID 0001: Production Device
3:0	RESERVED	R	0x0	Reserved

1.1.44 DEVICE_STS Register (Address = 0x51) [Default = 0x00]

DEVICE_STS is shown in Table 1-46.

Return to the Summary Table.

Table 1-46. DEVICE_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	CFG_CKSUM_STS	R	0x0	Config Checksum Passed This bit will be set following initialization if the Configuration data in the eFuse ROM had a valid checksum
6	CFG_INIT_DONE	R	0x0	Power-up initialization complete This bit will be set after Initialization is complete. Configuration from eFuse ROM has completed.
5:2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

1.1.45 GENERAL_STATUS Register (Address = 0x52) [Default = 0x05]

GENERAL_STATUS is shown in Table 1-47.

Return to the Summary Table.

Table 1-47. GENERAL_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7	AON_MODE_LATCHED	R	0x0	AON mode is latched (indicating the loss of PLL reference)
6	RX_LOCK_DETECT	R	0x0	Deserializer LOCK status This bit indicates the LOCK status of the Deserializer.
5	RESERVED	R	0x0	Reserved

Table 1-47. GENERAL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	LINK_LOST_FLAG	R	0x0	Back Channel Link lost Status changed This bit is set if a change in BC LINK DET lost status has been detected. This bit will be cleared upon read of CRC ERR CLR register or HS PLL loses lock.
3	BIST_CRC_ERR	R	0x0	BIST Error is detected. The BIST_ERR_CNT register contain the number of bist error
2	HS_PLL_LOCK_VAL	R	0x1	Forward Channel High speed PLL lock flag
1	CRC_ERR	R	0x0	Back Channel CRC error detected This bit is set when the back channel errors detected when BC LINK DET is asserted. This bit will be cleared upon write 1 to the CRC ERR CLR register.
0	LINK_DET	R	0x1	Back Channel Link detect This bit is set when BC link is valid.

1.1.46 GPIO_PIN_STS Register (Address = 0x53) [Default = 0x00]

GPIO_PIN_STS is shown in Table 1-48.

Return to the Summary Table.

Table 1-48. GPIO_PIN_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	GPIO_STS	R	0x0	GPIO Pin Status This register reads the current values on GPIO pins. Bit 3 reads GPIO3 pin status Bit 2 reads GPIO2 status Bit 1 reads GPIO1 status Bit 0 reads GPIO0 status

1.1.47 BIST_ERR_CNT Register (Address = 0x54) [Default = 0x00]

BIST_ERR_CNT is shown in Table 1-49.

Return to the Summary Table.

Table 1-49. BIST_ERR_CNT Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BIST_BC_ERRCNT	R	0x0	CRC error count in BIST mode.

1.1.48 CRC_ERR_CNT1 Register (Address = 0x55) [Default = 0x00]

CRC_ERR_CNT1 is shown in Table 1-50.

Return to the Summary Table.

Table 1-50. CRC_ERR_CNT1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERRCNT1	R	0x0	CRC Error count in Mission Mode (LSB)

1.1.49 CRC_ERR_CNT2 Register (Address = 0x56) [Default = 0x00]

CRC_ERR_CNT2 is shown in Table 1-51.

Return to the Summary Table.

Table 1-51. CRC_ERR_CNT2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERRCNT2	R	0x0	CRC Error count in Mission Mode (MSB)

1.1.50 INTERRUPT_STS Register (Address = 0x57) [Default = 0x00]

INTERRUPT_STS is shown in Table 1-52.

Return to the Summary Table.

Table 1-52. INTERRUPT_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	INTERRUPT	R	0x0	Global Interrupt: Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INT_EN bit in the INTERRUPT_CTL register but does depend on the IE_xxx bits. For example, if IE_RX0 and IS_RX0 are both asserted, the INT bit will be set to 1
6	IS_DEV	R	0x0	Local Device Interrupt: A general device interrupt has been generated. If this bit is set, the LOCAL_DEV_ISR register must be read to determine the source of the interrupt. This interrup is cleared by reading the associated status register(s) for the event(s) that caused the interrupt
5:0	RESERVED	R	0x0	Reserved

1.1.51 CSI_ERR_CNT Register (Address = 0x5C) [Default = 0x00]

CSI_ERR_CNT is shown in Table 1-53.

Return to the Summary Table.

Table 1-53. CSI_ERR_CNT Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI_ERR_CNT	RC	0x0	CSI Error Counter Register This register counts the number of CSI packets received with errors since the last read of the counter. The count increments on uncorrectable 2 bit sync and ECC errors, CSI line length mismatch error and checksum error

1.1.52 CSI_ERR_STATUS Register (Address = 0x5D) [Default = 0x00]

CSI_ERR_STATUS is shown in Table 1-54.

Return to the Summary Table.

Table 1-54. CSI_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	ALL_LANE_SYNC2_ERR	RC	0x0	Indicates a 2 bit sync error (uncorrectable)
3	LINE_LEN_MISMATCH	RC	0x0	Indicates Line length less than the received Packet header Word count
2	CHKSUM_ERR	RC	0x0	Indicates a checksum error detected in the incoming data (uncorrectable)
1	ECC_2BIT_ERR	RC	0x0	Indicates a 2 Bit ECC error (uncorrectable) in the Packet header
0	ECC_1BIT_ERR	RC	0x0	Indicates a 1 Bit ECC error detected in the Packet header

1.1.53 CSI_ERR_DLANE01 Register (Address = 0x5E) [Default = 0x00]

CSI_ERR_DLANE01 is shown in Table 1-55.

Return to the Summary Table.

Table 1-55. CSI_ERR_DLANE01 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SOT_ERROR_1	RC	0x0	Lane 1: Single Bit Error in SYNC Sequence - Correctable
6	SOT_SYNC_ERROR_1	RC	0x0	Lane 1: Multi bit Error in SYNC Sequence - Uncorrectable
5	CNTRL_ERR_HSRQST_1	RC	0x0	Lane 1: Control Error in HS Request Mode
4	RESERVED	RC	0x0	Reserved
3	SOT_ERROR_0	RC	0x0	Lane 0: Single Bit Error in SYNC Sequence - Correctable
2	SOT_SYNC_ERROR_0	RC	0x0	Lane 0: Multi bit Error in SYNC Sequence - Uncorrectable
1	CNTRL_ERR_HSRQST_0	RC	0x0	Lane 0: Control Error in HS Request Mode
0	RESERVED	RC	0x0	Reserved

1.1.54 CSI_ERR_DLANE23 Register (Address = 0x5F) [Default = 0x00]

CSI_ERR_DLANE23 is shown in Table 1-56.

Return to the Summary Table.

Table 1-56. CSI_ERR_DLANE23 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SOT_ERROR_3	RC	0x0	Lane 3: Single Bit Error in SYNC Sequence - Correctable
6	SOT_SYNC_ERROR_3	RC	0x0	Lane 3: Multi bit Error in SYNC Sequence - Uncorrectable
5	CNTRL_ERR_HSRQST_3	RC	0x0	Lane 3: Control Error in HS Request Mode
4	RESERVED	RC	0x0	Reserved
3	SOT_ERROR_2	RC	0x0	Lane 2: Single Bit Error in SYNC Sequence - Correctable
2	SOT_SYNC_ERROR_2	RC	0x0	Lane 2: Multi bit Error in SYNC Sequence - Uncorrectable
1	CNTRL_ERR_HSRQST_2	RC	0x0	Lane 2: Control Error in HS Request Mode
0	RESERVED	RC	0x0	Reserved

1.1.55 CSI_ERR_CLK_LANE Register (Address = 0x60) [Default = 0x00]

CSI_ERR_CLK_LANE is shown in Table 1-57.

Return to the Summary Table.

Table 1-57. CSI_ERR_CLK_LANE Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	RESERVED	RC	0x0	Reserved
3:2	RESERVED	R	0x0	Reserved
1	CNTRL_ERR_HSRQST_CK0	RC	0x0	Clk Lane: Control Error in HS Request Mode
0	RESERVED	RC	0x0	Reserved

1.1.56 CSI_PKT_HDR_VC_ID Register (Address = 0x61) [Default = 0x00]

CSI_PKT_HDR_VC_ID is shown in Table 1-58.

Return to the Summary Table.

Table 1-58. CSI_PKT_HDR_VC_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	LONG_PKT_DATA_ID	R	0x0	Data ID from CSI Packet header

1.1.57 PKT_HDR_WC_LSB Register (Address = 0x62) [Default = 0x00]

PKT_HDR_WC_LSB is shown in Table 1-59.

Return to the Summary Table.

Table 1-59. PKT_HDR_WC_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LONG_PKT_WRD_CNT_LSB	R	0x0	Payload count lower byte from CSI Packet header

1.1.58 PKT_HDR_WC_MSB Register (Address = 0x63) [Default = 0x00]

PKT_HDR_WC_MSB is shown in Table 1-60.

Return to the Summary Table.

Table 1-60. PKT_HDR_WC_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LONG_PKT_WRD_CNT_MSB	R	0x0	Payload count upper byte from CSI Packet header

1.1.59 CSI_ECC Register (Address = 0x64) [Default = 0x00]

CSI_ECC is shown in Table 1-61.

Return to the Summary Table.

Table 1-61. CSI_ECC Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_LENGTH_CHANGE	RC	0x0	Indicates Line length change detected per frame
6	RESERVED	R	0x0	Reserved
5:0	CSI_ECC	R	0x0	CSI ECC byte from packet header

1.1.60 VC_ID0 Register (Address = 0x6A) [Default = 0x00]

VC_ID0 is shown in Table 1-62.

Return to the Summary Table.

Table 1-62. VC_ID0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3:0	VC_ID[3:0]	R	0x0	VC_ID Read

1.1.61 IND_ACC_CTL Register (Address = 0xB0) [Default = 0x00]

IND_ACC_CTL is shown in Table 1-63.

Return to the Summary Table.

Table 1-63. IND_ACC_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	RESERVED
4:2	IA_SEL	R/W	0x0	Indirect Register Select: Selects target for register access 000: PATGEN 001 - 111: RESERVED
1	IA_AUTO_INC	R/W	0x0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1
0	IA_READ	R/W	0x0	Indirect Access Read: Setting this allows generation of a read strobe to the selected register block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the IND_ACC_DATA register. This function is only required for blocks that need to pre-fetch register data.

1.1.62 IND_ACC_ADDR Register (Address = 0xB1) [Default = 0x00]

IND_ACC_ADDR is shown in Table 1-64.

Return to the Summary Table.

Table 1-64. IND_ACC_ADDR Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IA_ADDR	R/W	0x0	Indirect Access Register Offset: This register contains the 8-bit register offset for the indirect access.

1.1.63 IND_ACC_DATA Register (Address = 0xB2) [Default = 0x00]

IND_ACC_DATA is shown in Table 1-65.

Return to the Summary Table.

Table 1-65. IND_ACC_DATA Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IA_DATA	R/W	0x0	Indirect Register Data: Writing this register will cause an indirect write of the IA_DATA value to the selected analog block register. Reading this register will return the value of the selected analog block register

1.1.64 FPD_TX_ID0 Register (Address = 0xF0) [Default = 0x5F]

FPD_TX_ID0 is shown in Table 1-66.

Return to the Summary Table.

Table 1-66. FPD_TX_ID0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_TX_ID0	R	0x5F	FPD_TX_ID0: First byte ID code: '_'

1.1.65 FPD_TX_ID1 Register (Address = 0xF1) [Default = 0x55]

FPD_TX_ID1 is shown in Table 1-67.

Return to the Summary Table.

Table 1-67. FPD_TX_ID1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_TX_ID1	R	0x55	FPD_TX_ID1: 2nd byte of ID code: 'U'

1.1.66 FPD_TX_ID2 Register (Address = 0xF2) [Default = 0x42]

FPD_TX_ID2 is shown in Table 1-68.

Return to the Summary Table.

Table 1-68. FPD_TX_ID2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_TX_ID2	R	0x42	FPD_TX_ID2: 3rd byte of ID code: 'B'

1.1.67 FPD_TX_ID3 Register (Address = 0xF3) [Default = 0x39]

FPD_TX_ID3 is shown in Table 1-69.

Return to the Summary Table.

Table 1-69. FPD_TX_ID3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_TX_ID3	R	0x39	FPD_TX_ID3: 4th byte of ID code: '9'

1.1.68 FPD_TX_ID4 Register (Address = 0xF4) [Default = 0x37]

FPD_TX_ID4 is shown in Table 1-70.

Return to the Summary Table.

Table 1-70. FPD_TX_ID4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_TX_ID4	R	0x37	FPD_TX_ID4: 5th byte of ID code: '7'

1.1.69 FPD_TX_ID5 Register (Address = 0xF5) [Default = 0x31]

FPD_TX_ID5 is shown in Table 1-71.

Return to the Summary Table.

Table 1-71. FPD_TX_ID5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_TX_ID5	R	0x31	FPD_TX_ID5: 6th byte of ID code: '1'

1.2 PATGEN Registers

Table 1-72 lists the memory-mapped registers for the PATGEN registers. All register offset addresses not listed in Table 1-72 should be considered as reserved locations and the register contents should not be modified.

Table 1-72. PATGEN Registers

Address	Acronym	Register Name	Section
0x1	PGEN_CTL	PGEN_CTL	Go
0x2	PGEN_CFG	PGEN_CFG	Go
0x3	PGEN_CSI_DI	PGEN_CSI_DI	Go
0x4	PGEN_LINE_SIZE1	PGEN_LINE_SIZE1	Go
0x5	PGEN_LINE_SIZE0	PGEN_LINE_SIZE0	Go
0x6	PGEN_BAR_SIZE1	PGEN_BAR_SIZE1	Go

Table 1-72. PATGEN Registers (continued)

Address	Acronym	Register Name	Section
0x7	PGEN_BAR_SIZE0	PGEN_BAR_SIZE0	Go
0x8	PGEN_ACT_LPF1	PGEN_ACT_LPF1	Go
0x9	PGEN_ACT_LPF0	PGEN_ACT_LPF0	Go
0xA	PGEN_TOT_LPF1	PGEN_TOT_LPF1	Go
0xB	PGEN_TOT_LPF0	PGEN_TOT_LPF0	Go
0xC	PGEN_LINE_PD1	PGEN_LINE_PD1	Go
0xD	PGEN_LINE_PD0	PGEN_LINE_PD0	Go
0xE	PGEN_VBP	PGEN_VBP	Go
0xF	PGEN_VFP	PGEN_VFP	Go
0x10	PGEN_COLOR0	PGEN_COLOR0	Go
0x11	PGEN_COLOR1	PGEN_COLOR1	Go
0x12	PGEN_COLOR2	PGEN_COLOR2	Go
0x13	PGEN_COLOR3	PGEN_COLOR3	Go
0x14	PGEN_COLOR4	PGEN_COLOR4	Go
0x15	PGEN_COLOR5	PGEN_COLOR5	Go
0x16	PGEN_COLOR6	PGEN_COLOR6	Go
0x17	PGEN_COLOR7	PGEN_COLOR7	Go
0x18	PGEN_COLOR8	PGEN_COLOR8	Go
0x19	PGEN_COLOR9	PGEN_COLOR9	Go
0x1A	PGEN_COLOR10	PGEN_COLOR10	Go
0x1B	PGEN_COLOR11	PGEN_COLOR11	Go
0x1C	PGEN_COLOR12	PGEN_COLOR12	Go
0x1D	PGEN_COLOR13	PGEN_COLOR13	Go
0x1E	PGEN_COLOR14	PGEN_COLOR14	Go
0x1F	PGEN_COLOR15	PGEN_COLOR15	Go

Complex bit access types are encoded to fit into small table cells. Table 1-73 shows the codes that are used for access types in this section.

Table 1-73. PATGEN Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

1.2.1 PGEN_CTL Register (Address = 0x1) [Default = 0x00]

PGEN_CTL is shown in Table 1-74.

Return to the Summary Table.

Table 1-74. PGEN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RESERVED	R/W	0x0	RESERVED

Table 1-74. PGEN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	PGEN_ENABLE	R/W	0x0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

1.2.2 PGEN_CFG Register (Address = 0x2) [Default = 0x33]

PGEN_CFG is shown in Table 1-75.

Return to the Summary Table.

Table 1-75. PGEN_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	PGEN_FIXED_EN	R/W	0x0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0: Send Color Bar Pattern 1: Send Fixed Color Pattern
6	RESERVED	R/W	0x0	RESERVED
5:4	NUM_CBARS	R/W	0x3	Number of Color Bars 00: 1 Color Bar 01: 2 Color Bars 10: 4 Color Bars 11: 8 Color Bars
3:0	BLOCK_SIZE	R/W	0x3	Block Size. For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 12.

1.2.3 PGEN_CSI_DI Register (Address = 0x3) [Default = 0x24]

PGEN_CSI_DI is shown in Table 1-76.

Return to the Summary Table.

Table 1-76. PGEN_CSI_DI Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PGEN_CSI_VC	R/W	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier
5:0	PGEN_CSI_DT	R/W	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.

1.2.4 PGEN_LINE_SIZE1 Register (Address = 0x4) [Default = 0x07]

PGEN_LINE_SIZE1 is shown in Table 1-77.

Return to the Summary Table.

Table 1-77. PGEN_LINE_SIZE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[15:8]	R/W	0x7	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

1.2.5 PGEN_LINE_SIZE0 Register (Address = 0x5) [Default = 0x80]

PGEN_LINE_SIZE0 is shown in Table 1-78.

Return to the Summary Table.

Table 1-78. PGEN_LINE_SIZE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

1.2.6 PGEN_BAR_SIZE1 Register (Address = 0x6) [Default = 0x00]

PGEN_BAR_SIZE1 is shown in Table 1-79.

Return to the Summary Table.

Table 1-79. PGEN_BAR_SIZE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

1.2.7 PGEN_BAR_SIZE0 Register (Address = 0x7) [Default = 0xF0]

PGEN_BAR_SIZE0 is shown in Table 1-80.

Return to the Summary Table.

Table 1-80. PGEN_BAR_SIZE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

1.2.8 PGEN_ACT_LPF1 Register (Address = 0x8) [Default = 0x01]

PGEN_ACT_LPF1 is shown in Table 1-81.

Return to the Summary Table.

Table 1-81. PGEN_ACT_LPF1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[15:8]	R/W	0x1	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

1.2.9 PGEN_ACT_LPF0 Register (Address = 0x9) [Default = 0xE0]

PGEN_ACT_LPF0 is shown in Table 1-82.

Return to the Summary Table.

Table 1-82. PGEN_ACT_LPF0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

1.2.10 PGEN_TOT_LPF1 Register (Address = 0xA) [Default = 0x02]

PGEN_TOT_LPF1 is shown in Table 1-83.

Return to the Summary Table.

Table 1-83. PGEN_TOT_LPF1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[15:8]	R/W	0x2	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

1.2.11 PGEN_TOT_LPF0 Register (Address = 0xB) [Default = 0x0D]

PGEN_TOT_LPF0 is shown in Table 1-84.

Return to the Summary Table.

Table 1-84. PGEN_TOT_LPF0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[7:0]	R/W	0xD	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

1.2.12 PGEN_LINE_PD1 Register (Address = 0xC) [Default = 0x0C]

PGEN_LINE_PD1 is shown in Table 1-85.

Return to the Summary Table.

Table 1-85. PGEN_LINE_PD1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[15:8]	R/W	0xC	Line Period Most significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.

1.2.13 PGEN_LINE_PD0 Register (Address = 0xD) [Default = 0x67]

PGEN_LINE_PD0 is shown in Table 1-86.

Return to the Summary Table.

Table 1-86. PGEN_LINE_PD0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period Least significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.

1.2.14 PGEN_VBP Register (Address = 0xE) [Default = 0x21]

PGEN_VBP is shown in Table 1-87.

Return to the Summary Table.

Table 1-87. PGEN_VBP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_VBP	R/W	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

1.2.15 PGEN_VFP Register (Address = 0xF) [Default = 0x0A]

PGEN_VFP is shown in Table 1-88.

Return to the Summary Table.

Table 1-88. PGEN_VFP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_VFP	R/W	0xA	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

1.2.16 PGEN_COLOR0 Register (Address = 0x10) [Default = 0xAA]

PGEN_COLOR0 is shown in Table 1-89.

Return to the Summary Table.

Table 1-89. PGEN_COLOR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0. For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

1.2.17 PGEN_COLOR1 Register (Address = 0x11) [Default = 0x33]

PGEN_COLOR1 is shown in Table 1-90.

Return to the Summary Table.

Table 1-90. PGEN_COLOR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

1.2.18 PGEN_COLOR2 Register (Address = 0x12) [Default = 0xF0]

PGEN_COLOR2 is shown in Table 1-91.

Return to the Summary Table.

Table 1-91. PGEN_COLOR2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

1.2.19 PGEN_COLOR3 Register (Address = 0x13) [Default = 0x7F]

PGEN_COLOR3 is shown in Table 1-92.

Return to the Summary Table.

Table 1-92. PGEN_COLOR3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

1.2.20 PGEN_COLOR4 Register (Address = 0x14) [Default = 0x55]

PGEN_COLOR4 is shown in Table 1-93.

Return to the Summary Table.

Table 1-93. PGEN_COLOR4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

1.2.21 PGEN_COLOR5 Register (Address = 0x15) [Default = 0xCC]

PGEN_COLOR5 is shown in Table 1-94.

Return to the Summary Table.

Table 1-94. PGEN_COLOR5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

1.2.22 PGEN_COLOR6 Register (Address = 0x16) [Default = 0x0F]

PGEN_COLOR6 is shown in Table 1-95.

Return to the Summary Table.

Table 1-95. PGEN_COLOR6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR6	R/W	0xF	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

1.2.23 PGEN_COLOR7 Register (Address = 0x17) [Default = 0x80]

PGEN_COLOR7 is shown in Table 1-96.

Return to the Summary Table.

Table 1-96. PGEN_COLOR7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

1.2.24 PGEN_COLOR8 Register (Address = 0x18) [Default = 0x00]

PGEN_COLOR8 is shown in Table 1-97.

Return to the Summary Table.

Table 1-97. PGEN_COLOR8 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

1.2.25 PGEN_COLOR9 Register (Address = 0x19) [Default = 0x00]

PGEN_COLOR9 is shown in Table 1-98.

Return to the Summary Table.

Table 1-98. PGEN_COLOR9 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

1.2.26 PGEN_COLOR10 Register (Address = 0x1A) [Default = 0x00]

PGEN_COLOR10 is shown in Table 1-99.

Return to the Summary Table.

Table 1-99. PGEN_COLOR10 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

1.2.27 PGEN_COLOR11 Register (Address = 0x1B) [Default = 0x00]

PGEN_COLOR11 is shown in Table 1-100.

Return to the Summary Table.

Table 1-100. PGEN_COLOR11 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

1.2.28 PGEN_COLOR12 Register (Address = 0x1C) [Default = 0x00]

PGEN_COLOR12 is shown in Table 1-101.

Return to the Summary Table.

Table 1-101. PGEN_COLOR12 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

1.2.29 PGEN_COLOR13 Register (Address = 0x1D) [Default = 0x00]

PGEN_COLOR13 is shown in Table 1-102.

Return to the Summary Table.

Table 1-102. PGEN_COLOR13 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

1.2.30 PGEN_COLOR14 Register (Address = 0x1E) [Default = 0x00]

PGEN_COLOR14 is shown in Table 1-103.

Return to the Summary Table.

Table 1-103. PGEN_COLOR14 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

1.2.31 PGEN_COLOR15 Register (Address = 0x1F) [Default = 0x00]

PGEN_COLOR15 is shown in Table 1-104.

Return to the Summary Table.

Table 1-104. PGEN_COLOR15 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR15	R/W	0x0	Pattern Generator Color 15 For Fixed Color Patterns, this register controls the sixteenth byte of the fixed color pattern.

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2022	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265