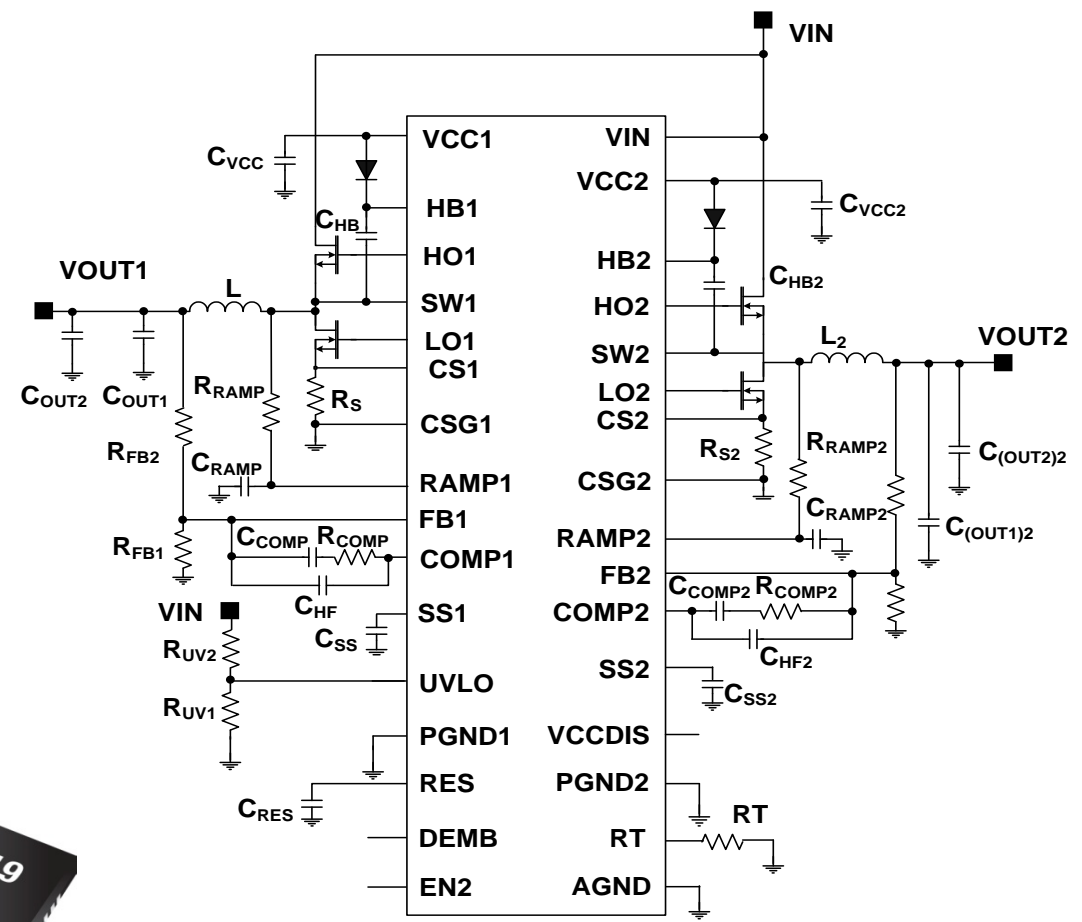


LM(2)5119 Wide VIN Range Dual Synchronous Buck Controller

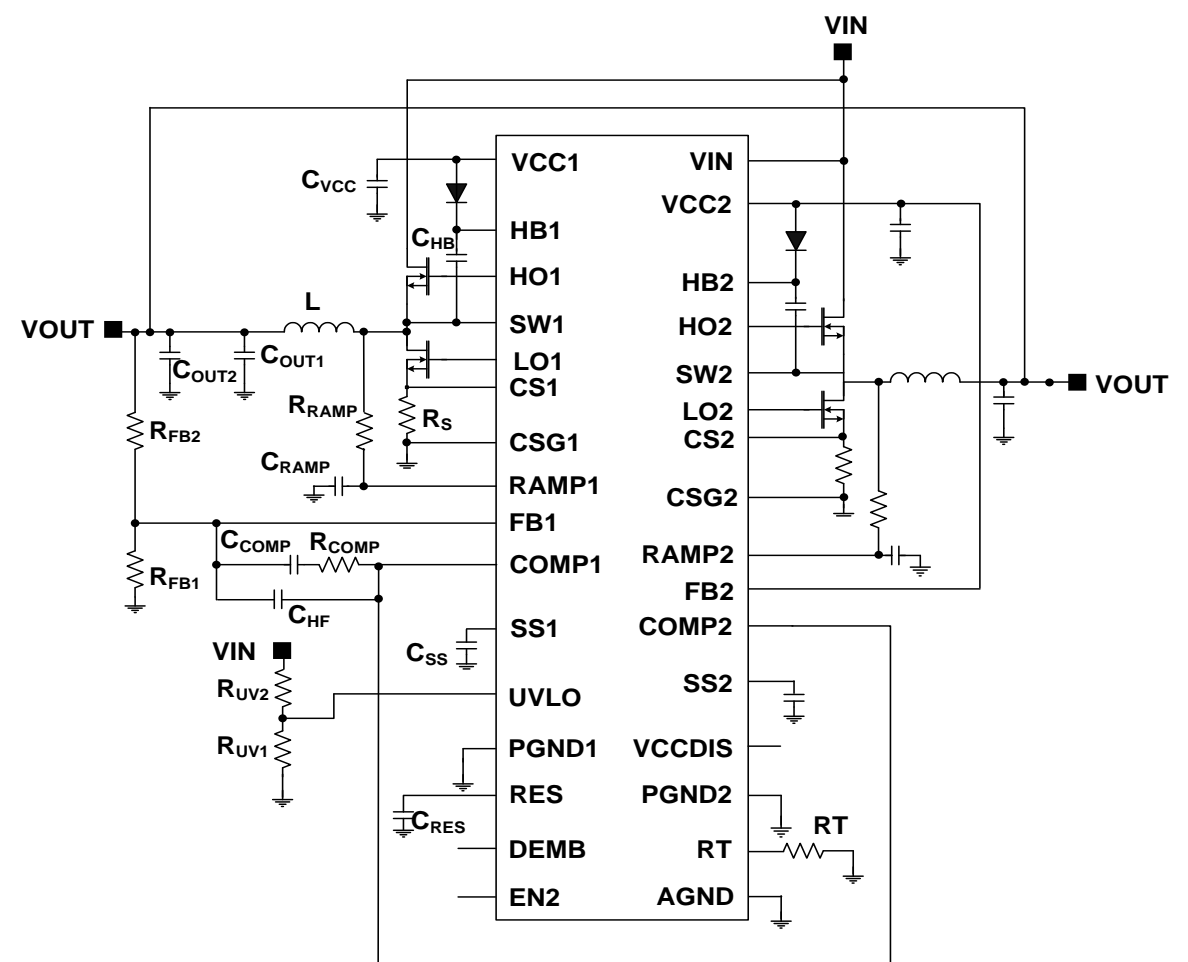


Note: The components calculated here are reasonable starting values for a design using the LM(2)5119 wide VIN controller. As such, components are not optimized for any particular performance attribute. Only one channel is shown. Calculate each channel separately for dual-output designs. Each channel is identical for interleaved designs.

Dual Output Schematic



Interleaved Schematic



Enter design parameters in the shaded cells

Version 1.5 1/27/2014

Step 1: General Requirements

$V_{IN}(\text{min})$ [V]	14
$V_{IN}(\text{max})$ [V]	55
V_{OUT} [V]	5
Max Load Current per Channel [A]	8
Ripple Current as % of Max Load Current	15%
Minimum Duty Cycle	0.09
Maximum Duty Cycle	0.36

Step 2: Interleaved or Dual O/P

Interleaved / Dual Output Operation **Dual Output**

IC Package **WQFN-32**

Recommended IC **LM5119**

Step 3: Switching Frequency

F_{SW} [kHz] **230**

Step 4: Frequency Programming

Recommended R_T [k Ω] **21.7**

Step 5: Filter Inductance

Recommended L_F per channel [μ H] **16.5**

Enter L_F [μ H] **15**

Max Inductor Ripple Current [A] **1.3**

Step 6: Current Limit

Target (% beyond Max Load) **20%**

Output Current at Current Limit Inception [A] **9.6**

Slope Compensation Factor (K) **2.5**

Recommended R_S [m Ω] per Channel **9.4**

Enter Closest Standard Value for R_S [m Ω] **10**

Peak Output Current with Output Short [A] **12.4**

Step 7: Ramp Configuration

R_{RAMP} [k Ω] **73.2**

Recommended C_{RAMP} [pF] **820**

Step 8: Output Capacitors

C_{OUT1} per channel [μ F] **470**

C_{OUT2} per channel [μ F] **20**

Net Output Cap ESR per channel [m Ω] **13**

$C_{OUT1} + C_{OUT2}$ [μ F] **490**

Peak-peak VOUT Ripple [mV] **17.2**

Step 9: Input Capacitors

Input Capacitor C_{IN} [μ F] **17.6**

Input Voltage Ripple [V] **0.49**

Step 10: VIN UV Shutdown

UV Shutdown Voltage [V] **13**

UV Hysteresis, V_{HYS} [V] **1.25**

Upper UVLO Resistor R_{UV2} [k Ω] **62.5**

Lower UVLO Resistor R_{UV1} [k Ω] **6.65**

Step 11: Feedback Resistors

Lower FB Resistor R_{FB1} [k Ω] **1.33**

Upper FB Resistor R_{FB2} [k Ω] **6.98**

Step 12: Compensation Network

Loop Bandwidth [kHz] **11**

Recommended R_{COMP} [k Ω] **27.4**

R_{COMP} [k Ω] **36.5**

Recommended C_{COMP} [nF] **6.3**

C_{COMP} [nF] **6.8**

Recommended Max C_{HF} [pF] **179**

Recommended Min C_{HF} [pF] **17**

C_{HF} [pF] **100**

Step 13: Soft-Start Capacitor

Soft-Start Time [ms] **3.8**

Soft-Start Capacitor C_{SS} [nF] **48**

Step 14: MOSFET Gate Charge

High-side MOSFET Q_g @ V_{VCC} [nC] **30**

Low-side MOSFET Q_g @ V_{VCC} [nC] **30**

MOSFET Total Gate Charge [nC] **60**

Step 15: Boot & VCC Capacitors

Minimum C_{VCC} [μ F] **0.40**

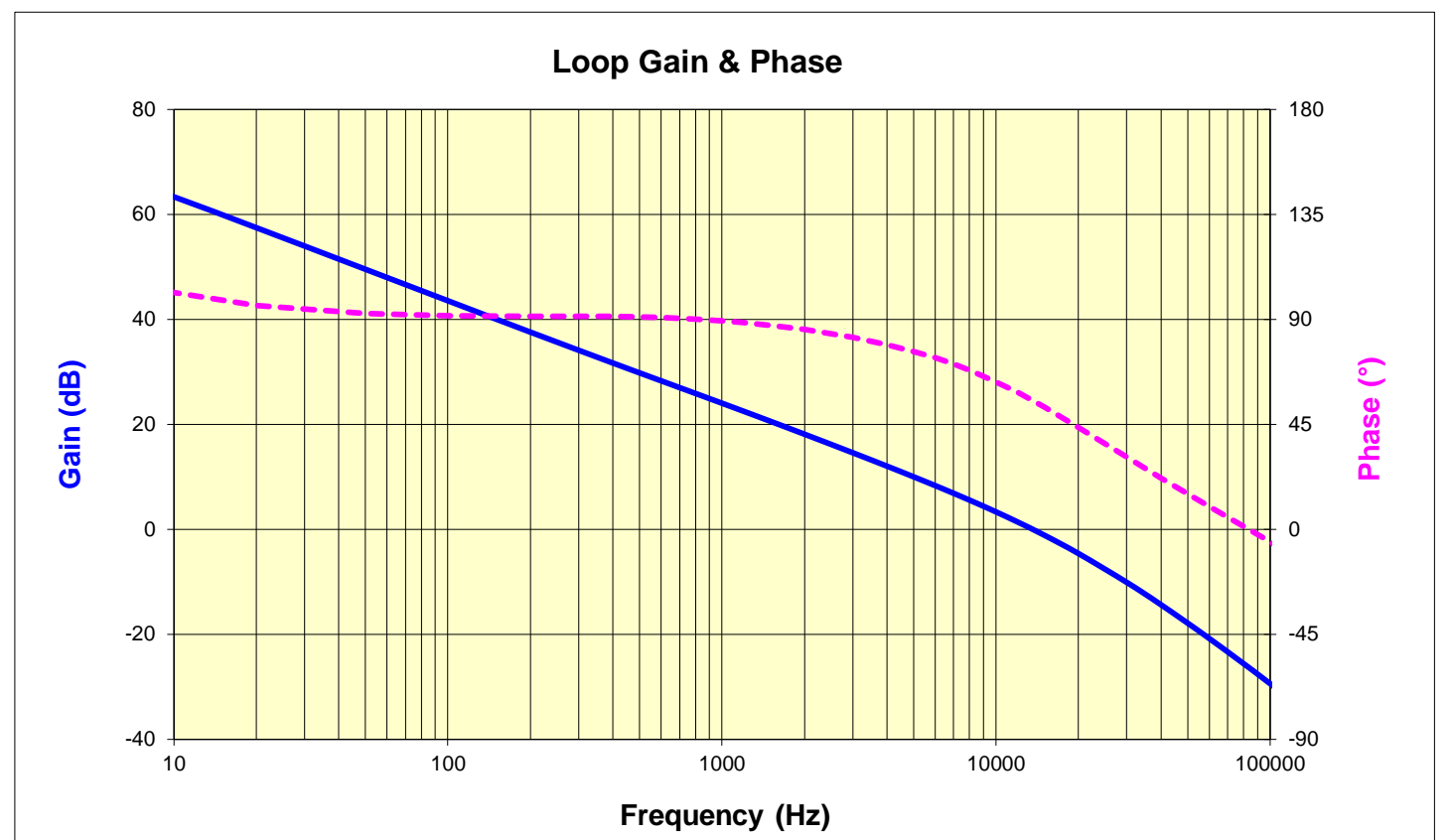
Minimum C_{HB} [μ F] **0.20**

VCC Run Current I_{VCC} [mA] **18**

Step 16: Restart Capacitor

Restart Time [ms] **59**

Restart Capacitor C_{RES} [μ F] **0.47**



LM(2)5119 Power Dissipation Calculations



Enter design parameters in the shaded cells

Common Assumptions

Ambient Temperature T_A	50°C
Package thermal Resistance R_{JA}	40°C/W
External VCC Select "Yes" or "No"	Yes
External VCC (V)	10

Channel 2 Requirements

High-side MOSFET Q_g @ V_{VCC} (nC)	20
Low-side MOSFET Q_g @ V_{VCC} (nC)	46
Channel 2 Total Gate Charge (nC)	66
Channel 2 VCC Run Current I_{CC} (mA)	17



Channel 1 Thermal Calculations

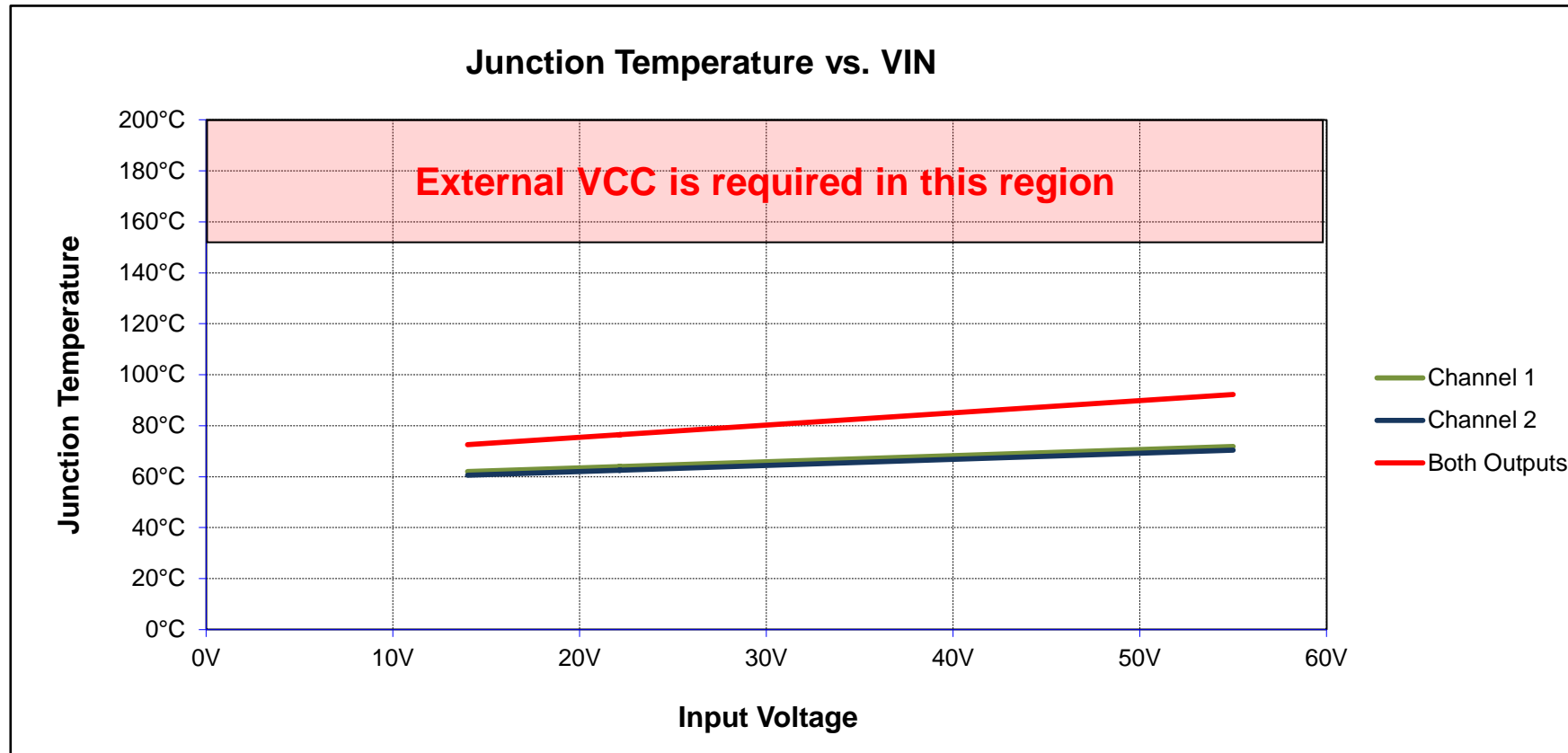
VIN	14.0V	18.1V	22.2V	22.1V	30.4V	34.5V	38.6V	42.7V	46.8V	50.9V	55.0V
IC Power	0.300W	0.325W	0.349W	0.349W	0.398W	0.423W	0.448W	0.472W	0.497W	0.521W	0.546W
ΔT_J above T_A	12°C	13°C	14°C	14°C	16°C	17°C	18°C	19°C	20°C	21°C	22°C
Junction Temperature	62°C	63°C	64°C	64°C	66°C	67°C	68°C	69°C	70°C	71°C	72°C

Channel 2 Thermal Calculations

VIN	14.0V	18.1V	22.2V	22.1V	30.4V	34.5V	38.6V	42.7V	46.8V	50.9V	55.0V
IC Power	0.264W	0.288W	0.313W	0.312W	0.362W	0.387W	0.411W	0.436W	0.461W	0.485W	0.510W
ΔT_J above T_A	11°C	12°C	13°C	12°C	14°C	15°C	16°C	17°C	18°C	19°C	20°C
Junction Temperature	61°C	62°C	63°C	62°C	64°C	65°C	66°C	67°C	68°C	69°C	70°C

Channel 1 + Channel 2 Thermal Calculations

VIN	14.0V	18.1V	22.2V	22.1V	30.4V	34.5V	38.6V	42.7V	46.8V	50.9V	55.0V
Total IC Power	0.564W	0.613W	0.662W	0.661W	0.761W	0.810W	0.859W	0.908W	0.957W	1.007W	1.056W
ΔT_J above T_A	23°C	25°C	26°C	26°C	30°C	32°C	34°C	36°C	38°C	40°C	42°C
Junction Temperature	73°C	75°C	76°C	76°C	80°C	82°C	84°C	86°C	88°C	90°C	92°C



The graph labeled "Channel 1" is the junction temperature rise for Channel 1 operating with Channel 2 off. The "Channel 2" graph is the junction temperature for Channel 2 operating with Channel 1 off. The graph labeled "Both Outputs" gives the junction temperature with both outputs operating.

Potentially high junction temperatures at high VIN may occur when both outputs are operating. Either decrease the switching frequency, decrease VIN, select lower gate charge MOSFETs or use an external source for VCC to reduce operating junction temperature.

LM(2)5119 Bode Plot Calculations



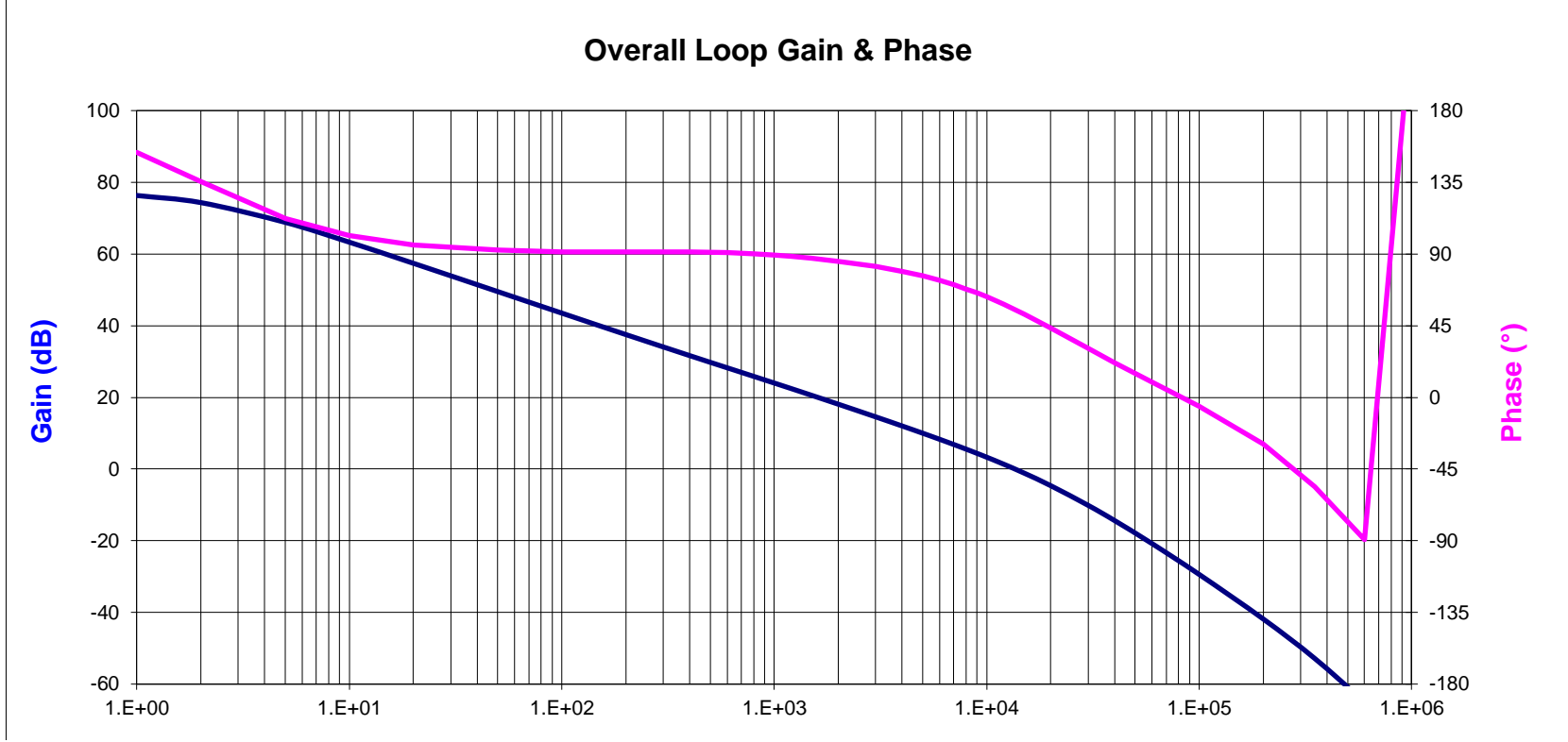
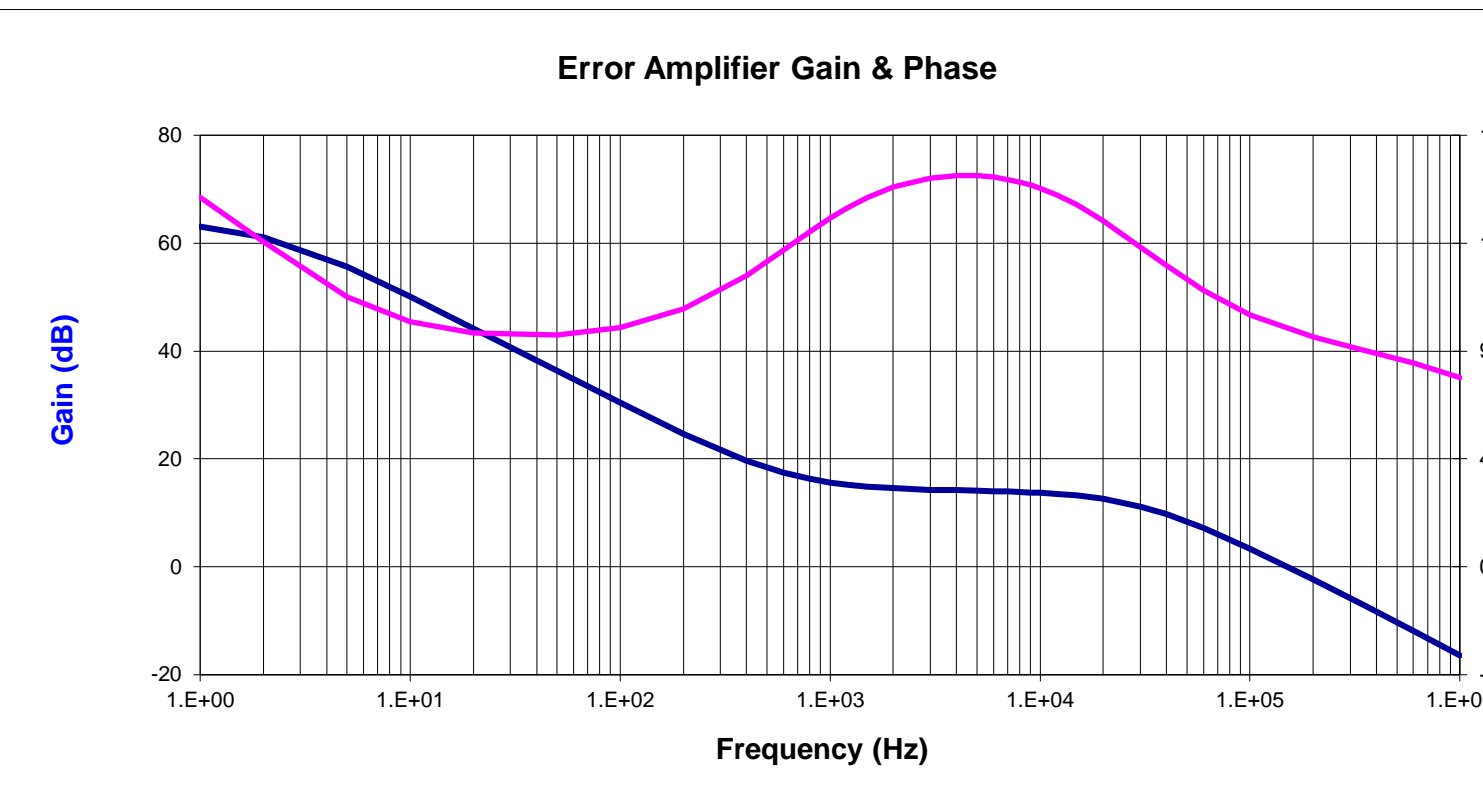
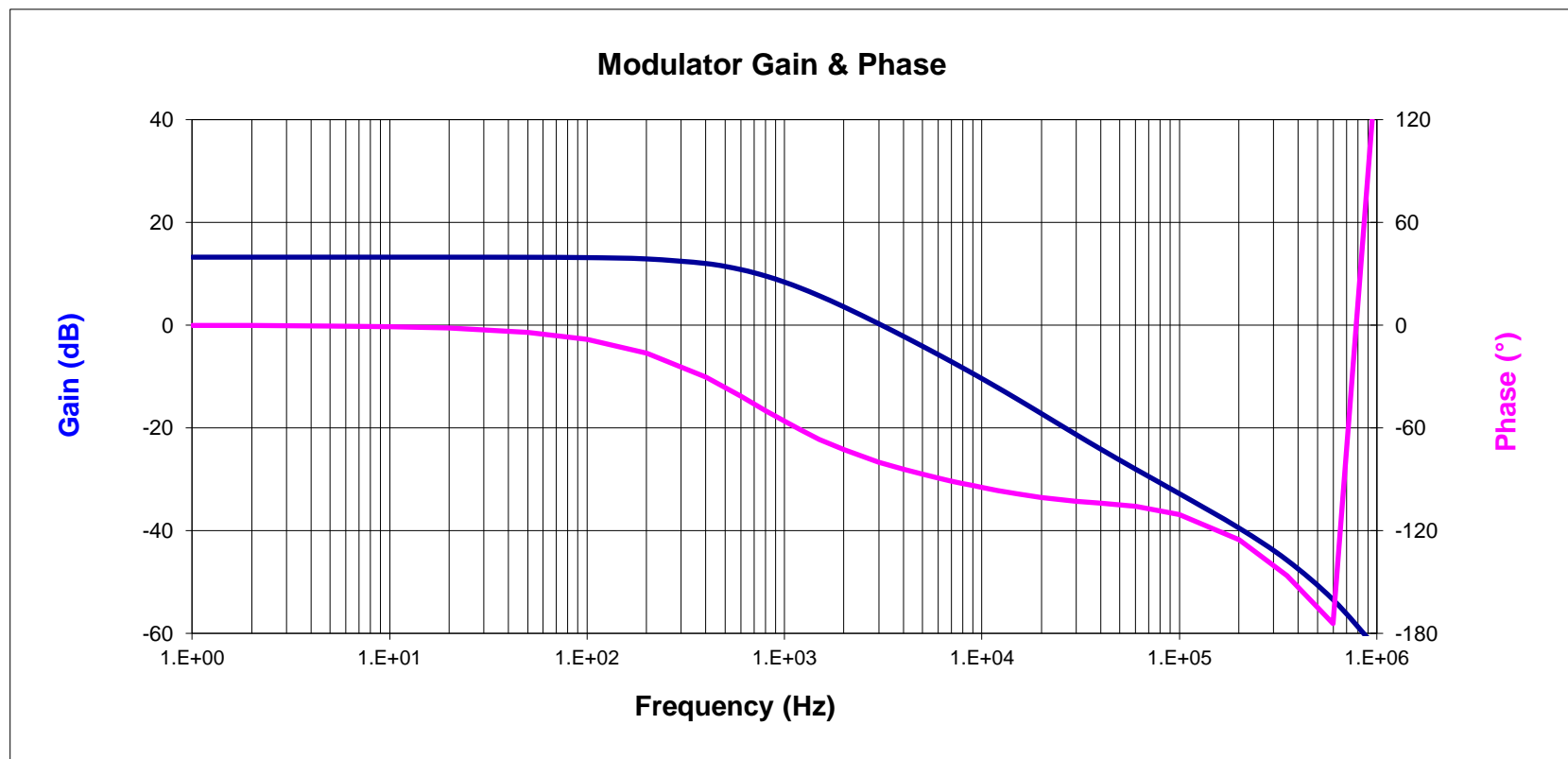
Frequency (Hz)	Frequency (rad/sec)	Modulator Gain (dB)	Modulator Phase (°)	Error Amplifier Gain (dB)	Error Amplifier Phase (°)	Loop Gain (dB)	Loop Phase (°)
1	6.28E+00	13.2	-0.1	63	154	76.4	153.9
2	1.26E+01	13.2	-0.2	61	136	74.4	135.6
5	3.14E+01	13.2	-0.4	56	113	68.9	112.3
10	6.28E+01	13.2	-0.8	50	102	63.3	101.6
20	1.26E+02	13.2	-1.7	44	98	57.5	95.9
50	3.14E+02	13.2	-4.2	36	97	49.5	92.6
100	6.28E+02	13.1	-8.3	30	100	43.5	91.6
200	1.26E+03	12.9	-16.2	25	108	37.6	91.3
400	2.51E+03	12.0	-30.2	20	121	31.7	91.2
600	3.77E+03	10.8	-41.3	17	132	28.3	90.8
800	5.03E+03	9.6	-49.7	16	140	25.9	90.2
1000	6.28E+03	8.4	-56.1	16	146	24.0	89.4
1200	7.54E+03	7.2	-61.1	15	150	22.5	88.6
1500	9.42E+03	5.7	-66.6	15	154	20.6	87.5
2000	1.26E+04	3.6	-72.8	15	158	18.1	85.7
3000	1.88E+04	0.3	-79.9	14	162	14.6	82.3
4000	2.51E+04	-2.2	-84.1	14	163	12.0	79.2
5000	3.14E+04	-4.1	-86.9	14	163	10.0	76.3
6000	3.77E+04	-5.7	-89.1	14	163	8.3	73.5
7000	4.40E+04	-7.1	-90.9	14	162	6.9	70.7
8000	5.03E+04	-8.3	-92.4	14	160	5.6	68.1
9000	5.65E+04	-9.4	-93.6	14	159	4.4	65.6
10000	6.28E+04	-10.4	-94.7	14	158	3.3	63.2
12000	7.54E+04	-12.1	-96.6	14	155	1.4	58.6
15000	9.42E+04	-14.3	-98.6	13	151	-1.1	52.4
20000	1.26E+05	-17.2	-100.7	13	144	-4.6	43.7
30000	1.88E+05	-21.3	-102.7	11	134	-10.1	30.9
40000	2.51E+05	-24.1	-103.7	10	126	-14.4	21.9
60000	3.77E+05	-28.0	-105.7	7	115	-20.8	9.7
100000	6.28E+05	-32.8	-110.6	3	105	-29.4	-5.4
200000	1.26E+06	-39.5	-125.1	-2	96	-41.8	-29.3
350000	2.20E+06	-45.7	-146.3	-7	90	-52.9	-55.9
600000	3.77E+06	-53.4	-174.3	-12	85	-65.3	-89.2
1000000	6.28E+06	-62.9	157.3	-16	79	-79.4	236.3

Frequency Compensation Parameters

Parameter	Value	Value
Modulator		
ω_{p_lf}	4382 rad/s	697 Hz
ω_{p_hf}	115000 rad/s	18.3 kHz
ω_{z_esr}	163666 rad/s	26.0 kHz
ω_{p_esr}	4009820 rad/s	638 kHz
ω_n	722566 rad/s	115 kHz
A_m	4.6 V/V	13.2 dB
Error Amplifier		
ω_{zero}	4029 rad/s	641 Hz
ω_{pole}	20756 rad/s	3.3 kHz
ω_{hf}	278002 rad/s	44.2 kHz
ω_{bw}	1.9E+07 rad/s	3 MHz
A_{OL}	10000 V/V	80 dB
ω_{ol}	1885 rad/s	300 Hz
A_{EA}	-1.57 V/V	
Z_{EA}	3303 Ω	
ω_o	20756 rad/s	3.3 kHz
Z_{ea}	4.883 Ω	
K_{FB}	0.160 V/V	-15.9 dB

Additional Definitions

RLOAD	0.625	Ω
DC GAIN MOI	0.006	V/V
VCC	7.6	V



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