Product Bulletin

TMS320TCI1x UMTS Infrastructure Chipset

Key Benefits

- Eliminates ASIC development costs while maintaining the same flexibility as DSP+custom ASIC solution
- Reduces bill of materials cost up to 50 percent – doubles channel density to 64 channels
- Flexible for OEM product differentiation – chipset can be configured and controlled through DSP software

The new TMS320TCI1x UMTS infrastructure chipset from Texas Instruments offers substantial development and bill of materials (BOM) cost reduction for cellular infrastructure original equipment manufacturers (OEMs). The chipset includes the TMS320TCI100 digital signal processor (DSP), which is a code- and pin-compatible version of the TMS320C6416 DSP, and runs at 720 MHz; the TMS320TCI110 receive chip rate application-specific standard processor (ASSP); and the TMS320TCI120 transmit chip-rate ASSP.

With the TCI1x UMTS infrastructure chipset, OEMs can differentiate their products without incurring excessive research and development expenditures. The chipset provides a single platform with the same flexibility as OEMs' current DSP+custom ASIC solutions at a substantially lower cost. The cost savings include virtual elimination of up-front ASIC development costs and a 50 percent reduction in BOM costs. The TCI110 and TCI120 ASSPs are comprised of flexible hardware resources that are allocated, de-allocated, configured and controlled via commands and register settings under real-time DSP software control. Parameters such as the number of sectors, users and fingers per given user; search window lengths; and accumulation lengths are controlled via the TCI100 DSP software, allowing manufacturers to tailor the chipset to meet their unique requirements.

TI UMTS Infrastructure Chipset Solution

The chipset is a highly integrated solution consisting of the high-performance TCI100 DSP, the TCI110 receive ASSP and the TCI120 transmit ASSP. The TCI110 ASSP, along with a TCI100 DSP acting as a chip rate assist (CRA) DSP, implements the receive chip rate functionality. The CRA DSP is used to control and configure the TCI110 ASSP and to host

UMTS Infrastructure Chipset

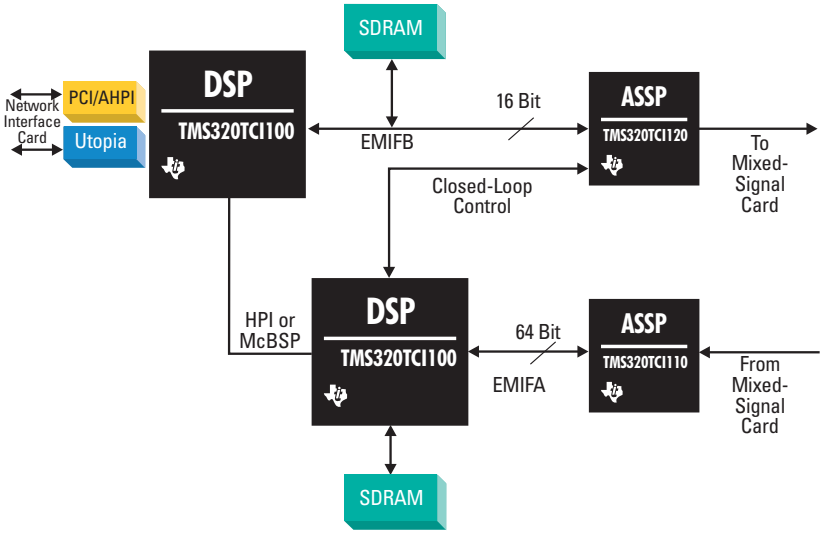

Figure 1: Channel card based on the TCI1x UMTS Infrastructure Chipset

chip-rate processing algorithms such as channel estimation and maximal ratio combining. The TCI120 ASSP implements the transmit chip rate functionality. An additional TCI100 DSP, acting as a symbol-rate DSP, implements both transmit and receive symbol-rate functionality.

TCI100 DSP

The high-performance TCI100 DSP is optimized for wireless infrastructure applications and operates at a clock speed of 720 MHz. It has two multipliers that support four 16 × 16-bit multiplies per cycle. The enhanced direct memory access (DMA) controller has 64 independent channels and can be operated in slave mode. The embedded Viterbi coprocessor can support 350 voice (12.2-kbps AMR) channels and the Turbo coprocessor can support 28 high-data-rate (384-kbps) users. The TCI100 DSP supports a 64-bit external memory interface (EMIF) bus (EMIFA), a 16-bit EMIF bus (EMIFB) and other commonly used peripherals such as PCI, HPI, Utopia and multi-channel buffered serial port (McBSP).

TCI110 Receive Chip-Rate ASSP

The TCI110 ASSP is a highly flexible and customizable receive chip-rate ASSP. It performs uplink chip-rate processing in coordination with a TCI100 DSP. This CRA DSP controls and configures the TCI110 ASSP device and performs chip-rate functions such as channel estimation and maximal ratio combining of the rake fingers. The highly flexible, programmable device provides the ability to dynamically allocate correlation resources based on the number of user equipment (UE) supported by the device, the data rate of each UE and the number of multi-paths (rake fingers) per UE.

The main functional blocks of the TCI110 ASSP include:

TCI110 ASSP Block Diagram

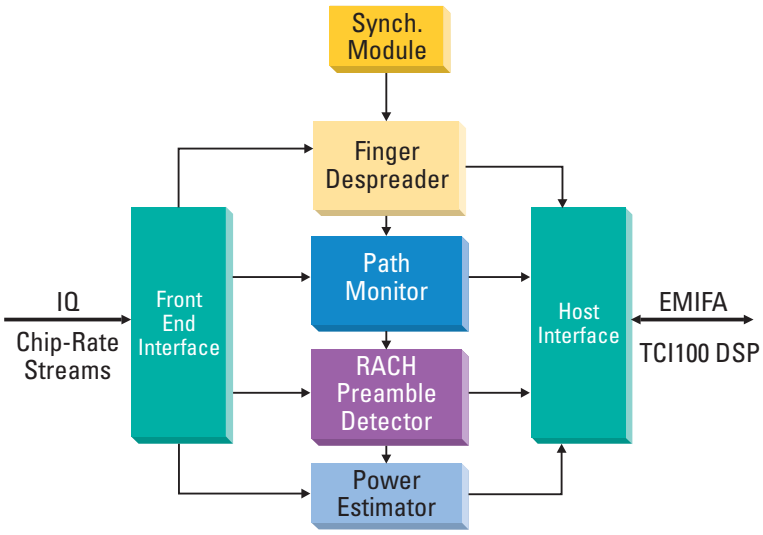

Figure 2: Block diagram of the TCI110 ASSP

- **Front end interface (FEI)** – supports up to 12 antennae and up to 24 input sample streams. This allows for delayed sample streams from the same antenna that may be used for non-causal algorithms for channel estimation and transport format combination indicator decoding. The FEI's main functionality is to distribute the input streams to the different functional blocks of the TCI110 ASSP, including the finger de-spreader, path monitor, preamble detector and power estimator. The FEI also interpolates or decimates input streams to the appropriate sample rate required by these functional blocks.
- **Finger de-spreader (FD)** – carries out symbol de-spreading for the dedicated control channels (DPCCH), dedicated data channels (DPDCH), physical random access channel (PRACH) and physical common packet channel (PCPCH) messages. It also carries out the early, on-time and late correlations on the DPCCH.
- **Path monitor (PM)** – supports search operations on the DPCCH and the control part of PRACH and PCPCH messages that are required to estimate the delay profile of each UE. The PM transfers all correlation results to the CRA DSP. Based on these results, the CRA DSP allocates rake fingers on the FD.
- **Preamble detector (PD)** – supports the detection of preambles on the common uplink physical channels, PRACH and PCPCH (access and CD preambles). Within a configurable search window, the PD stores the 16 largest detection results and the associated offsets for each of the 16 signatures. Based on these results, the CRA DSP determines if a preamble is present, acknowledges its detection and programs the FD accordingly.
- **Host interface (HI)** – is an efficient, high-bandwidth interface between the TCI110 ASSP and the CRA DSP. The interface communicates to the DSP via the 64-bit EMIFA bus. The interface consists of a host interrupt interface (HII) that prepares the correlator outputs for transfer to the CRA DSP. Once the HII programs the EDMA controller of the CRA DSP and groups the user data

TCI120 ASSP Block Diagram

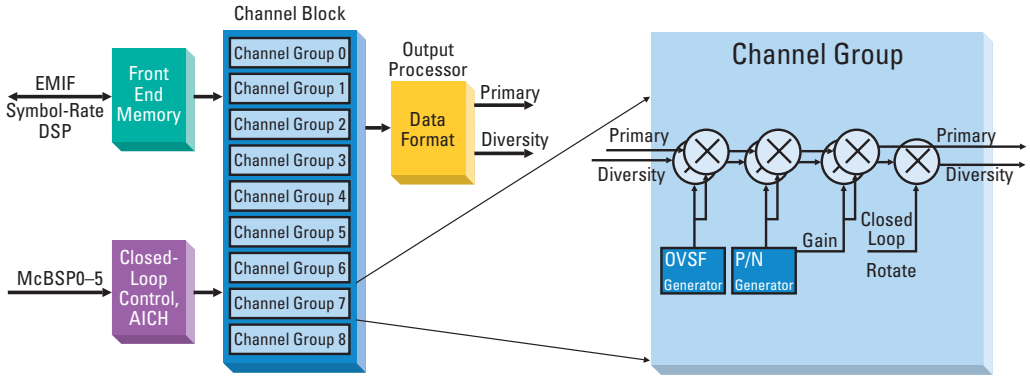

Figure 3: Block diagram of the TCI120 ASSP and the Channel Group

for transfer, the host transfer interface transfers the data over the EMIF bus. Grouping the symbols of all the fingers of a particular user and transferring data to the DSP on a slot-by-slot basis reduces the DSP CPU interrupt rate significantly, decreases the DSP CPU processing overhead and leads to a higher channel density solution.

TCI120 Transmit Chip-Rate ASSP

The TCI120 ASSP, in conjunction with a TCI100 DSP, implements the 3G Partnership Project frequency division duplex (3GPP FDD) Node B downlink physical layer functionality. It also supports high-speed data packet access (HSDPA) channels based on Release 5 of the 3GPP FDD standard. The TCI120 device performs chip-rate processing including channelization and scrambling as well as downlink functions such as power control and diversity processing. The TCI100 DSP that interfaces to the TCI120 device performs downlink symbol-rate processing and configures the TCI120 ASSP. The TCI120 device is highly flexible, programmable and supports variable-rate voice and data users supporting up to 288 simultaneous channels. The TCI120 ASSP also supports open-loop transmit diversity and closed-loop transmit diversity, Mode 1 for both Release 99 and Release 5 channels.

The main functional blocks of the TCI120 ASSP include:

- **Input interface** – The transmit symbol rate (TSR) DSP writes both control and user data to the external memory on a frame-by-frame basis via the EMIF. The TSR DSP then initiates a direct memory access transfer to write the control and user data to the TCI120 ASSP from the external memory on a slot-by-slot basis.
- **Closed loop interface** – The CRA DSP forms the closed loop interface with the TCI120 coprocessor via the McBSP. The CRA DSP provides closed-loop power control, closed-loop transmit diversity and acquisition indicator channel (AICH) information via this interface. The TCI120 ASSP provides six McBSP interfaces to support the closed-loop interface with six CRA DSPs.
- **Channel block (CB)** – consists of nine channel groups that can be configured to support up to 32 channels. The individual channels within the channel group can be configured as either dedicated channels of any spreading factor or as common channels. For HSDPA, the TCI120 ASSP supports both quaternary phase-shift keying (QPSK), 16-quadrature amplitude (16-QAM) modulation and supports up to 15 HS-PDSCH codes per sector and 15 HS-SCCH sets per sector.
- **Output interface (OI)** – supports two output chip-rate streams, one for the primary antenna and the other for the diversity antenna. Each 16-bit complex antenna stream consists of a time division multiplexed bus containing multiplexed 16-bit I and Q words for three sectors or carriers. The I and Q words for a sector are formed by summing the I and Q outputs of all the channel groups allocated to that sector. Each IQ antenna stream seamlessly interfaces to one TI GC5016 digital up/downconverter. A single GC5016 device supports pulse-shape filtering, interpolation and digital up-conversion for the three sectors.

UMTS Chipset Software

UMTS chipset software completes TI's UMTS digital baseband solution. The comprehensive software package includes the TCI100 foundation software, modular applications libraries and TCI1x development tools.

TCI100 Foundation Software

The TCI100 foundation software includes software modules required

to design channel cards based on the TCI1x UMTS chipset.

- **TCI110 Device Control Software** – provides numerous APIs to transfer resource allocation and update requests to the TCI110 ASSP from the DSP user application code.
- **TCI110 Resource Manager** – abstracts the TCI110 implementation details from the user's chip-rate application code and monitors resources on the TCI110 ASSP.
- **TCI120 Device Control Software** – designed to configure the TCI120 ASSP and to transfer user data to the ASSP.
- **Modular Applications Libraries –** TCI1x UMTS Software Design Kit includes transmit and receive symbol-rate software, receive chip-rate software, physical layer services manager and physical layer reference design software.

TCI1x Development Tools

The TCI1x development tools include the TCI1x evaluation module (EVM) and the TCI1x development tools plug-ins.

- **TCI1x UMTS Chipset EVM** – implements a standalone, 3GPP FDD-compliant modem based on the UMTS infrastructure chipset. The EVM can be used to evaluate the ASSPs and software offering and assess their performance. Along with development tools, the EVM also facilitates early software development.
- **TCI1x Development Tools Plug-In** – include Code Composer Studio™ plug-ins. The plug-ins include the TCI110 emulator probe and the TCI120 emulator probe. These emulator probes provide real-time diagnostic visibility into the devices, thereby providing debugging capabilities during software development.

For More Information

The UTMS chipset from Texas Instruments provides a complete solution for wireless infrastructure designers to get low-cost, high-density 3G channel card designs to market quickly. To learn more, call your local TI field sales office, or visit

www.ti.com/tci1xpb_wi

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Americas

Phone	+1(972) 644-5580
Fax	+1(972) 927-6377
Internet/Email	support.ti.com/sc/pic/americas.htm

Europe, Middle East, and Africa

Phone	
Belgium (English)	+32 (0) 27 45 55 32
Finland (English)	+358 (0) 9 25173948
France	+33 (0) 1 30 70 11 64
Germany	+49 (0) 8161 80 33 11
Israel (English)	1800 949 0107
Italy	800 79 11 37
Netherlands (English)	+31 (0) 546 87 95 45
Spain	+34 902 35 40 28
Sweden (English)	+46 (0) 8587 555 22
United Kingdom	+44 (0) 1604 66 33 99
Fax	+(49) (0) 8161 80 2045
Email	epic@ti.com
Internet	support.ti.com/sc/pic/euro.htm

Japan

Fax	International	+81-3-3344-5317
	Domestic	0120-81-0036
Internet/Email	International	support.ti.com/sc/pic/japan.htm
	Domestic	www.tij.co.jp/pic

Asia

Phone	
International	+886-2-23786800
Domestic	Toll-Free Number
Australia	1-800-999-084
China	108-00-886-0015
Hong Kong	800-96-5941
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Thailand	001-800-886-0010
Fax	886-2-2378-6808
Email	tiasia@ti.com
Internet	support.ti.com/sc/pic/asia.htm

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