TMS320TCI6612/14
High performance comes to small cell base stations

Texas Instruments

Product bulletin

Traffic on wireless networks is increasingly data-centric. As wireless data rates increase with high-speed 3G now, and even faster 4G services coming online, the ability to efficiently handle the large volume of data flowing through base stations becomes critically important. With the right silicon technology and design, base stations can handle the immense amount of network traffic 4G demands. Operators are moving to heterogeneous networks that overlay macro- and small-cell solutions to deliver enhanced user experiences. Multiple input, multiple output (MIMO) antenna arrays and advanced receivers are key elements of the new wireless standards that increase the bandwidth of the network. Leveraging the ideal processing element for small cell base stations enables developers to deliver the data bandwidth needed at the speeds customers demand.

The TMS320TCI6612 and TMS320TCI6614 are new wireless base station system-on-chips (SoCs) that deliver the industry's highest performing small cell base station solutions with simultaneous dual mode 3G and 4G. The TCI6612 and TCI6614 are ideally suited to the data-centric performance that wireless network operators are demanding today for 4G small cell base stations. The multiple TMS320C66x DSP cores – 2 cores in the TCI6612 and 4 cores in the TCI6614 -- provide programmable performance while new hardware accelerators focus on bit rate processing to allow base station manufacturers to deliver up to 40 percent more spectral efficiency over conventional decoding techniques. Control processing is performed by an integral ARM RISC core in each SoC that enables developers to design low power, high performance solutions for small cell base stations.

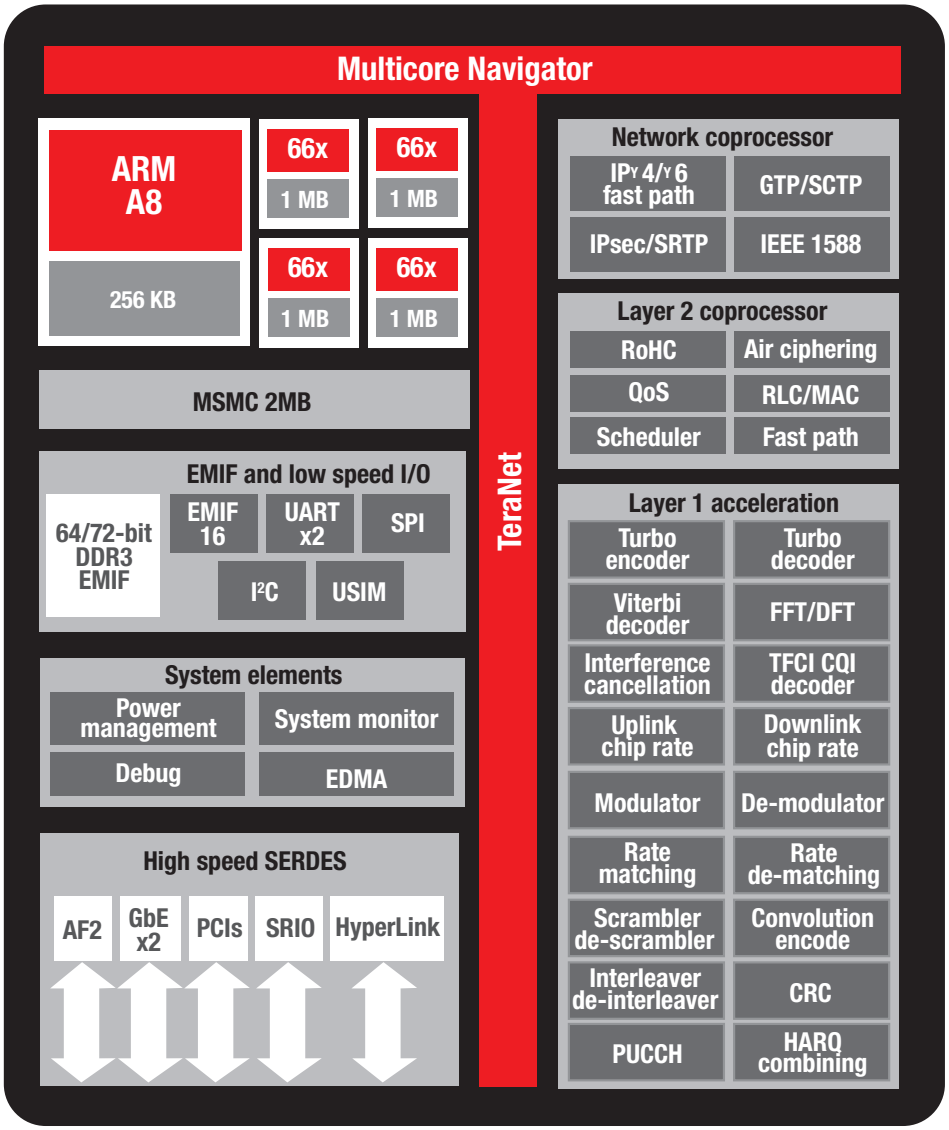
The TCI6612 and TCI6614 SoCs are based on TI's scalable KeyStone multicore architecture. They feature a mix of processing elements including radio accelerators, network and security coprocessors, fixed- and floating-point capable digital signal processor (DSP) cores and an ARM RISC processor, providing the ideal processing element for all aspects of high performance small cell base stations. Multicore Navigator, a queue-based packet structure, coupled with TI's Open Navigator programming interface, gives designers the ability to easily add differentiating, value-added features. In addition, TI has integrated a digital radio into their SoCs, lowering the costs as well as easing the integration and design of small cell base stations.

With both floating- and fixed-point processing on each DSP core, the TCI6612 and TCI6614 enable base station designers to take advantage of rapid algorithm prototyping and quick software redesigns, reducing costs and development time. Because the C66x cores are so powerful, significantly fewer cores are needed to provide four times the processing power of previous generations of DSPs. Designers will enjoy simplified programming with fewer cores, along with increased performance

The integration of the ARM RISC core greatly reduces system cost. The ARM Cortex-A8 core enables developers to design low power, high performance solutions supporting more users on data-centric applications and bringing a new level of power efficiency and integration to base station developers. The Cortex-A8 coupled with the incorporation of packet and security processors eliminate the need for an external network processors.

Key features

- Simultaneous, dual mode wireless base station system-on-chip (SoC) that delivers unmatched high performance for small cell form factors
- Highest performing multicore small cell base station system-on-chip (SoC on the market today, delivering unmatched throughput and lowest latency for simultaneous multi-standard wireless base stations
- Bit coprocessor increases SoC system performance and enables advanced receiver algorithms to achieve improved spectral efficiency by up to 40 percent over conventional decoding techniques
- TI's new C66x DSP combines floating and fixed point on the same core, delivering floating-point performance at fixed-point speeds for the first time
- KeyStone SoC with an integral ARM® Cortex-A8 processor for control plane processing
- Only solution to feature coprocessors for every standard, including WCDMA chip rate – no FPGA/ASIC required
- Network coprocessor and Multicore Navigator combine to provide Layer 2 and transport acceleration for all wireless base station standards
- Based on TI's new KeyStone architecture, enabling scalability and portability from macro to small cells reducing product development expense
- Multicore Navigator brings single-core simplicity to multicore SoCs
- Best power/performance ratio, coupled with unique power-saving hibernation modes, delivers the lowest power for base stations
- Leverages high-performance 40-nm process technology



▲ *TCI6614 block diagram*

Designers benefit from the TCI6612/14's software compatibility with the previously announced TCI6616 and TCI6618 wireless base station SoCs to design multimode base stations that support all 2G, 3G, and 4G standards. OEMs can simplify the migration to 4G with this flexibility, and it allows base station OEMs to develop a wider portfolio of solutions at a lower cost and in a shorter time than with competing solutions. The TCI6612 and TCI6614 are pin compatible allowing manufacturers to offer tailored solutions from a single hardware design.

TCI6612/TCI6614 high-performance solution for small cell base stations

Designed specifically for small cell wireless infrastructure baseband applications, the TCI6612 and TCI6614 SoCs are ideal solutions for small cell base stations. These SoCs also enable baseband solutions for GSM, CDMA, WCDMA, TD-SCDMA, WiMAX, FDD-LTE, and TDD-LTE applications. To make the transition from C6000™ DSPs easier, the TCI6612 and TCI6614 are backward code-compatible, allowing software reuse and maintaining value-added designs and IP. In addition, TI's TCI6612 and TCI6614 leverage the KeyStone architecture for scalability to meet the need of all base stations, from single-sector small cells to multi-sector macro cells. With one software base driving a variety of base station products, developers will realize the highest R&D efficiency possible as well as optimized product costs.

The TCI6612 and TCI6614 are based on 40-nm process technology and deliver up to 4.8 GHz of raw DSP processing power, as well as performance of up to 153.6 16-bit GMACs per second, making either device a cost-effective solution for high-performance DSP programming challenges. Due to its floating-point capability, the TCI6612 and TCI6614 offer performance of up to 76.8 billion floating-point operations per second (GFLOPs), making these SoCs the industry's most powerful floating- and fixed-point SoCs. Because the TCI6612 and TCI6614 incorporate both fixed- and floating-point capabilities on the same core, they can perform up to five times faster than a fixed-point implementation alone. In addition, the development and debugging cycle time for complex algorithms is significantly reduced from a multiple-month cycle to just a few days. The TCI6612 integrates two C66x DSP cores while the TCI6614 offers four C66x DSP cores for larger small cell base station designs.

The TCI6612 and TCI6614 integrate large on-chip memory organized as a two-level memory system that minimizes latency and increases system performance. The level-1 (L1) program and data memories on the devices are 32KB each per core. The level-2 (L2) memory is shared between program and data space for a total of 4,096KB (1,024KB per core). They contain 2,048KB of multi-core shared memory (MSM) that is used as a shared L2 SRAM or shared L3 SRAM. A dedicated Multicore Shared Memory Controller (MSMC) prevents memory contention between the cores and arbitrates access to the shared memory between the cores and other IP blocks.

The TCI6612 and TCI6614 have a high-performance peripheral set with everything needed to develop robust base stations of varying coverage and capacity, including:

- I²C, SPI, and UART
- PCI Express port with two lanes supporting GEN1 and GEN2
- Twelve 64-bit general-purpose timers (also configurable as sixteen 32-bit timers)
- 32-pin general-purpose input/output (GPIO) port with programmable interrupt/event generation mode
- Multicore Navigator for hardware-accelerated dispatch
- Four lanes of serial RapidIO® (SRIO), compliant with RapidIO 2.1 spec for up to 5-Gbps operation per lane
- 64-bit DDR3 SDRAM interface
- 16-bit external memory interface (EMIF) for connecting to flash memory (NAND and NOR) and asynchronous SRAM
- Second-generation SERDES-based antenna interface (AIF2) capable of up to 6.144 Gbps operation per link with six high-speed serial links, compliant to OBSAI RP3 and CPRI standards

For efficient communications between the device and the network, the TCI6612 and TCI6614 include a network coprocessor that consists of:

- Two 10/100/1000 Ethernet media access controllers (EMACs), which provide an efficient interface between the DSP core processors and the core network
- Management data input/output (MDIO) module (also part of the EMAC) that continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system
- Packet coprocessor that provides L2 to L4 classification functionalities and the processing power of up to 1.5 Gbps
- Security accelerator block capable of wire-speed processing on 1-Gbps Ethernet traffic on IPSec, SRTP, and 3GPP air interface security protocols
- Embedded Ethernet switch that allows multiple devices to be connected through SGMII, eliminating the need for a board level Ethernet switch

The TCI6612's and TCI6614's high-performance embedded coprocessors perform intensive signal processing functions common to wireless base station applications. The result is increased overall system performance, yielding 40 percent spectral efficiency over conventional decoding techniques.

Bit Rate Coprocessor for increased spectral efficiency

The bit rate coprocessor (BCP) is a multistandard acceleration engine that offloads all bit rate processing in the wireless signal chain without the need to involve the DSP core at any step once the BCP is engaged. The BCP contains the modulator, demodulator, interleaver/de-interleaver, turbo and convolution encoding, rate matcher/rate de-matcher, correlator for block code decoding, and CRC engine. The BCP enables turbo interference cancellation for MIMO equalization and enables high-performance PUCCH format 2 decoding. It offloads approximately 15 GHz of CPU MIPS. These techniques, coupled with the powerful MIMO processing capabilities of TI's new DSP C66x cores, yield an SoC that delivers on the promise of 4G for operators and users alike.

Faster coprocessors for optimized base station designs

Since 2001, TI has delivered radio coprocessing functions that consist of configurable hardware accelerators to offload processing demands as well as increase overall system performance. TI's coprocessors also reduce base station power requirements and dissipation as well as board complexity, making new products easier to design, build, and deploy.

Coprocessor	Total performance (@1.2-GHz core frequency)
FFT/DFT	MSPS @ 256-FFT MSPS @ 192-DFT
Turbo decode	LTE – Mbps @ 6144 block size, 6 iterations WCDMA – Mbps @ 5114 block size
Turbo encode	LTE/WCDMA 1.6 Gbps
Viterbi decoder	>38 Mbps (K = 9) Mbps
Rake Search Accelerator	32-bit multiplication per cycle
WCDMA despreading	256 AMR users supported @ eight fingers
WCDMA spreading	256 users supported with two radio links and diversity 1.5 packet @ 1 Gbps
Network Coprocessor	2.8 Gbps
BCP	LTE – DL 2.2 Gbps, UL 1.1 Gbps WCDMA – DL: 800 Mbps, UL 400 Mbps

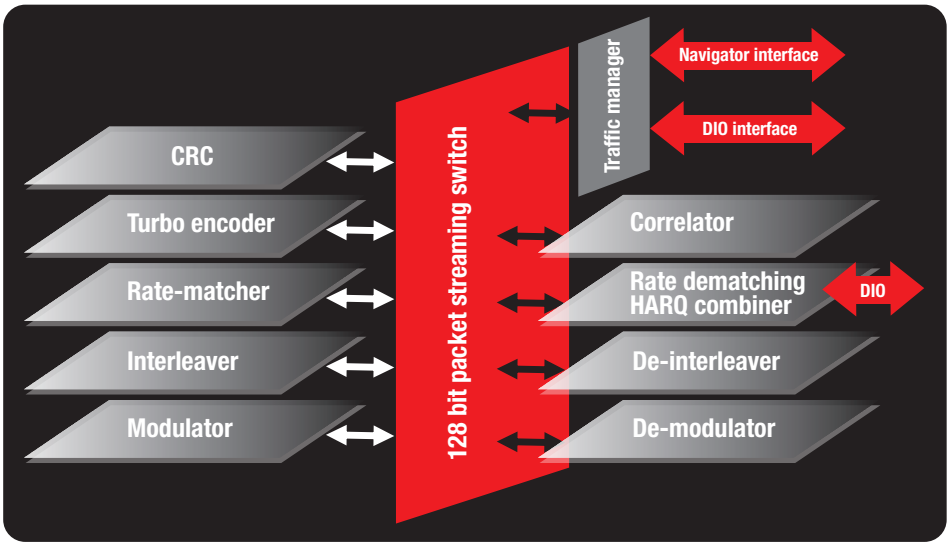
▲ *Coprocessors for TCI6612 and TCI6614*

As wireless radio standards evolve and related implementations become standardized, each evolution of TI's wireless SoCs includes additional coprocessing, providing a compelling path to lower power and costs while enabling higher performing base station solutions from our customers. TI's SoC strategy of integrating DSP and ARM cores with coprocessors is the most efficient and most economical approach to wireless base station SoC design and continues to be the market-leading solution. TI's coprocessors eliminate external FPGAs and ASICs that were previously needed to deliver the performance demanded of 3G and 4G base stations.

The TCI6612 and TCI6614 have multiple, dedicated high-performance embedded coprocessors to perform intensive signal processing functions common to wireless base station applications. The coprocessors are; four enhanced Viterbi decoder coprocessors (VCP2_A, VCP2_B, VCP2_C, and VCP2_D), three third-generation turbo decoder coprocessors (TCP3d_A, TCP3d_B, and TCP3d_C), turbo encoder coprocessor (TCP3e), three fast Fourier transform coprocessors (FFTC_A, FFTC_B, and FFTC_C) and a bit rate coprocessor. Together, they significantly accelerate channel encoding/decoding operations. Also included in the SoCs are four tightly coupled rake/search accelerators (RSAs) for code division multiple access (CDMA) assistance with chip-rate processing.

Delivering full multicore entitlement

The TCI6612 and TCI6614 SoCs are based on TI's KeyStone multicore architecture. KeyStone is the first of its kind to provide full multicore



▲ *BCP architecture*

entitlement. This provides non-blocking access to all processing cores, peripherals, coprocessors, and I/Os. Innovations that unleash full multicore entitlement are: Multicore Navigator, TeraNet, Multicore Shared Memory Controller (MSMC), and HyperLink.

Multicore Navigator – TI's Multicore Navigator is an innovative packet-based manager that controls and abstracts the connections between the various subsystems on the SoCs. With a unified interface for communication, data transfer, and job management, Multicore Navigator enables higher system performance with fewer interrupts and reduced software complexity with a "fire and forget" paradigm. Benefits of Mutlicore Navigator include:

- Dynamic resource/load sharing
- Offloading CPU overhead/delay related to inter-subsystem communications
- Hardware-based task prioritization
- Dynamic load balancing
- Common communication methodology for all IP blocks (software, I/O, and accelerators)

TeraNet – TeraNet is a hierarchal switch fabric that combines to deliver more than two terabits of bandwidth for data transfer within the SoC. This virtually guarantees that the cores or coprocessors are never starved for data and can deliver the entitled processing horsepower. Because the switch fabric is hierarchical instead of a flat crossbar, overall power consumption is much lower in idle states and systems latency is minimized. Low latency is a key requirement of next-generation base stations.

Multicore Shared Memory Controller (MSMC) – TI's TCI6612 and TCI6614 include unique memory architecture for enhanced performance. TI's Multicore Shared Memory Controller (MSMC) allows the cores to directly access shared memory without having to use any TeraNet bandwidth. The MSMC arbitrates access to shared memory between the cores and other IP blocks, eliminating memory contention. Shared memory access for code is nearly identical in latency to local L2 access, with highly effective prefetch mechanisms for code and data.

TI's TCI6612/TCI6614's DDR3 external memory interface (EMIF) is a 1,600-MHz, 64-bit bus with 8 GB of addressable memory space. Tied directly to the MSMC, the DDR3 EMIF reduces latency associated with external memory fetches and provides the speed increase and support needed for larger applications that operate on large amounts of data, which is essential for advanced 3G and 4G base stations.

HyperLink – HyperLink, with four lanes at up to 12.5 Gbaud/lane, is a proprietary high-speed interconnect that allows low protocol and high-speed communication and connectivity to other KeyStone devices providing OEMs a seamless path to scalable solutions. The HyperLink on the TCI6612 and TCI6614 works in conjunction with the Multicore Navigator to dispatch tasks to multiple devices transparently, so they execute as if they are running on local resources.

TCI6612/TCI6614 as Layer 2 and transport processing engine

The TCI6612/TCI6614 combines unmatched PHY processing capabilities with dedicated coprocessors for Layer 2 and transport layer processing. This enables designers to create base stations without a separate network processor thereby reducing board complexity and cost without compromising performance.

The network coprocessor enables fast-path processing in the transport network layer and deep into the Layer 2 of the radio network. Within the SoC's network coprocessor, the Packet Accelerator and the Security Accelerator perform fully-accelerated autonomous packet-to-packet processing. They leverage the Multicore Navigator, which uses a zero-copy method to optimize data processing at all layers. Classification and ordering, multicore-accessible storage, memory management, segmentations and reassembly, and delivery across multiple cores and devices are all supported by the network coprocessor. Layer 2 data-plane and transport plane overhead can be reduced by 10-15 times due to the fast-path and zero-copy processing.

Lowest power consumption for performance

TI has a history of providing the lowest power wireless base station SoCs on the market. TI is able to achieve its ultimate low power through the combination of its process technology, SmartReflex™ technology, and the proactive use of power management techniques (such as adaptive voltage scaling) in every wireless base station semiconductor device to keep active power to a minimum. TI's latest technology in the TCI6612/TCI6614 has brought the SoC power consumption for small cell base stations down to the industry's lowest levels at 26 mW of power per Mbps of data transferred.

Complete tools and support

TI provides a full suite of best-in-class Eclipse-based development and debugging tools with the TCI6612 and TCI6614. These include a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows debugger interface for visibility into source-code execution. TI's compiler generates highly efficient code that is "first-pass efficient" so there is less need to optimize it. TI's debugging tools help developers visualize problems and resolve them quickly, so designers can get products to the field faster while saving development resources. In addition, TI will offer an evaluation module (EVM) to help customers prototype quickly. All of these tools integrate the ARM RISC processor as well, enabling designers to quickly and efficiently develop code for all subsystems of the SoCs.

For more information

To learn more about the TCI6612 and TCI6614 SoCs visit **www.ti.com/c66multicore**. Discover how the TCI6612 and TCI6614 can add performance to your next small cell base station design.

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