TCI6631K2L SoC

High performance, low power solution for Non Line of Sight (NLOS) wireless backhaul

Texas Instruments

Based on TI's high-throughput KeyStone™ II architecture, the new TCI6631K2L system-on-chip (SoC) is a scalable low-power baseband solution with an integrated digital radio front end (DRFE) that meets the more stringent power, size and bill of materials (BOM) cost requirements of wireless backhaul. The device's dual-ARM®/quad-DSP cores deliver the processing power that TI's wireless infrastructure solutions are known for and combine this with design innovations that pinpoint the specific set of requirements for NLOS backhaul.

Cost-effective and operationally efficient indoor and outdoor wireless NLOS backhaul solution will be a key service delivery layer for the expanding role of small cells in the carrier infrastructure. Small cell base stations need to be installed in specific locations to fill in the cellular coverage, which is rarely where there is easy access to the network infrastructure. The simplest and most cost-effective solution is to install a Point-to-Point (PtP) or Point-to-Multi-Point (PtMP) NLOS wireless backhaul solution to connect the network to one or more small cell base stations located nearly anywhere.

Scalable high-performance wireless backhaul

The TCI6631K2L SoC applies the technology breakthroughs achieved by the previous generations of TI's wireless infrastructure SoCs and scales them to the special set of requirements common for most wireless communication solutions. At the same time, the KeyStone II architecture gives the TCI6631K2L SoC a high degree of scalability within the range of NLOS backhaul use cases. The KeyStone II architecture affords the device a powerful framework that ensures the responsiveness that wireless users expect and which they will demand for years to come. The scalability, flexibility and versatility of the KeyStone II architecture lends itself to higher levels of integration and system design innovations.

A critical aspect of the scalability of the TCI6631K2L SoC is the consistent and continuous software track that is essential to all of TI's base station SoCs. In addition to the hardware compatibilities of the KeyStone II architecture, software developed for any KeyStone-based device is scalable upward or downward to other KeyStone SoCs, which include SoCs that support metro and micro base stations. As a result, system providers can reduce software development costs considerably by re-using code across multiple infrastructure systems that target the various segments of the marketplace.

Integrated digital radio front end

To date, backhaul architectures have mostly featured FPGA implementations of the DRFE, which has often been deployed in multiple discrete devices or even in an enclosure separate from the baseband processing block. Moving forward, designs will require compact low-power enclosures with no active cooling. Simpler board designs with greater integration of components will be needed to achieve both

Key Features

- Highly flexible and scalable NLOS backhaul solution
- Low power – Meets Power over Ethernet Plus (PoE+) budget in many applications
- Complete System on a Chip (SoC) for layer 1, 2, and 3 protocol support
- Full suite of wireless PHY and Digital Radio Front End (DRFE) accelerators required for most wireless protocols
  - Significantly reducing the processor loading
  - Full support for Digital up/down conversion (DDUC), QAM-256, encoding/decoding modulation
  - Crest Factor Reduction (CFR), Digital Pre-Distortion (DPD) to allow more efficient and cost-effective power amplifiers
- Targeted to meet the needs of a wide range of wireless backhaul applications
- Six general purpose processing cores to support a wide range of Software Defined Radio (SDR) solutions
  - Two ARM® Cortex®-A15 RISC cores
  - Four TMS320C66x DSP cores with fixed- and floating-point processing
- KeyStone II architecture with extremely high throughput speeds optimizes processing cores
- High-speed JESD204B chip-to-chip interface optimizes board layout (fewer lanes, fewer pins) and reduces power consumption
- Advanced integrated network coprocessor offloads ARM/DSP cores, allowing greater system differentiation
- Highly integrated into one device to reduce BOM costs, system size and power consumption

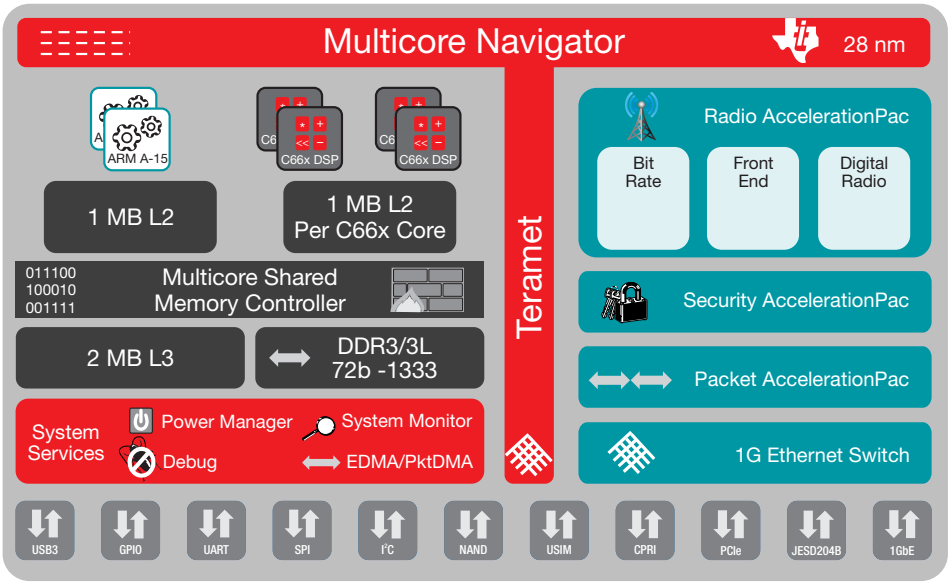
the lower capital expenditure (capex) and operational expenditure (opex) goals dictated by the introduction of many new yet smaller sites into networks long dominated by macro-size cell towers.

In response to these requirements, the TCI6631K2L SoC is the first wireless backhaul infrastructure SoC to integrate the functionality of a DRFE on chip. By taking this approach, as well as by developing additional innovations involving a new more efficient chip-to-chip interface, advanced co-processor capabilities and others, the TCI6631K2L SoC is able to meet the low power, lower cost and simpler design requirements of wireless backhaul.

By integrating the DRFE, the TCI6631K2L SoC combines all the high-throughput digital processing into one optimized processing unit, including control, baseband and DRFE. As a result, the SoC is able to perform a variety of functions on chip, such as the fundamental signal-processing functions like channelization and re-sampling, as well as channel aggregation and distribution, which are essential to heterogeneous networks.

Combining many of the DRFE functions with the baseband processing allows for the data conversion and RF up/down conversion processing to be integrated into another radio SoC that is fabricated with a process node more compatible with performance analog and RF operations. In addition, the DRFE capabilities on the TCI6631K2L SoC have been augmented with advanced analog/RF impairment correction algorithms that can interface with analog radio processing and improve the efficiencies and cost effectiveness of the particular power amplifier (PA) deployed in a wireless backhaul design. The two most RF-critical impairment correction algorithms are crest factor reduction (CFR) and digital pre-distortion (DPD).

- **Crest Factor Reduction (CFR)**
  CFR is a signal-processing algorithm that affects a signal's peak-to-average ratio (PAR). Since selection of the system's PA must accommodate the greatest PAR expected, reducing the PAR can decrease the size and improve the power efficiency of the system's PA by as much as 400 percent, reducing the overall power consumption of the system and the cost of the PA significantly. The CFR algorithm reduces the PAR by introducing noise into the signals within certain limits. The TCI6631K2L SoC's CFR module includes advanced features like multiple stages of peak cancellation with provisions to estimate fractional peaks and limit over cancellation, automatic estimation of the CFR cancellation pulse shapes based on signal spectral content monitoring, dynamic threshold adjustments and automatic gain control loops.



▲ *KeyStone II-based TCI6631K2L SoC*

- **Digital Pre-Distortion (DPD)**
  DPD is a way to coax more linear performance from the system's PA. The power efficiency of PAs decrease or drift away from an ideal linear performance line as the device approaches its peak drive point (also known as its saturation point). When the PA is not operating efficiently, it wastes power – increasing the overall power consumption of the system – and generates excessive heat, which in turn complicates the thermal management issues for the system designer. DPD allows the PA to operate more efficiently longer along a more linear performance path as it approaches its peak drive point. This opens up a wider array of PAs for the system designer to choose from, including more cost-effective devices which reduce the system's BOM. At the same time, more than adequate margin is provided for system performance.

Simplifying designs

The sheer number of sites needed in a seamless heterogeneous network will necessitate simple, very cost-effective system designs. In addition to greater integration at the silicon level, circuit board design and layout can be simplified to reduce BOM and board production costs. A new serial communications link interface, which conforms to the JESD204B standard from JEDEC, achieves this simplification.

JESD204B provides for a high-throughput, low-pin-count serial link between analog-to-digital (ADC) and digital-to-analog (DAC) converters, and on-board logic devices such as field programmable gate arrays (FPGA), digital signal processors (DSPs), SoCs, application-specific integrated circuits (ASIC) and others. By embedding the clock in the data stream and including certain embedded algorithms to optimize the sampling of data bits, JESD204B is able to simplify routing between devices because significantly fewer lanes are needed on the board. To achieve the same throughput as JESD204B, for example, the more prominent SerDes interfaces, such as PCI Express (PCIe) and the Common Public Radio Interface (CPRI), would require more lanes on the board. This reduces the number of input/output (I/O) channels on devices, reducing pin counts and enabling smaller packages. In addition to simplifying system design, JESD204B shortens circuit board bring-up by reducing the setup/hold times that are usually performed across the many more lanes typically employed by other SerDes interfaces like PCIe and CPRI that are based on low-voltage differential signaling (LVDS) pairs. JESD204B is a flexible and scalable serial link interface that can accommodate a wide range of data transfer speeds and configurations, such as multiple ADCs or DACs on one JESD differential pair.

Other capabilities of the TCI6631K2L SoC that can have a profound effect on simplifying designs are the coprocessors which can offload much of the processing load from the ARM and DSP cores, or eliminate the need for additional external processors without increasing the complexity of the system. For example, adding a discrete network processor to the system would mean adding the device itself as well as its associated memory, clock and power management functionality.

The TCI6631K2L SoC's integrated Network Coprocessor (NCP) can perform all of the transport network termination, and packet and security processing of a traditional network processor as well as all operations and management functions. The NCP includes a packet accelerator as well as extensive security accelerators supporting both the IPSec encryption algorithm for wireline connections and various wireless protocol encryption packages. Additionally, the TCI6631K2L SoC's NCP has been enhanced with the integration of an Ethernet switching element on-chip, eliminating the need for an external and costly switching device.

High-performance wireless physical layer accelerators

The TCI6631K2L SoC includes the high-performance radio accelerators which simplify the wireless physical layer (PHY) implementation and off-load the routine processing tasks from the DSP cores. Integrated with the SoC are two FFT coprocessors needed for OFDM support, two Turbo-encoders (TCP) essential for high-efficiency modulation, four Viterbi decoders (VCP) for demodulation and bit-rate co-processors (BCP) for bit-stream encoding and rate matching.

These accelerators have set the standard for high-performance PHY drivers for standard WiMax (802.16), SmartGrid (802.15.4) and WiFar (802.22) drivers as well as many proprietary backhaul PHY solutions; providing the optimal level of acceleration for custom SDR PHY solutions with minimal load to the core processors.

Enabling low-power solutions

Various aspects of the TCI6631K2L SoC not only make it a low-power device, but its various capabilities such as the integrated DRFE reduce the overall power consumption of the entire system. As a result, single-carrier dual-band system configurations based on the TCI6631K2L SoC will meet the power budget of Power over Ethernet Plus (PoE+), an important consideration in some use cases such as enterprise applications where an access point may be deployed inside a building and connected to the facility's Ethernet network. With PoE, the base station can be powered by and have wide area access to the Internet via one Ethernet cable, simplifying deployment and installation issues.

At the same time, the TCI6631K2L SoC is a scalable solution, capable of supporting architectures beyond single-carrier systems. In fact, the advanced features of the TCI6631K2L SoC will support channel aggregation where channels are combined in the same bandwidth to increase throughput and maximize efficiency.

The TCI6631K2L SoC is the latest in TI's long line of the industry's lowest-power wireless base station and infrastructure SoCs.

Similar to the devices before it, the TCI6631K2L SoC has achieved its exceedingly low power consumption through a combination of process technologies, TI's SmartReflex™ low-power technology and innovative power management techniques, such as dynamic voltage, frequency scaling, memory retention until access, power and clock gating, and others.

Scalable solutions based on the KeyStone II architecture

The KeyStone II architecture on which the TCI6631K2L SoC is based affords the SoC considerable scalability and flexibility within the device itself, but sharing the same base architecture with other communications infrastructure SoCs enables scalability beyond the TCI6631K2L SoC to larger, more powerful SoCs such as the TCI6636 SoC for metro and micros.

The key objective behind the KeyStone II architecture is to provide more than enough throughput and on-chip resources such that the processing cores will be able to reach their optimum processing performance without constraints. Referred to as multicore "entitlement", this empowering of the processing cores is ensured by the architecture's ability to provide non-blocking access to all processing cores, peripherals, co-processors and I/O channels. Some of the key aspects of the KeyStone architecture are its Multicore Navigator, TeraNet, Multicore Shared Memory Controller and HyperLink.

The **Multicore Navigator** controls and abstracts the connections among the various subsystems that make up the KeyStone architecture and the particular SoC. This innovative packet-based manager has a unified interface for communications, data transfers and job management. While delivering higher system performance, it ensures fewer interrupts and reduces the complexity of software because of its "fire-and-forget" action model.

TeraNet – a hierarchal switch fabric – delivers more than two terabits of data bandwidth within the TCI6631K2L SoC. This virtually guarantees that the cores and coprocessors are never idle because of data communication latencies. As a result, each processing element is able to operate at its optimum rate. Since the TeraNet switch fabric is hierarchical instead of a flat crossbar, overall power consumption is much lower in idle states and systems latency is minimized. Low latency is a key requirement of next-generation base stations, large and small.

With the **Multicore Shared Memory Controller (MSMC)** cores can directly access shared memory without adding traffic to the TeraNet. Instead, MSMC eliminates memory contention by arbitrating accesses to shared memory among the cores and other processing elements. Highly effective pre-fetch mechanisms for code and data make accesses to shared memory nearly the same in latency as accesses to local L2 memory.

The **DDR3 external memory interface (EMIF)** on the TCI6631K2L SoC is made up of one 1,600-MHz, 72-bit bus supporting as much as 8 GB of addressable memory space. With its direct connection to the MSMC, the DDR3 EMIF is able to reduce any latency associated with external memory fetches and provide the speed needed for large data transfers, which is essential for advanced 3G and 4G base stations.

Enabling an extensible and scalable system architecture, the TCI6631K2L SoC has two **HyperLink** interfaces for high-speed communication with other KeyStone devices. Each HyperLink supports a bandwidth of up to 100 Gbps with low protocol overhead. HyperLink functions in conjunction with the Multicore Navigator, dispatching processing tasks to any available device transparently, so that the task executes as if it were running on local resources.

Powerful core performance

The KeyStone II architecture leverages advanced 28-nm technology for improved cost efficiency through the integration of multiple

RISC cores and DSP cores and lower system power consumption.

The two ARM® Cortex®-A15 RISC cores provide high-performance RISC processing at ultra-low power consumption levels. The four TMS320C66x DSP cores integrated into the TCI6631K2L SoC provide programmable performance supported by a variety of co-processors specializing in packet, symbol and bit-rate processing so that base station manufacturers can easily support a mix of protocols in heterogeneous networks.

Because the C66x DSP cores are capable of both fixed- and floating-point computations, each core can perform up to five times faster than a traditional floating-point core. In addition, the development and debugging cycle time for complex algorithms is significantly reduced from a multiple-month cycle to just a few days. The C66x DSP cores include 90 instructions targeted for floating-point and vector-math-oriented processing.

Complete tools and support

TI has developed a range of tools and support capabilities that save base station suppliers time, resources and development budget so that these resources can be allocated to developing differentiating features in their own systems. The availability of a PHY eliminates one of the most complex tasks of base station design. To facilitate seamless integration with a complete PHY which is modular and open so customers can add value within the PHY by incorporating proprietary algorithms that may be critical to product differentiation. As a result of the PHY's flexible design, base station manufacturers can easily customize their products to meet the needs of different network operators.

Other development tools include TI's well-known Code Composer Studio™ (CCStudio) integrated development environment (IDE), a full suite of best-in-class Eclipse-based development and debugging tools. CCStudio IDE features a C compiler, Assembly optimizer to simplify programming and scheduling and a Windows® debugger for visibility into source code execution. The compiler generates highly efficient code that is first-pass efficient, reducing the need to optimize code. The debugging tools help designers get products to market faster while saving development resources by visualizing problems and finding solutions quickly. In addition, an evaluation module (EVM) is available to facilitate rapid development of prototypes. All of these tools integrate with the ARM RISC cores as well so that designers can quickly and efficiently develop code for all subsystems within a single IDE platform.

For more information

To learn more about the TCI6631K2L SoC visit **www.ti.com/multicore**.

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