

DRA75x “Jacinto 6 EP” and “Jacinto 6 Ex” Automotive Applications Processors



Introduction

The DRA75x is a high-performance, infotainment application device family integrated on a 28-nm technology.

Device overview

- TI’s new DRA75x processors, “Jacinto 6 EP” and “Jacinto 6 Ex”, developed on the same architecture as other “Jacinto” devices, enable automotive manufacturers to scale their investment without additional R&D investment or significant bill-of-material (BOM) increase to deliver a diverse portfolio of products with hardware and software compatibility. The devices extend and augment the “Jacinto 6” family in the following ways:
 - “Jacinto 6 EP” – Adds a second TMS320C66x digital signal processor (DSP) core for image manipulation technologies such as dynamically stitching multiple cameras into a single, surround or overhead view; additional radio use-cases (multi-tuner configurations and evolving use-cases); audio and speech processing; active noise control (ANC); voice recognition and a variety of other technologies.
 - “Jacinto 6 Ex” – Further extends performance and integration possibilities from the “Jacinto 6 EP” by offering the TI Vision AccelerationPac including two embedded vision engines (EVEs) enabling simultaneous informational advanced driver assistance systems (ADAS) and infotainment functionalities without compromising the performance of either system.

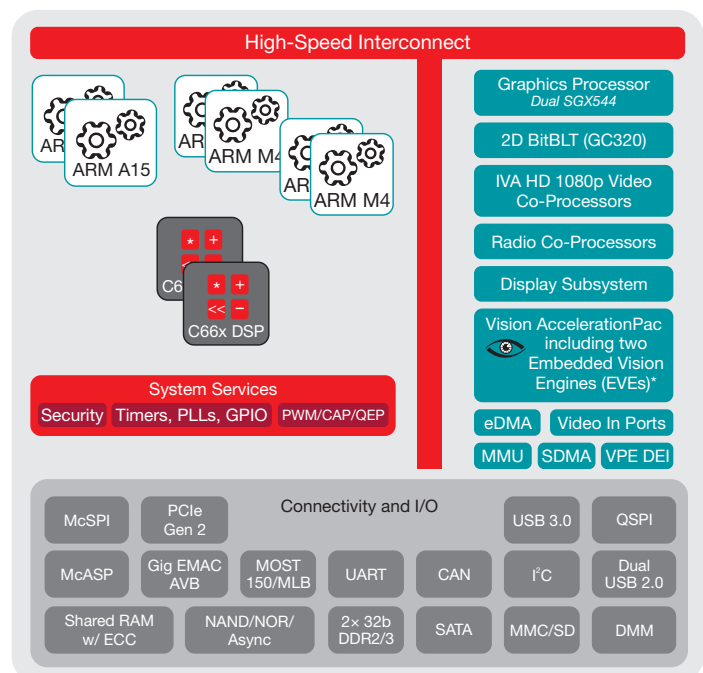
Device features

- The device is composed of the following subsystems
 - Two ARM® Cortex®-A15 microprocessor units (MPUs)
 - Two digital signal processors (DSP C66x subsystem)
 - Image and video accelerator high-definition (IVA-HD) subsystem
 - Two ARM Cortex-M4 processing subsystems, each including two ARM Cortex-M4 microprocessors
 - Vision AccelerationPac including two embedded vision engines (EVEs)*
 - Display subsystem (DSS)
 - Video Processing subsystem (VPE)
 - Video Input Capture (VIP)
 - 3D-graphics processing unit (GPU) subsystem, including Imagination Technologies POWERVR™ SGX544-MPx single-core
 - 2D-graphics accelerator (BB2D) subsystem, including Vivante™ GC320 core
 - Three pulse-width modulation (PWM) subsystem
 - Real-time clock (RTC) subsystem
 - Debug subsystem
- The device provides a rich set of connectivity peripherals including:
 - USB 3.0, USB 2.0
 - SATA 2
 - PCI Express Gen2
 - 3-port Gigabit Ethernet Switch with AVB

- State-of-the-art, integrated power management techniques
- The device also integrates:
 - On-chip memory
 - External memory interfaces
 - Memory management
 - Level 3 (L3) and level 4 (L4) interconnects
 - System peripherals
 - Car, audio and media peripherals including CAN, MOST MLB and Ethernet AVB
 - Radio accelerators

DRA75x description

The DRA75x device is offered in a 760-ball, 23×23-mm, 0.8-mm ball pitch with Via Channel™ Array (VCA) technology, ball grid array (BGA) package. The figure below is the block diagram of the DRA75x device.



▲ DRA75x block diagram

*Vision AccelerationPac for Jacinto 6 Ex only

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