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8:00 A.M.–9:00 A.M. – Keynote: The Super Heroes of the Signal Processing Domain						
<p>9:15 A.M.–10:45 A.M. AACPlus – High-Efficiency Audio Coding for Broadcast and Mobile Applications (S055)</p> <p>11:00 A.M.–12:00 P.M. Low-Delay Audio Coding on TI DSPs (S017)</p> <p>11:00 A.M.–12:00 P.M. High-Quality Audio Processing Using 16-/32-Bit Fixed-Point DSPs (S972)</p>	<p>9:15 A.M.–10:15 A.M. Comparing and Contrasting 3G Long-Term Evolution vs. WiMAX (S590)</p> <p>10:15 A.M.–11:15 A.M. Developing Code for the 3G Mobile Infrastructure and Beyond (S348)</p> <p>10:45 A.M.–11:45 A.M. Reviewing DSP-Based Adaptive Antenna Solutions for WiMAX (S270)</p> <p>11:15 A.M.–12:15 P.M. The IP Multimedia Subsystem: SIP for Carrier Delivery of Global Communications Service (S198)</p>	<p>9:15 A.M.–10:15 A.M. What's New with TMS320C2000™ Digital Signal Controllers? (S797)</p> <p>10:15 A.M.–11:15 A.M. Simplifying Motor Design Through DSP Control Algorithms (S274)</p> <p>11:15 A.M.–12:15 P.M. A Four-Quadrant, Full-Torque at Zero Speed Drive Using a TMS320C2000™ Controller (S001)</p>	<p>9:15 A.M.–10:45 A.M. Getting Started with the TMS320C645x™ DSPs: Overview and Reference Designs (S013)</p> <p>9:15 A.M.–10:45 A.M. Microprocessors vs. Digital Signal Processors (S044)</p> <p>9:15 A.M.–10:45 A.M. Low-Cost Network Camera (S990)</p> <p>11:00 A.M.–12:30 P.M. An Overview of RapidIO™ with DSPs: The Interconnect, Interworking and Applications (S026)</p> <p>11:00 A.M.–12:00 P.M. DSP: The Electronics Market Driver (S553)</p> <p>11:00 A.M.–12:00 P.M. DSP Intercommunication in Audio/Video Infrastructure Environment (S573)</p>	<p>11:00 A.M.–12:00 P.M. SoCrates: System Visibility Tooling (S273)</p>	<p>9:15 A.M.–10:45 A.M. Getting the Most of the DaVinci™ Video Processing Sub-System (S583)</p> <p>9:15 A.M.–10:45 A.M. Understanding the Windows Media Ecosystem and VC-1 (S779)</p> <p>9:15 A.M.–10:45 A.M. <i>Panel:</i> Automotive Vision (S984)</p>	<p>11:00 A.M.–12:00 P.M. New Communications Curriculum with TI DSP Hardware at the University of Toronto (S053)</p>
12:00 P.M.–2:00 P.M. – Lunch and Exhibit Hall						
<p>3:15 P.M.–4:15 P.M. Optimization of Ogg Vorbis I Decoder on TMS320C5000™ DSP Platform (S031)</p>	<p>2:00 P.M.–3:00 P.M. TDD Technologies in Mobile Communications: A Case Study of TD-SCDMA Deployment (S223)</p> <p>3:00 P.M.–4:00 P.M. Introduction to MicroTCA (S169)</p> <p>3:30 P.M.–4:30 P.M. <i>Panel:</i> Using MicroTCA to Personalize Infrastructure (S593)</p> <p>4:30 P.M.–5:30 P.M. A System Perspective: ATCA and AMC for Multimedia Gateways (S269)</p>	<p>2:00 P.M.–3:00 P.M. Wireless Interrogation of SAW Strain Sensors for Automotive Applications Using TI's TMS320C28x™ Controller (S146)</p> <p>2:00 P.M.–3:00 P.M. Demonstrating an MSP430-Based Sensorless BLDC Motor Controller/General-Purpose Inverter with Power Factor Correction (S878)</p> <p>3:15 P.M.–4:15 P.M. A TMS320F2810 Controller-Based Ultrasonic Flowmeter Design with Software Security (S658)</p>	<p>12:00 P.M.–1:15 P.M. Analog e-Lab LIVE: Optimizing Analog to Digital Conversion in DSP-Based Applications (S156)</p> <p>2:00 P.M.–3:00 P.M. Power Management in Wireless SoC and Software (S056)</p> <p>2:00 P.M.–3:00 P.M. DC-DC Power Conversion Techniques for Battery-Operated System (S149)</p> <p>3:15 P.M.–4:15 P.M. Leveraging DSPs from Open Source Multimedia Frameworks (S035)</p> <p>3:15 P.M.–4:15 P.M. Battery Selection, Safety and Monitoring in Mobile Applications (S148)</p>	<p>3:15 P.M.–4:15 P.M. Advanced Scripting Techniques for Automating Regression Tests and Measurements with the Code Composer Studio™ IDE Scripting Utility (S030)</p> <p>3:15 P.M.–4:15 P.M. Utilizing the TMS320C64x™ Compiler to Optimize Performance and Reduce Code Size (S861)</p>	<p>2:00 P.M.–3:00 P.M. Developing IP Video Solutions: The Ins and Outs of Developing Video Phones (S060)</p> <p>2:00 P.M.–3:00 P.M. Compressive Imaging: A New Framework for Computational Image and Video Processing (S112)</p> <p>2:00 P.M.–3:00 P.M. Embedded Intelligence to Support the Entire Enterprise (S886)</p> <p>3:15 P.M.–4:15 P.M. DSP and FPGA Complementary Solutions for High-Definition Video Infrastructure Systems (S284)</p>	<p>2:00 P.M.–3:00 P.M. TI University Program Overview and Update (S183)</p>
5:00 P.M.–7:00 P.M. – Exhibit Hall and Hors d'oeuvres						

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8:00 A.M.–9:00 A.M. – Keynote: The Super Heroes of the Signal Processing Domain						
<p>9:15 A.M.–10:45 A.M. Implementing Efficient Delay Line Effects with dMAX, an Audio-Tuned DMA Engine (S058)</p> <p>9:15 A.M.–10:45 A.M. <i>Panel:</i> Audio Multi-Channel (S589)</p> <p>11:00 A.M.–12:00 P.M. Multi-Channel and Surround Sound Audio Coding on Floating-Point DSPs (S063)</p>	<p>9:15 A.M.–10:15 A.M. The Software-Defined Radio (SDR) Technology's Short-Term Applicability to Wireless Infrastructure Time-to-Market and Cost Drivers (S872)</p> <p>9:45 A.M.–11:15 A.M. What is the Role of SDR in Commercial Infrastructure? (S592)</p> <p>11:00 A.M.–12:00 P.M. Implementation of an SCA Core Framework on a TI TMS320C6416 DSP (S011)</p> <p>11:15 A.M.–12:15 P.M. Waveform Component Portability for DSP Processing Platforms (S885)</p>	<p>9:15 A.M.–10:15 A.M. Creating Closed-Loop Motion-Control Applications with The Mathworks Real-Time Workshop™ (S659)</p> <p>10:15 A.M.–11:15 A.M. Audio and Video Architecture for Velodyne Subwoofers Using TMS320C2000™ Digital Signal Controllers (S560)</p> <p>11:15 A.M.–12:15 P.M. Implementing High-Bandwidth, Low-Cycle Count Controllers for Digital Power Supplies (S456)</p>	<p>9:15 A.M.–10:45 A.M. Effective Usage of EDMA 3.0 (S039)</p> <p>9:15 A.M.–10:45 A.M. <i>Panel:</i> Reviewing the Changing Rules in the World of System Design (S581)</p> <p>9:15 A.M.–10:45 A.M. How to Deploy Compelling DSP + FPGA System Solutions Using C-Based and Model-Based Design (S874)</p> <p>9:15 A.M.–10:45 A.M. <i>Panel:</i> Processor Benchmarking – Measuring DSP Performance in a Meaningful Way (S981)</p> <p>11:00 A.M.–12:00 P.M. Using Power Modules to Power Processors (S224)</p>	<p>11:00 A.M.–12:00 P.M. Automated Programmability Solutions for TI DM Multicore Chips: TMS320DM320 DSP-Based Media Processor (S511)</p> <p>11:00 A.M.–12:00 P.M. Debugging Cache Coherence and Optimizing Cache Performance with New TMS320C64x™ DSP Tools (S942)</p>	<p>11:00 A.M.–12:00 P.M. TMS320C64x DSP Generation of Media Processors in Medical Ultrasound Imaging (S029)</p> <p>11:00 A.M.–12:00 P.M. Modeling De-Interlacing and De-Mosaicing Algorithms Using Simulink and Implementing on TMS320DM642 Digital Media Processors (S888)</p>	<p>11:00 A.M.–12:00 P.M. FPGA Coprocessor for TMS320C6000™ DSP Platform of DSP Starter Kits (DSKs) (S225)</p>
12:00 P.M.–2:00 P.M. – Lunch and Exhibit Hall						
<p>2:00 P.M.–3:00 P.M. A Beat-Matching Algorithm for a TMS320C55x™ DSP-Based Portable Media Player (S561)</p> <p>3:00 P.M.–4:00 P.M. Class-D Audio Amplifiers: Advantages, Tradeoffs and When to Choose D Versus A, B or AB (S601)</p>	<p>2:00 P.M.–3:00 P.M. Analyzing the Role and Evolution of Radio Network Controllers (S557)</p> <p>3:00 P.M.–4:00 P.M. RapidIO™ – A Case Study in Addressing the Dataplane Interconnect Performance Gap in Power-Efficient Embedded Communications Systems Performance Gap (S023)</p> <p>3:30 P.M.–4:30 P.M. Gigabit Ethernet vs. RapidIO™ (S551)</p> <p>4:00 P.M.–5:00 P.M. Building an Architecture for Video Transcoding and Transrating in the Infrastructure (S591)</p>	<p>2:00 P.M.–3:00 P.M. Enabling High-Frequency Power Conversion Applications Using Digital Controllers with High-Resolution PWM (S700)</p> <p>3:00 P.M.–4:00 P.M. Using Multi-Phase DC/DC Power Supply Control with the TMS320C28x™ Controller (S549)</p> <p>4:00 P.M.–5:00 P.M. Power Line Communication for Control Applications Using a Single TMS320C2000™ DSP Controller (S701)</p>	<p>2:00 P.M.–3:00 P.M. Decoding Power Supply Specifications for Embedded Systems (S571)</p> <p>2:00 P.M.–3:00 P.M. Linear 100 dB-w Wide Dynamic Range CMOS Sensor and TMS320DM642 Digital Media Processor Solution (S900)</p> <p>3:00 P.M.–4:00 P.M. Power Management Requirements and Solutions for High-Performance DSPs and FPGAs (S994)</p> <p>3:00 P.M.–4:30 P.M. Choosing a Processor: Benchmarks and Beyond (S043)</p>	<p>2:00 P.M.–3:00 P.M. Implementation of Fractional Math Operations in C++ (S911)</p> <p>3:00 P.M.–4:00 P.M. Developing Reference Framework 6 (RF6) DSP Programs with TI DSP/BIOS™ Processors (S036)</p> <p>4:00 P.M.–5:00 P.M. From Simulink to TI DSPs: An Accelerated Approach to Implementation (S510)</p> <p>4:00 P.M.–5:00 P.M. Power-Optimizing Embedded Applications (S589)</p>	<p>2:00 P.M.–3:00 P.M. H.264 Video Encoder Architectures for Real-Time HD Encoding Applications (S002)</p> <p>2:00 P.M.–3:00 P.M. Expanding Broadcast Infrastructures to Provide IPTV Services Leveraging High-Performance H.264 Transcoding (S893)</p> <p>3:00 P.M.–4:00 P.M. Adding Video Processing to Existing Voice Applications to Achieve Triple-Play Capabilities (S903)</p> <p>4:00 P.M.–5:00 P.M. High-Quality User Interfaces for Video Devices: Flash Player on TI TMS320C64x DSPs (S975)</p> <p>4:30 P.M.–5:30 P.M. Design and Capabilities for the Emerging Video Telephony Market (S168)</p>	<p>2:00 P.M.–3:00 P.M. Data Acquisition: Getting Started with Texas Instruments Products (S801)</p> <p>3:00 P.M.–4:00 P.M. An Application-Driven Undergraduate Laboratory Based on the TI TMS320C6713 DSK (S876)</p> <p>4:00 P.M.–5:00 P.M. Mission Critical Embedded Systems: An Expanded Curriculum Experiment (S913)</p>
5:00 P.M.–7:00 P.M. – Exhibit Hall and Conference Party						

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8:00 A.M.–9:00 A.M. – Keynote: The Super Heroes of the Signal Processing Domain						
<p>10:15 A.M.–11:15 A.M. Audio Improvements for Beam Forming, Echo and Noise Cancellation and Headphone Audio Shock Elimination (S899)</p> <p>11:15 A.M.–12:15 P.M. Innovative Solutions for Overcoming Ambient Noise Disturbances for Cellular Handset Users (S871)</p> <p>11:15 A.M.–12:15 P.M. Strategies for Handling Sample Rate Changes in Digital Audio Systems (S902)</p>	<p>9:15 A.M.–10:15 A.M. The Role of Picostations in CDMA (S170)</p> <p>9:45 A.M.–10:45 A.M. Implementation of Pico Basestation Baseband Using TI's TMS320C6482 DSP (S222)</p> <p>10:15 A.M.–11:15 A.M. Reducing Implementation Costs by Using CFR-Enabled High-Performance Transmitters (S272)</p> <p>11:15 A.M.–12:15 P.M. Basic Linear Algebra Subroutines, CLAPACK and the TMS320C67x™ DSP Generation (S938)</p>	<p>9:15 A.M.–10:15 A.M. An Open Digital Platform Architecture for Mechatronic Applications (S113)</p> <p>10:15 A.M.–11:15 A.M. Time-Triggered Protocols – A New Paradigm in Automotive and Industrial Networking (S095)</p> <p>11:15 A.M.–12:15 P.M. Implementation of a DSP Controller for a Permanent Magnet Synchronous Motor Using Model-Based Design Approach (S349)</p>	<p>10:15 A.M.–11:15 A.M. Video-Port to Video-Port Communication Using the TMS320DM642 Digital Media Processor (S858)</p> <p>11:15 A.M.–12:15 P.M. Seismic Sensor Demonstration System Using an ADS1256 and TMS320C5510 DSP (S860)</p> <p>11:15 A.M.–12:15 P.M. Designing Portable C Code: A Real World Example FAT16 on Secure Digital (SD) and/or CompactFlash™ Card that Runs on the TMS320C55x™ DSP and the MSP430 (S924)</p>	<p>9:15 A.M.–10:15 A.M. A Package Standard for Binary Reuse (S006)</p> <p>9:15 A.M.–10:15 A.M. Analog Design Tools Workshop I: Filter Pro Active Filter Design Program (Part I of II: Please also attend S287 directly following this one) (S009)</p> <p>10:15 A.M.–11:15 A.M. Analog Design Tools Workshop II: TINA-TI Simulator (Part II of II: Please also attend S009 directly preceding this one) (S287)</p> <p>11:15 A.M.–12:15 P.M. Compact JTAG (cJTAG): A New JTAG-Compliant Test and Debug Standard (S547)</p> <p>11:15 A.M.–12:15 P.M. ABI Changes to the TI ARM® (TMS470) Compiler Tools (S892)</p>	<p>9:15 A.M.–10:15 A.M. Adaptive Cross-Layer Energy-Efficient Design for Mobile Video Systems (S285)</p> <p>9:15 A.M.–10:15 A.M. Designing the Encoding and Decoding Components of the Three Deployed Digital Broadcast TV Systems (S988)</p> <p>10:15 A.M.–11:15 A.M. DSP and FPGA Complementary Solutions for High-Definition Video Infrastructure Systems (S147)</p> <p>10:15 A.M.–11:15 A.M. Rapid Development of a Professional H.264 High-Definition Encoder (S286)</p> <p>10:15 A.M.–11:15 A.M. eXpress Multimedia Interface Standard (XMIS): A Step to the Plug-and-Play Architecture for Multimedia Codecs (S993)</p> <p>11:15 A.M.–12:15 P.M. Digital Camera Image Pipeline: Algorithm Improvements (S603)</p>	<p>9:15 A.M.–10:15 A.M. Teaching Fast Convolution Using TMS320C6711 and TMS320C6713 DSKs (S986)</p>

All session, dates and times are subject to change. Please see www.ti.com/tidc06content for the most current schedule.

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