



Module 15

Activity: Data Acquisition Systems



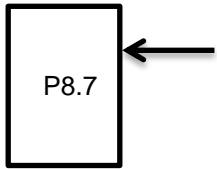
Activity: Data Acquisition Systems

Question 1

Write C code that samples ADC channel 18, P8.7. In particular implement these two functions. Use 14-bit mode, busy-wait, 3.3V reference.

```
void ADC0_InitSWTriggerCh18(void);
// initialize P8.7, channel A18
```

```
uint32_t ADC_In18(void);
// sample P8.7, channel A18
```



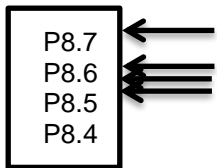
Question 2

Write C code that samples ADC channels 18-21, P8.7 to P8.4. In particular implement these two functions. Use 14-bit mode, busy-wait, 3.3V reference. Use call by reference to return four ADC samples.

```
void ADC0_InitSWTriggerCh18_19_20_21(void);
// initialize P8.7, P8.6, P8.5, P8.4, channels A18-A21
```

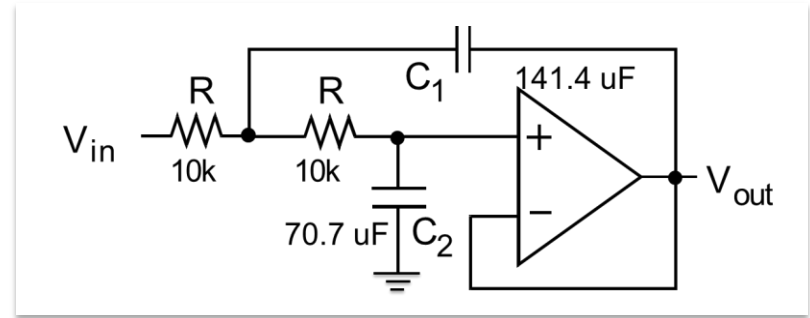
```
uint32_t ADC_In18_19_20_21 (
    uint32_t *ch18,
    uint32_t *ch19,
    uint32_t *ch20,
    uint32_t *ch21);
```

```
// sample P8.7, P8.6, P8.5, P8.4, channels A18-A21
```



Question 3

Using this design template, build a 1000 Hz, two-pole Butterworth low pass filter



Question 4

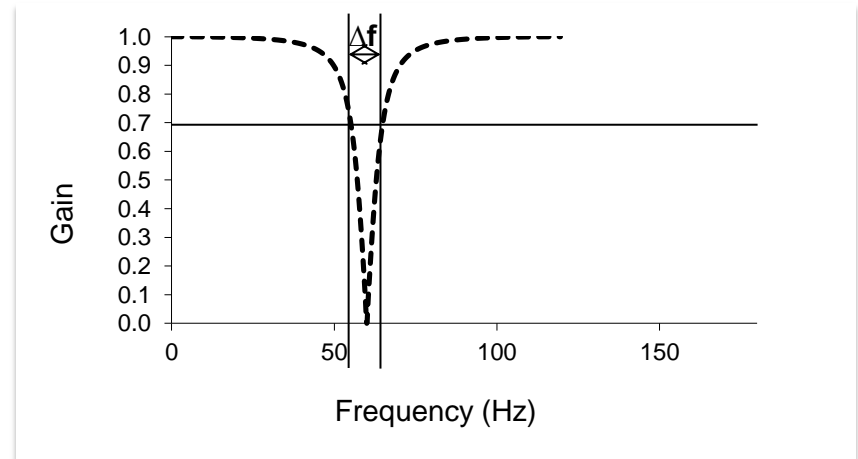
Write C code for the periodic ISR to implement this digital filter.

$$y(n) = (113 \cdot x(n) + 113 \cdot x(n-2) - 98 \cdot y(n-2)) / 12$$

where

- $x(n)$ is the current sample, e.g., $x[0] = \text{ADC_In12}()$;
- $x(n-1)$ is the previous sample, $x[1]$
- $x(n-2)$ is the sample two times ago, $x[2]$
- $y(n)$ is the current filter output, $y[0]$
- $y(n-2)$ is the filter output two times ago, $y[2]$

If the data are sampled at $f_s=240$ Hz, this filter is a high-Q ($Q=6$) 60 Hz reject filter.



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