Application Brief

How Ground Shifts Cause Logic Errors

Sadia Khan, Joshua Salinas

Introduction

Modern electronic systems often contain multiple boards, power domains, and distributed subsystems that do not share the same ground potential. These ground shifts can distort logic signals, corrupt communication, and lead to unexpected system behavior. As a result, a signal that is valid at the transmitter can fall outside the receiver's specificed input thresholds when a ground difference exists.

This article explains common causes of ground shift, how ground shift reduces logic margin, and demonstrates how TI's Ground-Level Translators (TXG) enable reliable communication between systems operating at different ground potentials.

Common Sources of Ground Shifts

In electronic systems, GND (ground) provides the voltage reference used by electronic circuits to interpret logic states. Table 1 summarizes the most common mechanisms that cause ground shift:

Table 1. Common Sources of Ground Shifts

Source of Ground Shift	How Shift Occurs
Cable and Connector Resistance	Load or return current flowing through cable and connector resistance creates an IR drop between different grounds.
Shared High-Current Return Paths	Motors, power converters, and other high-current loads can create a voltage difference across PCB traces, cables, and connectors.
Intentional Ground-Domain Offset	Some systems intentionally operate circuits at different ground potentials while still requiring digital communication between them.

Regardless of the source, these mechanisms create a voltage difference between two ground domains. If the shift becomes large enough, a valid transmitted HIGH or LOW can fall outside the receiver’s specified input range, resulting in a logic error.

How Ground Shifts Cause Logic Errors

A receiver interprets an input relative to its local ground. A difference in ground potential changes how the transmitted signal is seen by the receiver.

Figure 1 shows how positive and negative ground shifts reduce the available HIGH and LOW level logic margins. In this example, a +0.8V ground shift causes the assumed HIGH output to fail just below the receiver’s specified HIGH threshold, while a -0.8V ground shift causes the assumed LOW output to rise just above the specified LOW threshold. The diagram assumes receiver input thresholds of $V_{IH(min)} = 0.7 \times V_{CC}$ and $V_{IL(max)} = 0.3 \times V_{CC}$ for a 3.3V system, along with assumed transmitter output levels, to show the effect of ground shift on logic margin. Actual input thresholds are device-specific.

For 3.3V, the calculation is:

- $V_{IH(min)}$ = 0.7(3.3) = 2.31V
- $V_{IL(max)}$ = 0.3(3.3) = 0.99V

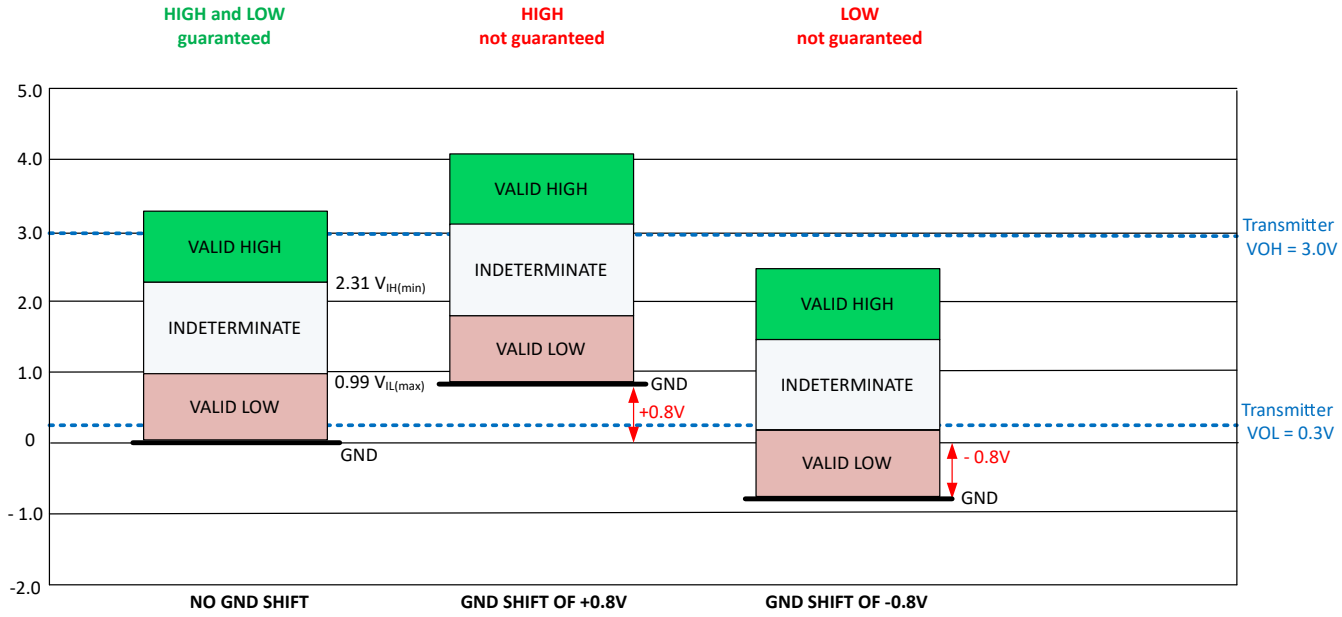

Figure 1. Effect of Ground Shift on CMOS Logic Levels

Example: Ground Shift Between Digital Circuits

Consider a 1.8V controller communicating with a 1.8V peripheral circuit. At lower supply voltages, the available logic margin becomes smaller, making the interface more sensitive to ground differences.

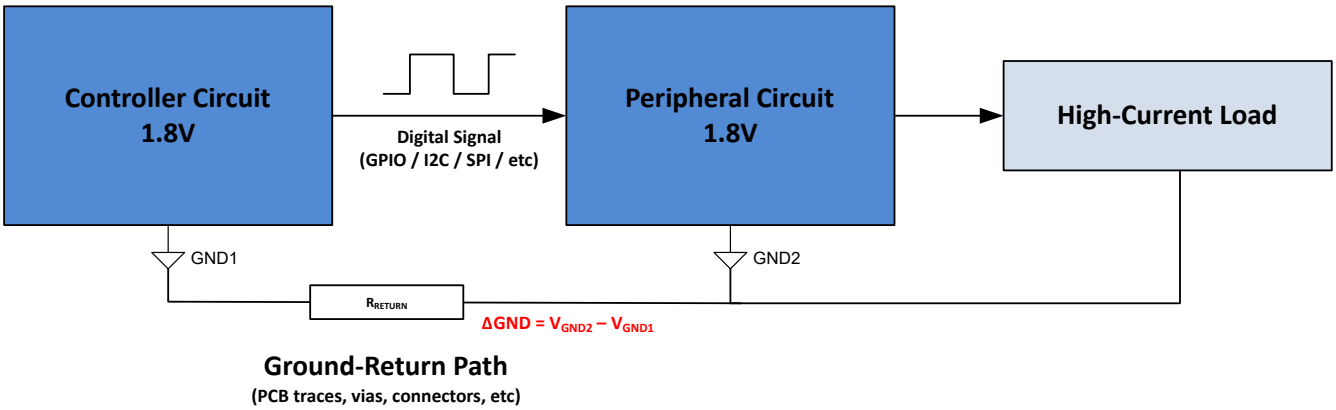

Figure 2. Ground Shift Caused by a Shared Ground-Return Path

Although both devices operate at the same supply voltage, load current flowing through a shared ground-return path can create a voltage difference between GND1 and GND2. The receiver interprets the digital signal relative to its local ground, which can reduce the available logic margin.

The ground shift created by the return path can be estimated as:

- $V_{GND\_SHIFT} = I_{Load} \times R_{return}$

In this block diagram, if 1A load current flows through 200mΩ of ground-return resistance, the resulting ground shift is 0.2V:

- $V_{GND\_SHIFT} = I_{Load} \times R_{return}$ = 1A × 200mΩ = 0.2V ground shift

Consequently, as current flow increases, the ground shift increases.

The example in Figure 3 shows how the same digital interface loses logic margin as the receiver ground shifts from 0V to -0.2V to -0.4V to -0.8V relative to the transmitter or system ground. At a ground shift of -0.2V, 190mV of LOW-level noise margin remains. At -0.4V, the receiver's $V_{IL(max)}$ shifts to 0.14V while the transmitted low remains at 0.15V. Because the transmitted LOW is now 10mV above the receiver's specified LOW threshold, it is no longer specified to be recognized as a LOW. At -0.8V, the transmitted LOW falls further outside the receiver's specified LOW region.

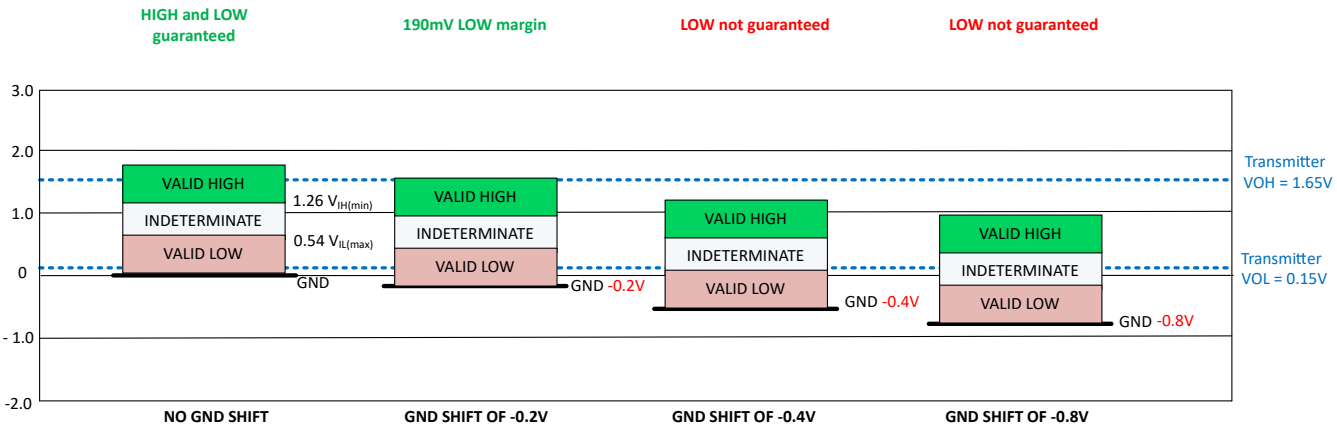

Figure 3. Reduced Margin as Ground Shift Increases

The amount of ground shift that can be tolerated is system dependent. Designers must evaluate the expected ground difference against the transmitter output levels and receiver input thresholds to determine whether the shift is minimal, reduces the available noise margin, or is large enough to cause a logic error. A ground shift that is insignificant for one interface can consume a substantial portion of the logic margin in another, particularly at lower supply voltages or in noisy environments.

When is a Ground-Level Translator Needed?

A common approach to addressing ground shift is to reduce the ground difference itself. Designers can use lower-resistance ground-return paths or star-grounding techniques to minimize shared return paths. For small, predictable ground differences, passive circuitry can also be used to maintain valid logic levels.

These approaches may not be practical when the ground difference is larger, varies with operating conditions, or cannot be eliminated. Galvanic isolation can enable communication across different ground potentials, but can also add components, cost, board area, and power.

TI's Ground-Level Translators (TXG) enable digital communication between devices referenced to different ground potentials. Each side of the TXG is referenced to its respective local ground, allowing valid logic levels to be maintained across the ground difference. Figure 4 shows a -0.8V ground shift causing a logic error between the Controller Circuit and Periphal Circuit. Figure 5 shows how a TXG ground-level translator maintains the appropriate logic levels relative to each circuit's local ground.

The TXG portfolio includes ground-level translators supporting up to ±10V, ±40V, and ±80V ground differences, with 1-,2-, 4-channel configurations available. TXG provides a compact and high-performance option when the ground difference cannot be practically eliminated and can also be implemented late in the design cycle when changes to the existing ground architecture are no longer feasible.

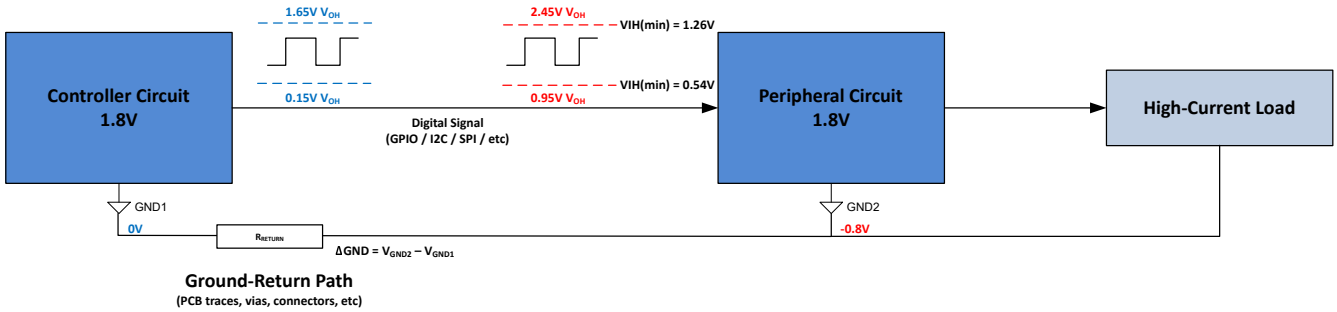

Figure 4. Ground Shift Causes the Receiver LOW Threshold to Be Violated

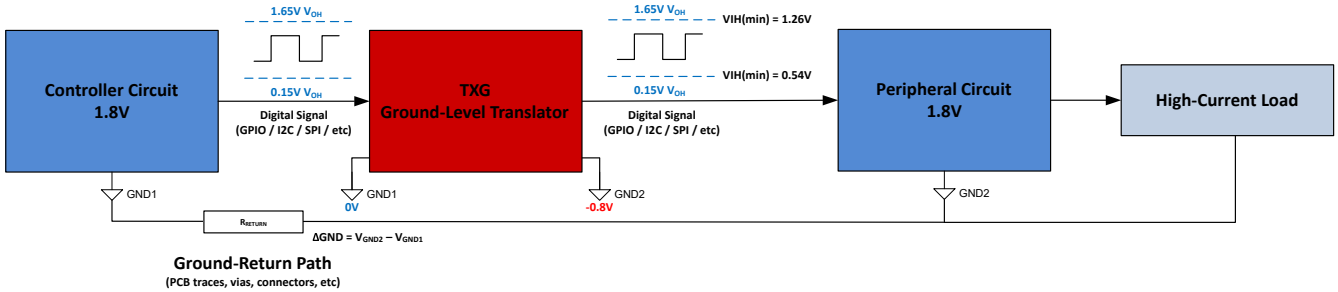

Figure 5. TXG Maintains Valid Logic Levels Across the Ground Difference

Conclusion

Ground shifts reduce available logic margin and can cause valid transmitted signals to fall outside a receiver's specified input thresholds. TI Ground-Level Translators enable reliable digital communication across different ground potentials by referencing each side of the device to its respective local ground.

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