

Achieving Multi-Channel, Low-Latency, High Precision Data Acquisition Systems Using the ADS125P08



Introduction

Many modern sensing platforms—such as a multi-sensor biomedical wearable that must capture ECG, EMG, temperature, and motion data simultaneously—require low-latency, high-precision measurements. However, most multiplexed ADCs are not both fast and precise enough for these demanding applications. Additionally, these ADCs require constant intervention from the host to configure the device and read data.

The [ADS125P08](#) meets this challenge by integrating three key features that enable multi-channel, low-latency, high precision, data acquisition systems:

- A flexible 16-channel multiplexer with a low latency, high resolution delta sigma ADC
- A highly-configurable channel auto-sequencer that reduces communication overhead
- A 512-word first-in, first-out (FIFO) buffer for efficient data transfer

Low latency, high resolution delta sigma ADC

The core features of the ADS125P08 are the 16-channel, highly-flexible input multiplexer followed by a buffered, low-noise, 24-bit delta-sigma ADC. The ADC architecture includes a low-latency digital filter required by high-throughput systems. [Figure 1](#) shows an example of high-precision system that measures multiple inputs with different signal types:

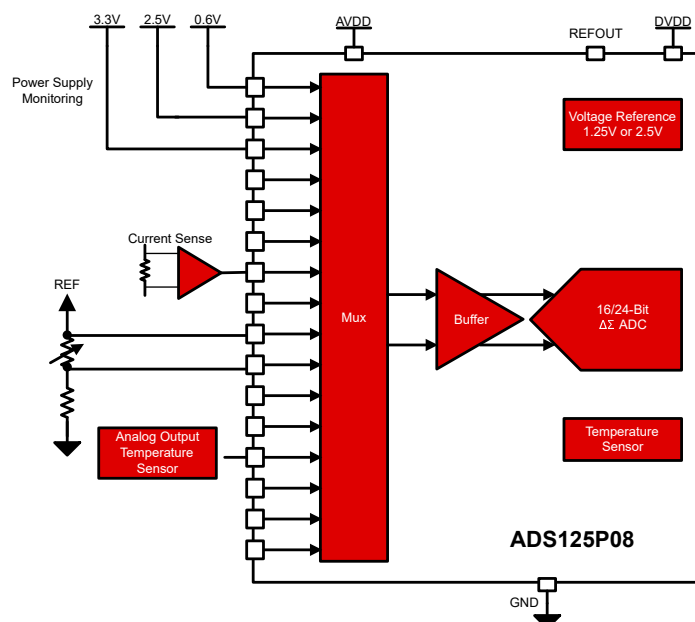


Figure 1. ADS125P08 System Monitoring

Table 1 lists the important ADS125P08 data sheet parameters required to measure the system shown in Figure 1, including the latency for different data rates, the corresponding noise performance, and the total cycle time to sample all 16 single-ended inputs:

Table 1. ADS125P08 Data sheet Parameters

Generic: Parameter	Values				Unit
Data Rate	1066	800	533	400	kSPS
Filter type	Sinc4	Sinc4	Sinc4	Sinc4	
Latency	4.8	6.1	9.6	11.1	μs
Effective resolution	17	18.4	19.6	19.9	Bits
Noise	41.2	17.52	9.52	7.71	μV _{RMS}
Total cycle time (16 channels)	76.8	97.6	153.6	177.6	μs
	13.0	10.2	6.5	5.6	kSPS

For example, Table 1 shows how the ADS125P08 can measure all 16 channels in 76.8 microseconds at 1066kSPS while maintaining >16-bit performance across all signal types. This performance enables the ADS125P08 to be used in all low-latency, high-precision applications.

Channel Auto-Sequencer

The ADS125P08 also includes a channel auto sequencer that stores up to 32 configurable conversion steps and runs them automatically. As a result, the auto-sequencer manages all channel-switching and timing inside the ADC, reducing per-sample re-configuration and extra SPI transactions. Additionally, the sequencer provides deterministic timing that reduces both command latency and overall communication overhead.

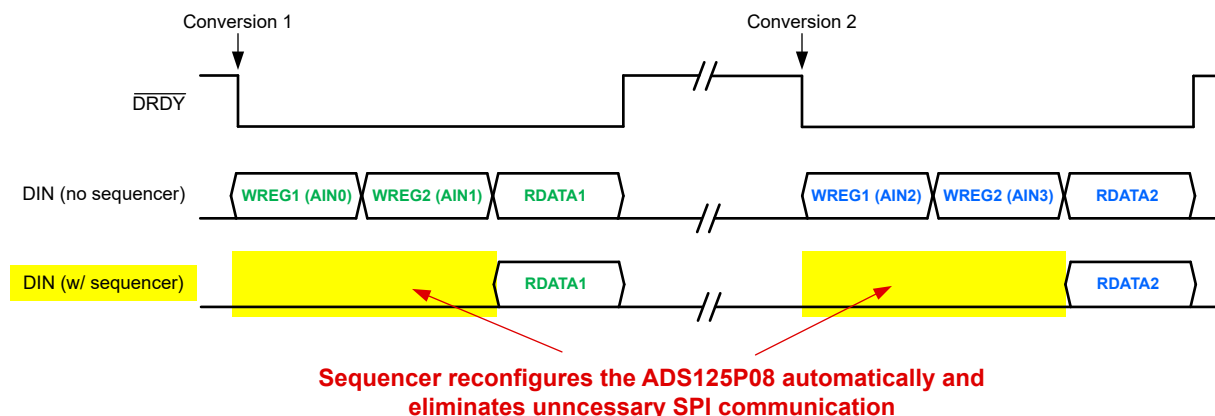


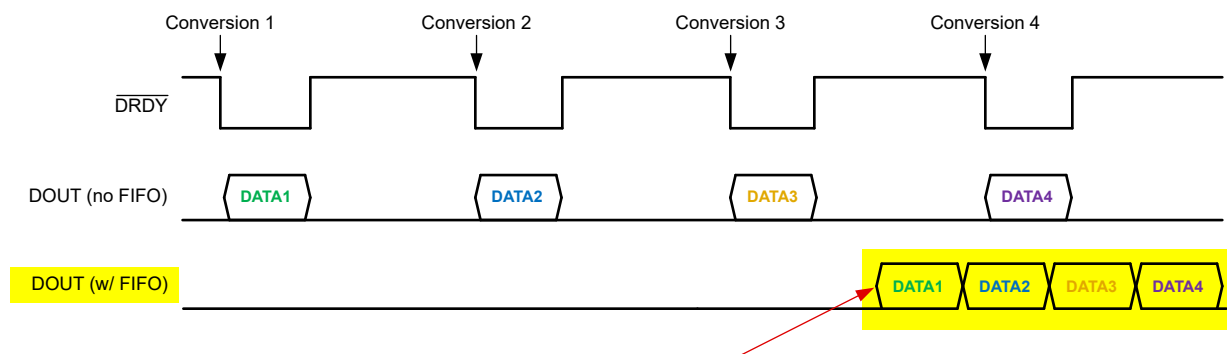
Figure 2. ADS125P08 Channel Auto Sequencer

Important ADS125P08 auto-sequencer features that reduce overall system latency include:

- **Pre-programmed step configurations:** Store up to 32 sequence steps (each with its own channel, filter, delay, and number-of-conversions) in volatile device registers after power-up. The ADC switches configurations internally without host SPI traffic, eliminating *WREG* command latency between each channel change.
- **Batch conversion per step:** Each step can execute up to 512 conversions automatically. The host therefore only needs to start the sequence once and then read the results from the FIFO compared to issuing a command for every conversion.
- **Multiple operating modes:** Continuous-sequence mode lets the ADC loop through the defined steps indefinitely, providing a steady stream of data with no host intervention. Single-sequence mode enables the host to obtain a quick snapshot with minimal handshaking.
- **DRDY behavior tied to sequencer:** DRDY can be asserted on every conversion, every step, every full sequence, or on defined FIFO thresholds. This lets the host synchronize reads to the most convenient granularity, avoiding unnecessary wakeups.

FIFO Buffer

The ADS125P08 integrates a FIFO buffer that temporarily stores up to 512 conversion results (data + status + CRC) so the ADC can keep sampling at full speed while the host reads data in larger bursts. Fewer SPI cycles, fewer interrupts, and automatic error checking all reduce time spent transferring data between the ADC and the processor.



Use ADS125P08 FIFO to read data at any time and enable bulk / burst transfers

Figure 3. ADS125P08 FIFO Buffer

Important ADS125P08 FIFO features that reduce overall system latency include:

- **Burst-mode data capture:** The 512-word 42-bit circular FIFO stores conversion results so the ADC can keep sampling at its maximum rate while the host reads at its own pace. This decouples the higher-speed ADC from the slower host-controller interface, eliminating the need for the host to poll after every conversion and reducing CPU load
- **Overflow/underflow indicators:** FIFO depth, overflow, and underflow flags let the firmware quickly detect when the host is falling behind or reading too fast, enabling corrective actions without costly data-loss handling.
- **Programmable thresholds:** FIFO-threshold registers can trigger the DRDY pin when a configurable number of samples is ready, allowing the host to be interrupted only when a useful batch is available—fewer interrupts and less latency.
- **CRC per word:** Built-in CRC validation removes the need for separate error-checking code, speeding up data verification.

References

- Texas Instruments, [ADS125P08 8/16-Channel, 1MSPS, 24-Bit, Delta-Sigma ADC Datasheet](#), datasheet

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