

Accelerating Real-Time Ultrasound Beamforming With Texas Instruments and the NVIDIA Holoscan Sensor Bridge



An ultrasound system provides noninvasive, real-time visual images of the body's internal organs, bones, tissues and blood flow using high-frequency sound waves. A typical system uses a transducer probe that integrates piezoelectric sensors. A high-voltage transmitter (TX) drives multiple channels. High-voltage sound signals travel through the human body; a low-noise analog front-end (AFE) receiver (RX) returns the signal as an echo. Both TX and RX connect to a processing unit that can generate images based on the transmitted sound signals and received echo.

A platform combining the Texas Instruments (TI) TX73L64 TX and AFE5932 AFE RX with the [NVIDIA Holoscan Sensor Bridge](#) (HSB) enables designers to design an ultrasound system.

The [TX73L64](#) is a highly integrated, high-performance TX device for ultrasound imaging systems. The device has 64 pulser circuits, 64 T/R switches and 32 low-noise amplifier (LNA) circuits and supports an on-chip beamformer. The TX/RX switches perform a 2-to-1 multiplexing operation to multiplex inputs of two channels to one LNA. The TX73L64 also integrates on-chip floating power supplies that reduce the number of required high-voltage power supplies. The device has 64 pulser circuits that generate three-level high-voltage pulses (up to $\pm 100\text{V}$) in order to excite multiple channels of an ultrasound transducer. The device supports a total of 64 outputs, while the maximum output current on each output is 1A.

The [AFE5932](#) is a highly integrated, low-power RX device that includes a total of 32 RX channels, each featuring an attenuator, a programmable gain amplifier and low-pass filter, and 16 analog-to-digital converters (ADCs). Each ADC samples two channels in an interleaved manner.

The AFE5932 EVM also enables control of two TX73L64 and two AFE5932 devices using a simple GUI with USB (using the field-programmable gate array (FPGA) board [TSWDC155C](#)). Designers can program brightness-mode or continuous-wave TX modes, and store and switch between multiple pattern and delay profiles for the TX devices. An LNA and digital time gain compensation control enables even more control over the RX signal.

The EVM uses a complementary metal-oxide semiconductor and the Low-Voltage Differential Signaling (LVDS) serial peripheral interface. Error flag registers detect faulty conditions and perform automatic thermal shutdown of the TX73L64 devices.

GUI software captures and analyzes data from the AFE, either ADC-sampled data or ADC test patterns. [Figure 1](#) shows the AFE5932 EVM connected to the TSWDC155C.

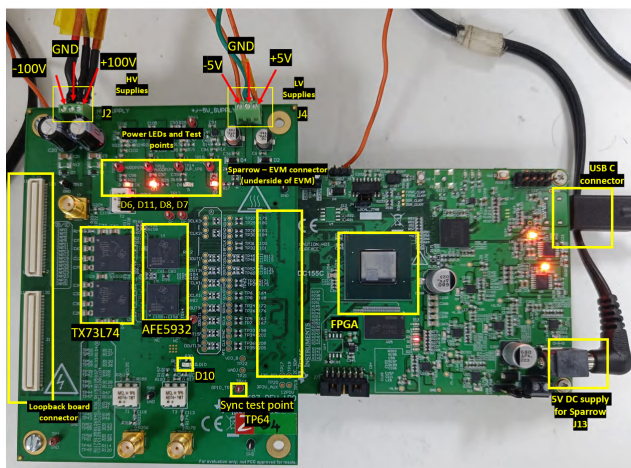


Figure 1. The AFE5932 EVM Connected to the TSWDC155C

TI and NVIDIA's joint reference demonstration takes raw channel data from the AFE5932 EVM, streamed through NVIDIA's HSB into a real-time Compute Unified Device Architecture (CUDA) delay-and-sum beamformer to produce a live B-mode image. The reference platform illustrates the tight integration between NVIDIA's HSB and TI's TX and RX devices, and gives designers a working pattern for putting modern graphics processing unit (GPU)-accelerated processing directly behind a TI AFE. [Figure 2](#) highlights how each of the system components are connected to each other and with the probe.

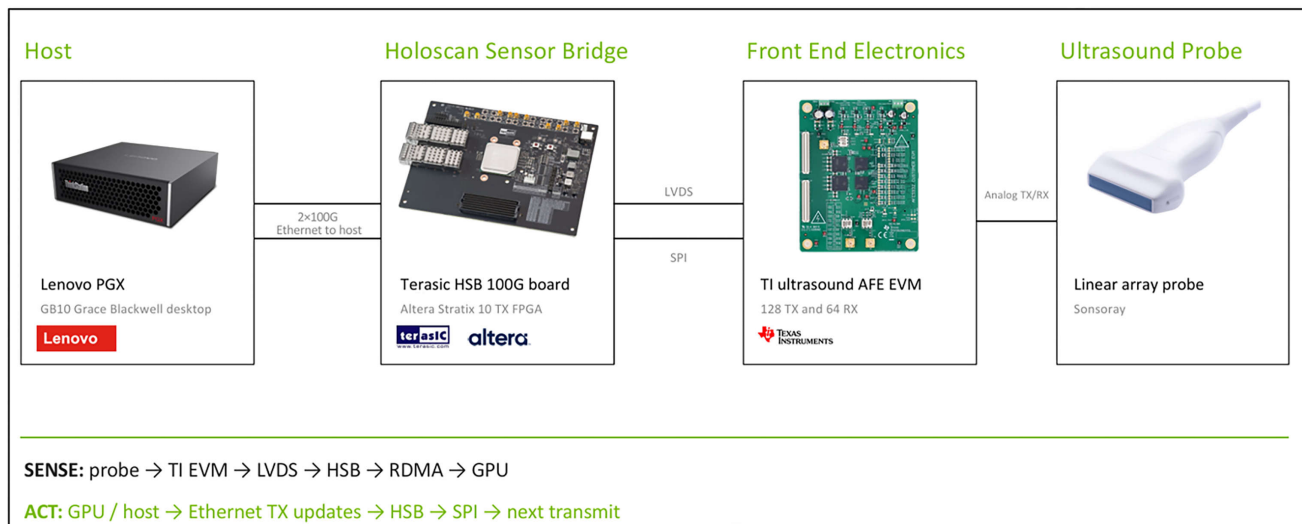


Figure 2. System Overview and Connections Between HSB and AFE5932EVM

The AFE5932 EVM pairs with a TSWDC155C FPGA board that egresses captured channel data over USB. Because the TSWDC155C does not expose Ethernet from the FPGA, this collaboration replaces it with an HSB-ready FPGA carrier (for example, an FPGA mezzanine card-coupled development board), on which NVIDIA implements the HSB RoCE v2 TX to drive sensor data to the GPU compute. The TSWDC155C FPGA design is referenced for the AFE-facing digital interface (LVDS, sync, Serial Peripheral Interface) but is not the target carrier.

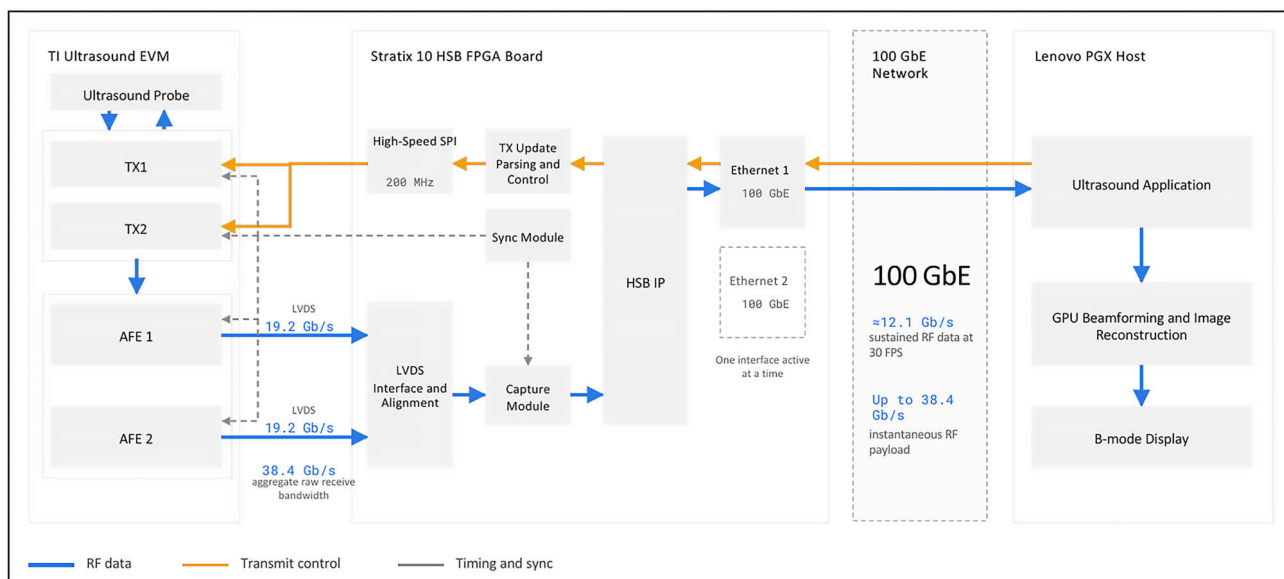


Figure 3. High-Level Block Diagram of Overall System and Connections Between Boards

The primary (P0) deliverable is a working delay-and-sum beamformer producing a live B-mode image from the AFE5932 EVM, end to end on the GPU through the HSB. CUDA delay and sum is a well-understood workload with previous NVIDIA reference implementations. Beyond P0, the same pipeline supports advanced artificial intelligence applications on raw sensor data such as a raw-to-insights pattern.

NVIDIA already has a public raw-to-insights ultrasound project with Siemens Healthineers (NV-Raw2Insights-US, GTC 2026), where channel data streamed through the HSB feeds a model performing real-time patient-adaptive image correction. Standing this pipeline up behind a TI AFE offers a direct path to those workloads.

A platform using TI's TX73L64 and AFE5932 interfaced with NVIDIA's HSB enables designers with a reference platform to design an ultrasound system.

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