Quad Digital Filter for 2nd-Order Delta-Sigma Modulator

FEATURES

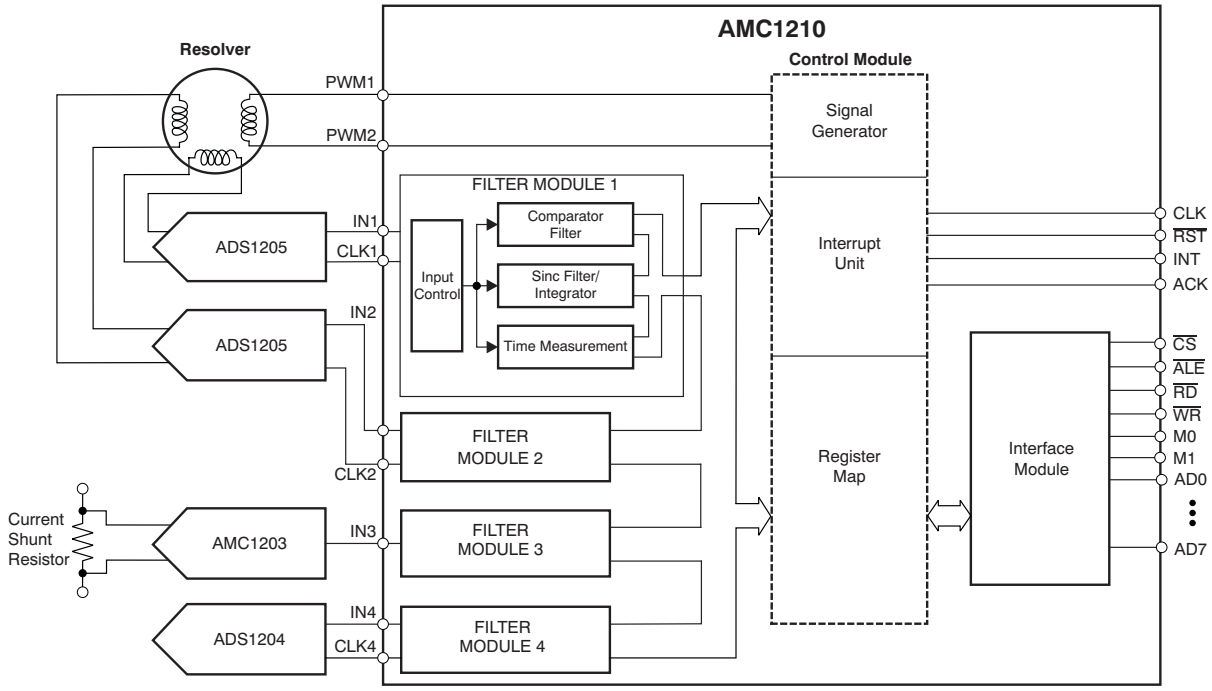
- **Four Independently-Programmable Digital Filters**
- **Four Window Comparators**
- **Three Parallel and One Serial Interface**
- **Comprehensive Interrupt System**
- **Programmable Input Configuration**
- **Carrier Frequency Generator for Resolver Applications**

APPLICATIONS

- **Current Measurement**
- **Resolver Decoding**

DESCRIPTION

The AMC1210 is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each input can receive an independent delta-sigma (ΔΣ) modulator bit stream. The bit streams are processed by four individually-programmable digital decimation filters. The AMC1210 also offers a flexible interface and a comprehensive interrupt unit, allowing customized digital functionality and immediate digital threshold comparisons for over-current monitoring.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
AMC1210	QFN-40	RHA	–40°C to +125°C	AMC1210I	AMC1210IRHAT	Tape and Reel, 250
					AMC1210IRHAR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted.(1)

	AMC1210	UNIT
Supply voltage, all supplies (AVDD, BVDD, CVDD, DVDD) to GND	–0.3 to +6	V
Digital input to GND	GND – 0.3 to BVDD + 0.3	V
Ground voltage difference, AGND to GND	±0.3	V
Input current to any pin except supply pins	–10 to +10	mA
Power dissipation	See Dissipation Ratings Table	
Operating virtual junction temperature range, T_J	–40 to +150	°C
Operating free-air temperature range, T_A	–40 to +125	°C
Storage temperature range, T_{STG}	–65 to +150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	$T_A \le +25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = +25°C$	$T_A = +70°C$ POWER RATING	$T_A = +85°C$ POWER RATING	$T_A = +125°C$ POWER RATING
RHA(1)	3787mW	30.3mW/°C	2424mW	1969mW	758mW

(1) The thermal resistance (junction-to-ambient) of the RHA package is 32°C/W.

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ELECTRICAL CHARACTERISTICS

At –40°C to +125°C, AVDD, CVDD, DVDD = 5V, and BVDD = 2.7V, unless otherwise noted. The following condition must be true on the supplies: CVDD ≥ DVDD ≥ BVDD.

PARAMETER	TEST CONDITIONS	AMC1210 MIN	AMC1210 TYP	AMC1210 MAX	UNIT
DIGITAL INPUT/OUTPUT					
Logic levels:			CMOS		
V_{OH}	BVDD = 2.7	2.4			V
	BVDD = 5.0	4.44			V
V_{OL}	BVDD = 2.7			0.4	V
	BVDD = 5.0			0.5	V
V_{IH}		0.7BVDD			V
V_{IL}				0.3BVDD	V
System clock frequency	Pin 'CLK'			90	MHz
Modulator clock frequency	Pins CLK1, CLK2, CLK3, CLK4 Mode = 0			22	MHz
SPI interface clock frequency	Pin $\overline{WR}$, option 1			25	MHz
SPI interface clock frequency	Pin $\overline{WR}$, option 2			40	MHz
Parallel interface read/write frequency	Pin $\overline{CS}$			22	MHz
POWER-SUPPLY REQUIREMENTS					
Power-supply voltage, pin AVDD		4.5		5.5	
Power-supply voltage, pins CVDD and DVDD	CVDD ≥ DVDD ≥ BVDD	3.0		5.5	V
Power-supply voltage, pin BVDD	CVDD ≥ DVDD ≥ BVDD	2.4		5.5	V
Total power(1)	All supplies = 5V		24.5		mW
Power-supply current	One filter module(2)		260		µA/MHz
Power-supply current	Four filter modules(2)		850		µA/MHz
	SPI interface		78		µA/MHz
	Parallel interface(3)		83		µA/MHz
	Signal generator		140		µA/MHz
SIGNAL GENERATOR OUTPUT					
V_{OH}	R_{LOAD} = 50Ω, bit HPE = 1	4.60	4.73		V
V_{OL}	R_{LOAD} = 50Ω, bit HPE = 1		0.26	0.4	V
V_{OH}	R_{LOAD} = 500Ω, bit HPE = 0	4.60	4.73		V
V_{OL}	R_{LOAD} = 500Ω, bit HPE = 0		0.26	0.4	V

(1) Power consumption with two filter modules functioning, both set to $Sinc^3$, SOSR = 256.
(2) The filter module is configured with the comparator unit filter set to $Sinc^3$, COSR = 32 and the sinc unit filter set to $Sinc^3$ structure and SOSR = 256.
(3) All three modes.

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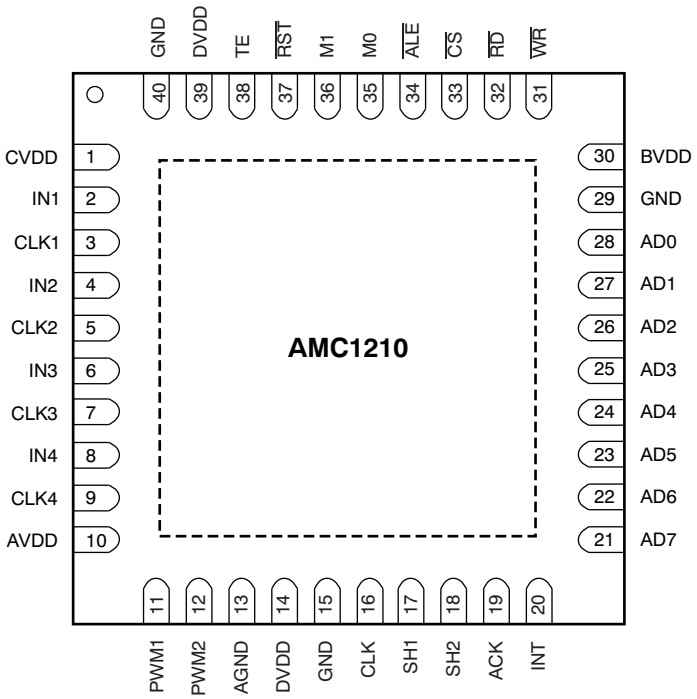
DEVICE INFORMATION

RHA PACKAGE(1)
QFN-40
(TOP VIEW)



(1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

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Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
1	CVDD		Modulator side supply(1)
2	IN1	Input	Data input from Modulator 1
3	CLK1	Bidirectional	Clock from/to Modulator 1
4	IN2	Input	Data input from Modulator 2
5	CLK2	Bidirectional	Clock from/to Modulator 2
6	IN3	Input	Data input from Modulator 3
7	CLK3	Bidirectional	Clock from/to Modulator 3
8	IN4	Input	Data input from Modulator 4
9	CLK4	Bidirectional	Clock from/to Modulator 4
10	AVDD		Signal generator supply
11	PWM1	Output	Signal generator output
12	PWM2	Output	Signal generator output (inverted)
13	AGND		Signal generator ground
14	DVDD		Core supply
15	GND		Ground
16	CLK	Input	System clock
17	SH1	Input	First asynchronous sample-and-hold
18	SH2	Input	Second asynchronous sample-and-hold
19	ACK	Output	Acknowledge signal
20	INT	Output	Interrupt signal
21	AD7	Bidirectional	Data bus bit 7 (most significant bit)
22	AD6	Bidirectional	Data bus bit 6
23	AD5	Bidirectional	Data bus bit 5
24	AD4	Bidirectional	Data bus bit 4
25	AD3	Bidirectional	Data bus bit 3
26	AD2	Bidirectional	Data bus bit 2
27	AD1	Bidirectional	Data bus bit 1
28	AD0	Bidirectional	Data bus bit 0 (least significant bit)(2)
29	GND		Ground
30	BVDD		Controller side supply(3)
31	$\overline{WR}$	Input	Write signal(2)
32	$\overline{RD}$	Input	Read signal(2)
33	$\overline{CS}$	Input	Chip select signal(2)
34	$\overline{ALE}$	Input	Address latch enable (2)
35	M0	Input	First mode pin
36	M1	Input	Second mode pin
37	$\overline{RST}$	Input	Active-low asynchronous reset
38	TE	Input	For factory test only; must be tied to ground
39	DVDD		Core supply
40	GND		Ground

(1) The pins for the modulator side are 1 to 9.
(2) Functionality is dependent on device setup. To see a list of pin functions/names in each mode, see Table 3.
(3) The pins for the controller side are 16 to 38.

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MODULATOR INPUT MODES

TIMING CHARACTERISTICS

Over recommended operating free-air temperature range at –40°C to +125°C, DVDD = +5V, CVDD = +5V, and BVDD = +2.7V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{w1}	Mode 0 clock period CLKx	45	1/64th of CLK period	ns
t_{w2}	Mode 0 clock high time CLKx	10	t_{w1} – 10	ns
t_{su1}	Setup time from data valid to CLKx high	5		ns
t_{h1}	Hold time from CLKx high to data invalid	5		ns
t_{w3}	Mode 1 clock period CLKx	90	1/128th of CLK period	ns
t_{w4}	Mode 1 clock high time CLKx	20	t_{w3} – 10	ns
t_{su2}	Setup time from data valid to CLKx high or low	5		ns
t_{h2}	Hold time from CLKx high or low to data invalid	5		ns
t_{w5}	Mode 2 data width INx	45		ns
t_{w6}	Mode 2 data pulse width INx	22		ns
t_{w7}	Mode 3 clock period CLKx	22	1/32nd of CLK period	ns
t_{w8}	Mode 3 clock high time CLKx	5	t_{w7} – 5	ns
t_{su3}	Setup time from data valid to any CLKx high	5		ns
t_{h3}	Hold time from any CLKx high to data invalid	5		ns
t_{w9}	System clock period CLK	11	10^6	ns
t_{w10}	System clock high time CLK	3	t_{w9} – 3	ns
t_{w11}	Mode 3 generated clock period CLK_x	t_{w9}	t_{w9} × MD control bits	ns
t_{w12}	Mode 3 generated high time CLKx	t_{w10} – 2	t_{w10} + 2	ns
t_{d1}	Delay from system clock CLK high to generated CLKx high	0	3	ns
t_{d2}	Delay from system clock CLK low to generated CLKx low	0	3	ns
t_{su4}	Setup time from data valid to any CLKx high	5		ns
t_{h4}	Hold time from any CLKx high to data invalid	5		ns

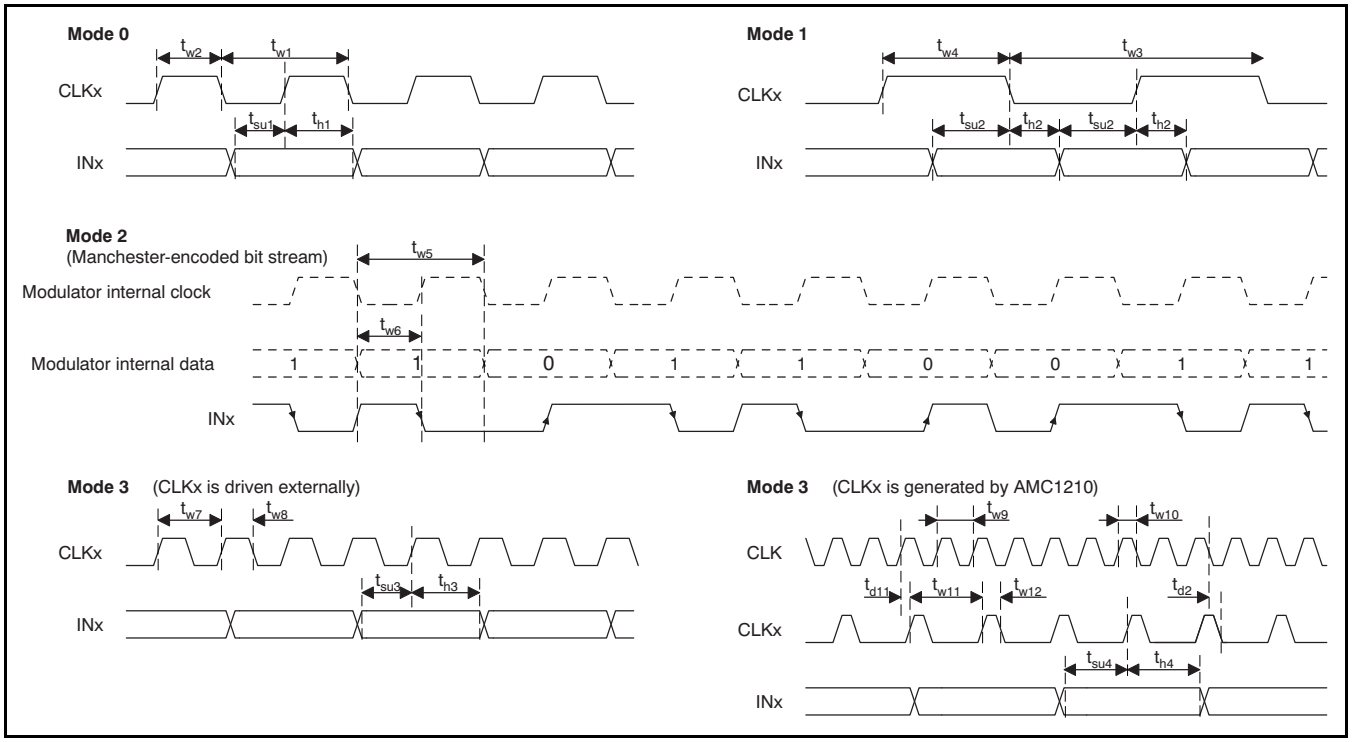

Figure 1. Modulator Input Mode Timing

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SPI INTERFACE MODES

TIMING CHARACTERISTICS(1)

Over recommended operating free-air temperature range at –40°C to +125°C, DVDD = +5V, and BVDD = +2.7V, unless otherwise noted.

PARAMETER		Option 1		Option 2		UNIT
		MIN	MAX	MIN	MAX	
t_{c1}	$\overline{WR}$ period	40		25		ns
t_{w1}	$\overline{WR}$ HIGH or LOW time	10		10		ns
t_{d1}	Delay time from $\overline{CS}$ falling to $\overline{WR}$ rising edge	0		0		ns
t_{d2}	Delay time from $\overline{CS}$ falling to ADO not tristate		10		10	ns
t_{su1}	Data setup time	5		5		ns
t_{h1}	Input data hold time	5		5		ns
t_{d3}	Output data delay time		24		24	ns
t_{d4}	Enable lag time	10		10		ns
t_{d5}	ADO disable time		10		10	ns
t_{w2}	Sequential transfer delay	15		15		ns

(1) All input signals are specified with $t_R = t_F = 5$ns (10% to 90% of BVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

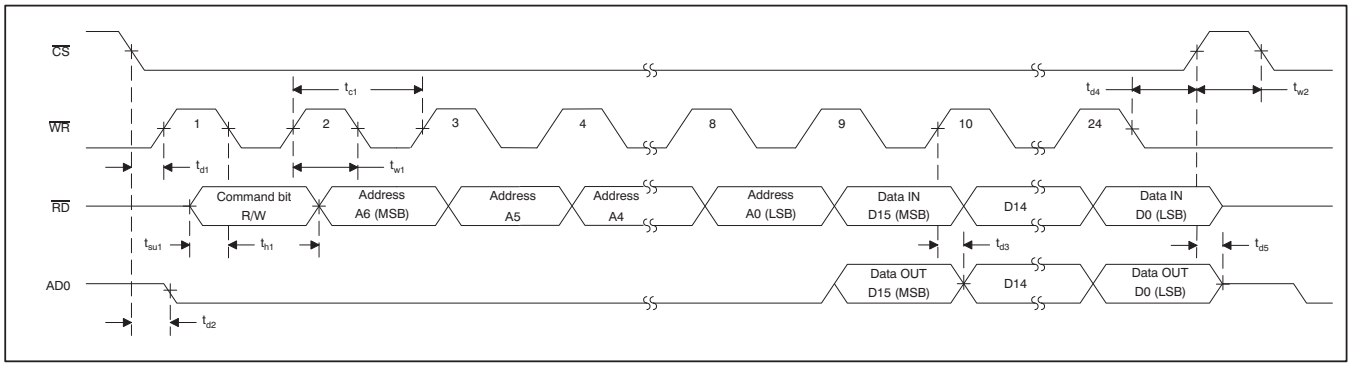

Figure 2. SPI Interface Option 1—SPI Normal Interface

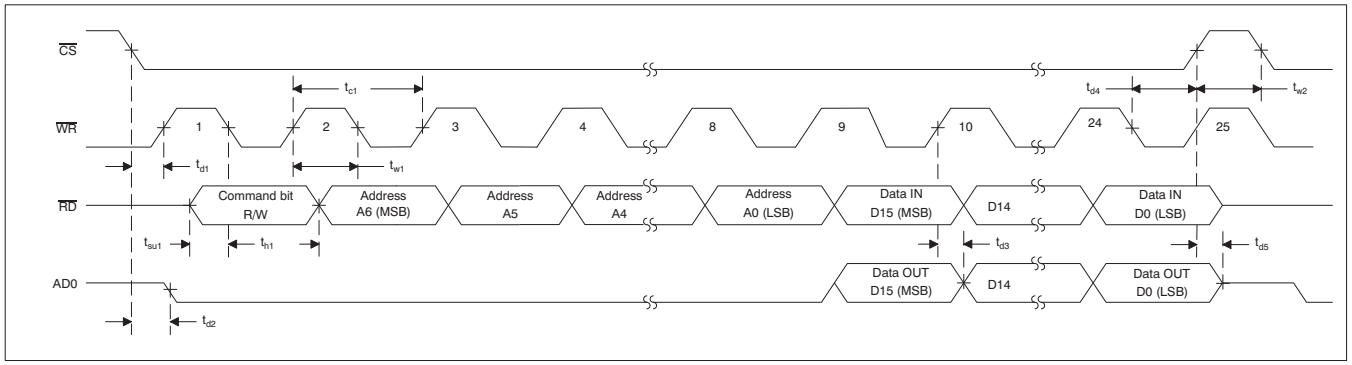

Figure 3. SPI Interface Option 2—SPI Fast Interface (> 25MHz)

PARALLEL MODE 1

TIMING CHARACTERISTICS(1)

Over recommended operating free-air temperature range at –40°C to +125°C, DVDD = +5V, and BVDD = +2.7V, unless otherwise noted.

PARAMETER(2)		MIN	MAX	UNIT
t_{w1}	$\overline{CS}$ low width	40		ns
t_{w2}	$\overline{CS}$ high width	5		ns
t_{d1}	Delay time from $\overline{CS}$ low to $\overline{WR}$ low	3		ns
t_{d2}	Delay time from $\overline{WR}$ high to $\overline{CS}$ high	5		ns
t_{w3}	$\overline{WR}$ low width	10		ns
t_{w4}	$\overline{WR}$ high width	10		ns
t_{su1}	Setup time from $\overline{ALE}$ high to $\overline{WR}$ low	0		ns
t_{h1}	Hold time from $\overline{WR}$ high to $\overline{ALE}$ low	2		ns
t_{su2}	Setup time from address valid to $\overline{WR}$ high	6		ns
t_{h2}	Hold time from $\overline{WR}$ high to address invalid	5		ns
t_{d3}	Delay time from $\overline{CS}$ low to $\overline{RD}$ low	0		ns
t_{d4}	Delay time from $\overline{RD}$ high to $\overline{CS}$ high	6		ns
t_{w5}	$\overline{RD}$ low width	30		ns
t_{w6}	$\overline{RD}$ high width	13		ns
t_{d5}	Delay time from $\overline{RD}$ low to data valid		30	ns
t_{d6}	Delay time from $\overline{RD}$ high to databus in tristate	0	10	ns
t_{d7}	Delay time from $\overline{WR}$ high to $\overline{RD}$ low	10		ns

(1) All input signals are specified with $t_R = t_F = 5ns$ (10% to 90% of BVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) t_{w2} is obsolete if $\overline{CS}$ stays low between the $\overline{WR}$ and $\overline{RD}$ pulses.

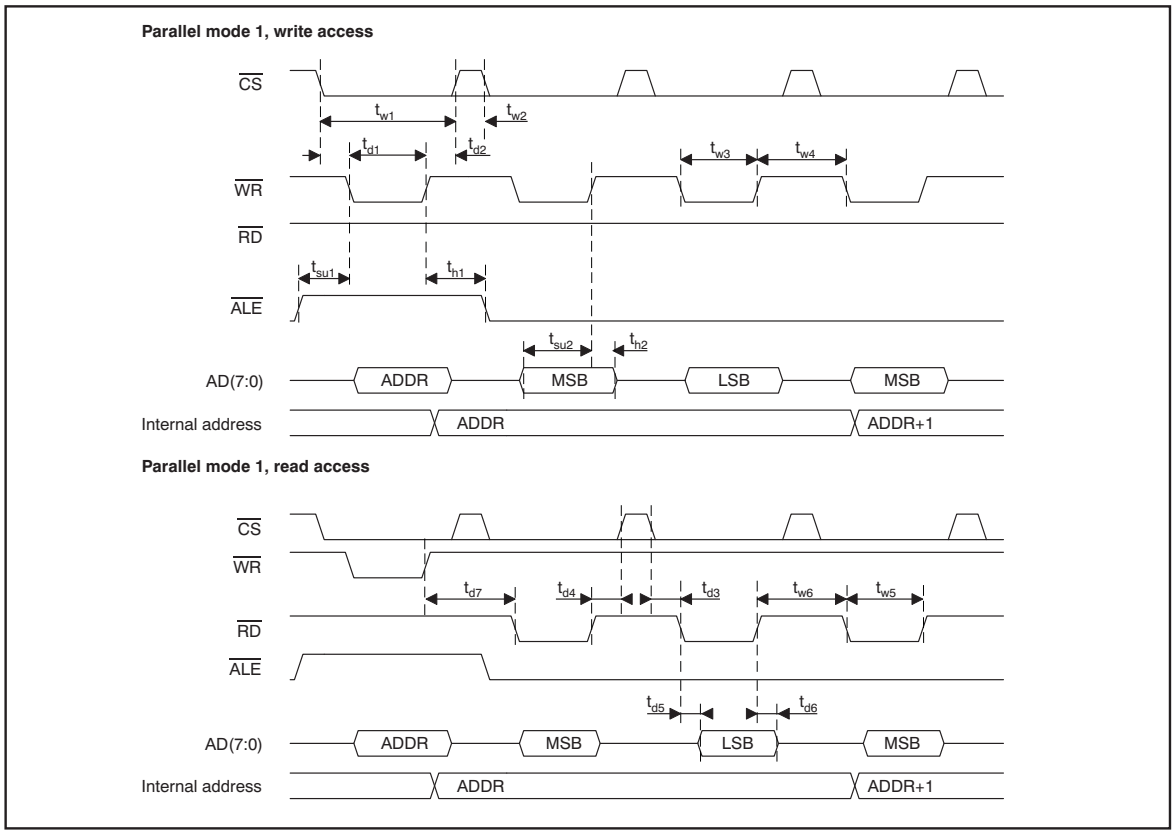

Figure 4. Parallel Mode 1 Timing

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PARALLEL MODE 2

TIMING CHARACTERISTICS(1)

Over recommended operating free-air temperature range at –40°C to +125°C, DVDD = +5V, and BVDD = +2.7V, unless otherwise noted.

PARAMETER(2)		MIN	MAX	UNIT
t_{w1}	$\overline{CS}$ low width	40		ns
t_{w2}	$\overline{CS}$ high width	5		ns
t_{d1}	Delay time from $\overline{ALE}$ low to $\overline{CS}$ high	5		ns
t_{d2}	Delay time from $\overline{WR}$ high to $\overline{CS}$ high	5		ns
t_{d3}	Delay time from $\overline{CS}$ low to $\overline{WR}$ low	3		ns
t_{w3}	$\overline{WR}$ low width	10		ns
t_{w4}	$\overline{WR}$ high width	10		ns
t_{w5}	$\overline{ALE}$ high width	10		ns
t_{d4}	Delay time from $\overline{ALE}$ low to $\overline{WR}$ low	10		ns
t_{su1}	Setup time from address valid to $\overline{ALE}$ low	6		ns
t_{h1}	Hold time from $\overline{ALE}$ low to address invalid	5		ns
t_{d5}	Delay time from $\overline{CS}$ low to $\overline{RD}$ low	0		ns
t_{su2}	Setup time from data valid to $\overline{WR}$ high	6		ns
t_{h2}	Hold time from $\overline{WR}$ high to data invalid	5		ns
t_{d6}	Delay time from $\overline{RD}$ high to $\overline{CS}$ high	6		ns
t_{w6}	$\overline{RD}$ low width	30		ns
t_{w7}	$\overline{RD}$ high width	13		ns
t_{d7}	Delay time from $\overline{RD}$ low to data valid		30	ns
t_{d8}	Delay time from $\overline{RD}$ high to databus in tristate	0	10	ns
t_{d9}	Delay time from $\overline{ALE}$ low to $\overline{RD}$ low	10		ns

(1) All input signals are specified with $t_R = t_F = 5ns$ (10% to 90% of BVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) t_{W2} is obsolete if $\overline{CS}$ stays low between the $\overline{WR}$, $\overline{RD}$ and $\overline{ALE}$ pulses.

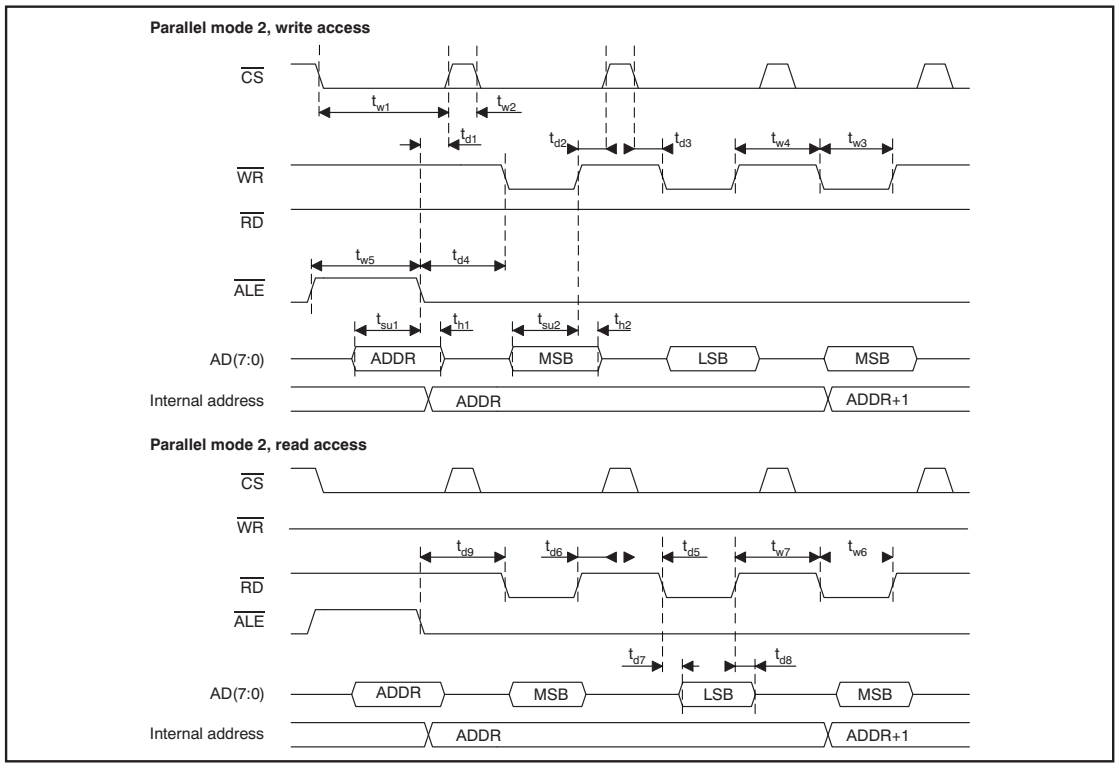

Figure 5. Parallel Mode 2 Timing

PARALLEL MODE 3

TIMING CHARACTERISTICS(1)

Over recommended operating free-air temperature range at –40°C to +125°C, DVDD = +5V, and BVDD = +2.7V, unless otherwise noted.

PARAMETER(2)		MIN	MAX	UNIT
t_{w1}	$\overline{CS}$ low width	40		ns
t_{w2}	$\overline{CS}$ high width	5		ns
t_{d1}	Delay time from $\overline{WR}$ low to $\overline{CS}$ low	5		ns
t_{d2}	Delay time from $\overline{ALE}$ high to $\overline{CS}$ high	5		ns
t_{d3}	Delay time from $\overline{RD}$ high to $\overline{CS}$ high	5		ns
t_{d4}	Delay time from $\overline{CS}$ low to $\overline{RD}$ low	3		ns
t_{w3}	$\overline{RD}$ low width	10		ns
t_{w4}	$\overline{RD}$ high width	30		ns
t_{w5}	$\overline{ALE}$ low width	6		ns
t_{d5}	Delay time from $\overline{ALE}$ high to $\overline{RD}$ low	10		ns
t_{su1}	Setup time from address valid to $\overline{ALE}$ high	5		ns
t_{h1}	Hold time from $\overline{ALE}$ high to address invalid	5		ns
t_{su2}	Setup time from data valid to $\overline{RD}$ high	5		ns
t_{h2}	Hold time from $\overline{RD}$ high to data invalid	5		ns
t_{d6}	Delay time from $\overline{RD}$ low to data valid		30	ns
t_{d7}	Delay time from $\overline{RD}$ high to databus in tristate	0	10	ns
t_{d8}	Delay time from $\overline{WR}$ high to $\overline{CS}$ low	5		ns

(1) All input signals are specified with $t_R = t_F = 5ns$ (10% to 90% of BVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) t_{w2} is obsolete if $\overline{CS}$ stays low between the $\overline{RD}$ and $\overline{ALE}$ pulses.

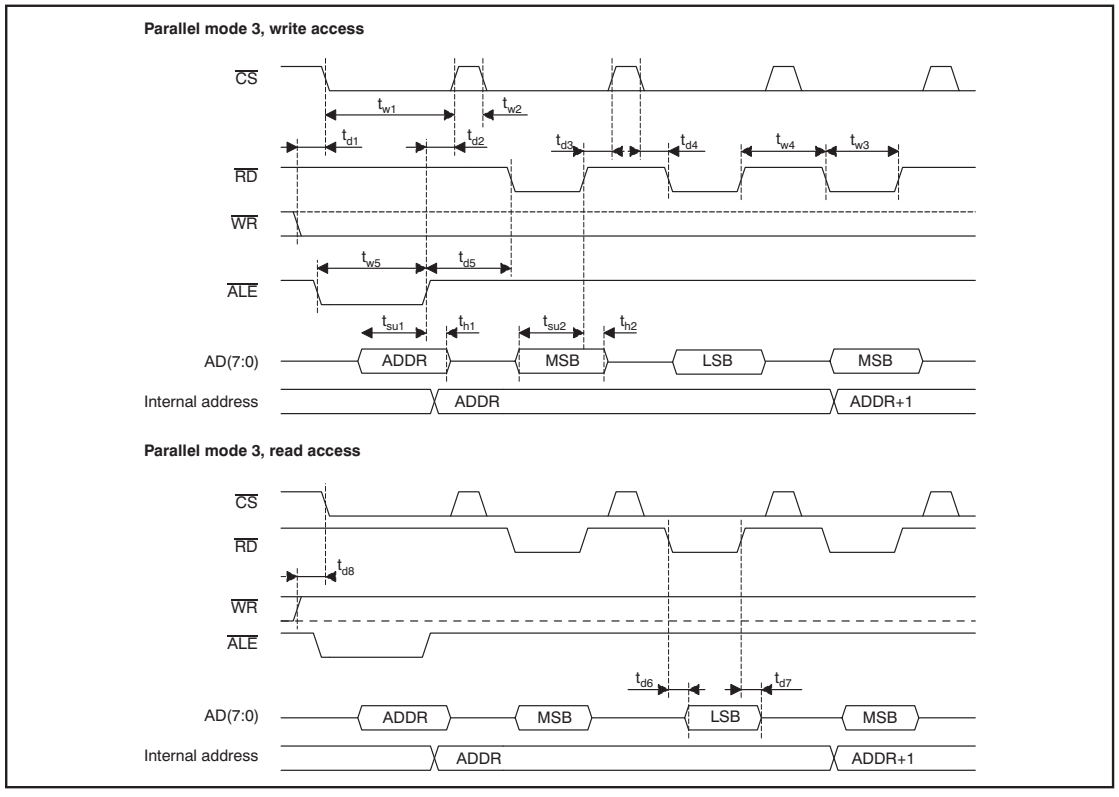

Figure 6. Parallel Mode 3 Timing

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TYPICAL CHARACTERISTICS

At –40°C to +125°C, AVDD, CVDD, DVDD = +5V, and BVDD = +2.7V, unless otherwise noted.
The following condition must be true on the supplies: CVDD ≥ DVDD ≥ BVDD.

FILTER MODULE CURRENT vs TEMPERATURE

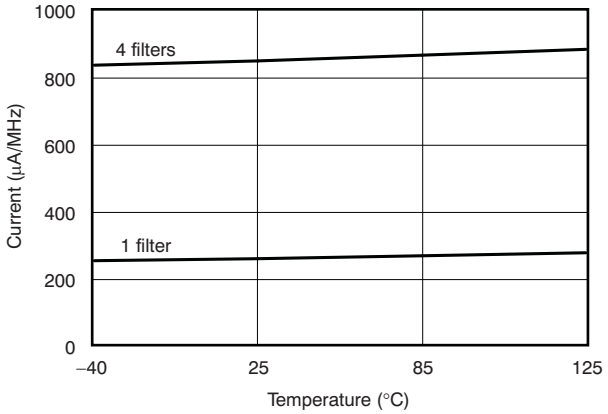

Figure 7.

INTERFACE MODULE CONTROL vs TEMPERATURE

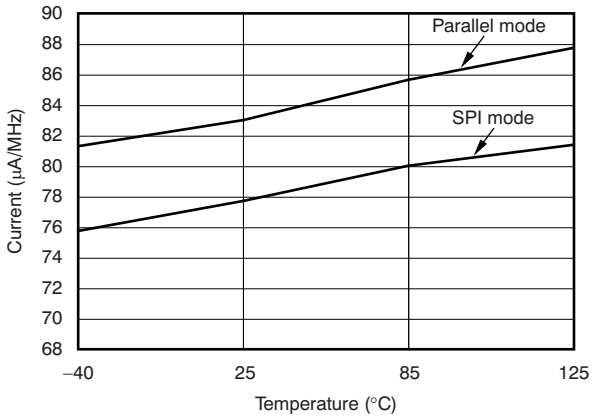

Figure 8.

SIGNAL GENERATOR CURRENT vs TEMPERATURE

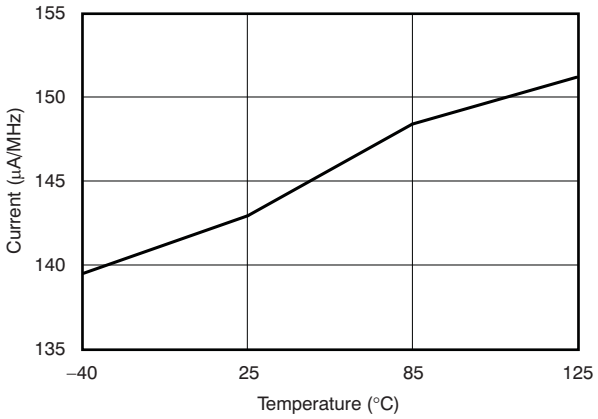

Figure 9.

PWM OUTPUT VOLTAGE vs TEMPERATURE

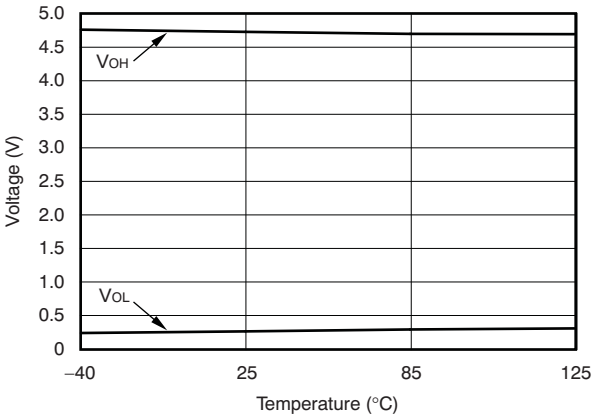

Figure 10.

TYPICAL CURRENT CONSUMPTION vs SUPPLY VOLTAGE

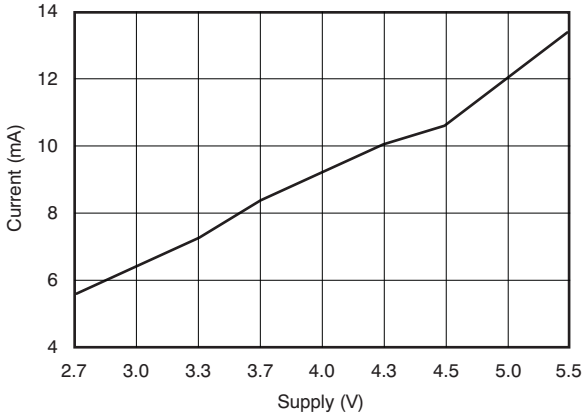

Figure 11.

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THEORY OF OPERATION

Overview

The AMC1210 is a flexible digital filter device specifically designed for motor control applications. It incorporates four independent digital filters into a digital processing block, allowing communication via SPI bus or 8-bit, multiplexed parallel I/O. Each datastream input can be clocked in using an external clock or a clock provided by a delta-sigma modulator. A time measurement unit allows software monitoring of the sample speed and data acquisition, and a comprehensive control and interrupt unit allows real-time monitoring of the AMC1210 status. A digital comparator unit is provided to alert programmable peak conditions on the different datastreams. When used in current measurement applications, the digital comparator unit can alert a system to over- or under-current situations.

Interface Module

The AMC1210 can communicate with digital signal processors (DSPs) or microcontrollers (μCs) in four different interface modes: one serial mode and three 8-bit, multiplexed parallel modes. The serial mode is a standard SPI mode, normally with a 24-bit transfer. The multiplexed parallel modes are designed to work together with a wide range of controllers. Mode pins M0 and M1 determine the mode selection. Table 2 shows the digital interface configuration.

Table 2. Digital Interface Configuration

INTERFACE MODES	PIN M1	PIN M0
SPI	0	0
Parallel Mode 1	0	1
Parallel Mode 2	1	0
Parallel Mode 3	1	1

The digital interface pins perform different functions depending on the interface mode. Table 3 shows the pin operations in different modes.

Table 3. Pin Functions in Different Communication Modes

PIN	SPI MODE	PARALLEL MODE 1	PARALLEL MODE 2	PARALLEL MODE 3
M1	0	0	1	1
M0	0	1	0	1
$\overline{ALE}$	–	Address/Data Select	Address Latch Enable	Address Valid
$\overline{CS}$	Frame sync	Chip Select	Chip Select	Chip Select
$\overline{RD}$	SPI Data In	Read	Read	Strobe
$\overline{WR}$	SPI Clock	Write	Write	Read/Write
AD0	SPI Data Out	Databus 0 (LSB)	Databus 0 (LSB)	Databus 0 (LSB)
AD1	–	Databus 1	Databus 1	Databus 1
AD2	–	Databus 2	Databus 2	Databus 2
AD3	–	Databus 3	Databus 3	Databus 3
AD4	–	Databus 4	Databus 4	Databus 4
AD5	–	Databus 5	Databus 5	Databus 5
AD6	–	Databus 6	Databus 6	Databus 6
AD7	–	Databus 7 (MSB)	Databus 7 (MSB)	Databus 7 (MSB)

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Clock Setup

The clock pin CLK controls the timing of several functions. Table 4 shows the units and features that use the CLK signal for timing.

Table 4. CLK Pin Functions

MODULE/UNIT	FEATURE	CLOCK FUNCTION
Interface/Signal Generator	Signal generator	Determines output data rate
Filter/Input Control	Manchester Decoder in control unit	Allows decoding of Manchester data
	CLKx signal in control unit	Provides timing for CLKx pin when bit CD in the control parameter = '1'
	Clock dividers for CLKx in control unit	Divides CLKx speed
	Modulator failure detection	Allows AMC1210 to monitor input clock CLKx
Filter/Time Measurement	Time measurement	TMU counts number of CLK cycles when TM = 0

If none of the features in this table are needed, the CLK pin should be connected to GND to avoid any increased current consumption.

SPI Mode

The SPI interface runs fully asynchronously to the rest of the system. The four signals of the SPI interface are WR, RD, AD0 and CS. The maximum speed of the SPI interface is 40MHz. When the select signal CS is high, the entire SPI interface is in reset state, except the Address and the Data Register. The SPI clock WR and the serial data input RD are disabled when CS is high. The incoming data is strobed by the SPI interface on the falling edge of the WR. Outgoing data is put on the output AD0 on the rising edge of the WR (see SPI Interface Modes). For a transmission of one 16-bit data word, 24 bits are required. The first incoming bit to the AMC1210 determines if the entire transmission is a read or a write operation. A high bit indicates a read operation, and a low bit indicates a write operation. There are seven address bits. The 16 data bits are transmitted or received after the address bits, according to the sequence shown in Table 5.

Table 5. SPI Write 24-Bit Word Format

A23	A22	A21	A20	A19	A18	A17	A16	MSB A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	LSB A0
R/W	Address							Data															

SPI Option 1

In SPI option 1, one 16-bit transfer is accomplished in the following manner:

1. On the first falling edge of WR, the read/write bit is strobed.
2. On the second falling edge of WR, the MSB of the address (bit 6) is strobed.
3. On the eighth falling edge of WR, the LSB of the address (bit 0) is strobed and the corresponding data of the register map is read.
4. On the ninth rising edge (MSB), the data read from the register map is latched into a shift register and shifted one position each rising edge of the WR. At speeds below 25MHz, it is recommended to perform a read on the next falling edge (Option 1). This data is always sent out, even when a write operation is performed.
5. On the 24th falling edge of WR (LSB), the last data bit is shifted in from RD and a write pulse is generated to write the data into the register map, if a write operation was performed.

Figure 2 and Figure 3 provide detailed timing information for the SPI modes.

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During continuous read or write, the address increments after each read or write. When the address reaches 7Fh, the address counter starts over from 0. The data is written into the register map on the 16th $\overline{WR}$ of a data word. If the $\overline{CS}$ is inactive before the 16th $\overline{WR}$ in a data word, the data is not written into the register map; the data is lost. Figure 12 shows a typical example of this functionality.

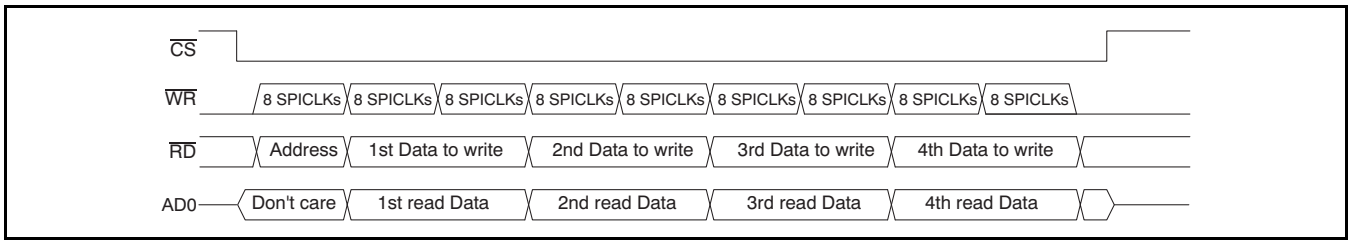

Figure 12. Typical Serial Communication Operation

SPI Option 2

SPI option 2 is recommended for use when the clock speed is greater than 25MHz. The only difference between option 1 and 2 is the edge from which the output data is strobed. In option 2, the user should read the data on the rising edge after the data from the register map is latched (one half clock cycle after Option 1). In this case, an extra clock cycle is needed (25 clock cycles instead of 24). See the timing diagram in Figure 3.

Parallel Mode 1

In Parallel Mode 1, the host port uses $\overline{WR}$ and $\overline{RD}$ for independent write and read access to the AMC1210. The current cycle is processed only when the $\overline{CS}$ input of the AMC1210 is low. $\overline{RD}$ indicates to the AMC1210 that the host processor has requested a data transfer. The AMC1210 then outputs data to the host.

To configure the registers in the AMC1210, the host process issues a $\overline{WR}$ signal to indicate that valid data is available on the bus. The data is latched into the AMC1210 with the rising edge of the $\overline{WR}$. The address for the AMC1210 must be valid at the first rising edge of $\overline{WR}$. To indicate that an address is issued, the signal $\overline{ALE}$ must be set to high before the $\overline{WR}$ signal is set to low. The $\overline{CS}$ signal can stay low between two consecutive writes or reads.

Figure 4 provides a detailed timing diagram of Parallel Mode 1.

Parallel Mode 2

In Parallel Mode 2, the host port uses $\overline{WR}$ and $\overline{RD}$ for independent write and read access to the AMC1210. The current cycle is processed only when the $\overline{CS}$ input of the AMC1210 is low. $\overline{RD}$ indicates to the AMC1210 that the host processor has requested a data transfer. The AMC1210 then outputs data to the host.

To configure the AMC1210 registers, the host process issues a $\overline{WR}$ signal to indicate that valid data is available on the bus. With the rising edge of $\overline{WR}$, the data is latched into the AMC1210. The address is latched into AMC1210 when the signal $\overline{ALE}$ is set to low. The $\overline{CS}$ signal can stay low between two consecutive writes or reads.

Figure 5 provides a detailed timing diagram of Parallel Mode 2.

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Parallel Mode 3

In Parallel Mode 3, the host port uses $\overline{RD}$ and $\overline{WR}$ for write and read access to the AMC1210. The current cycle is processed only when the $\overline{CS}$ input of the AMC1210 is low. $\overline{WR}$ indicates to the AMC1210 that the host processor has initiated a read or write transfer. If $\overline{WR}$ is high, the AMC1210 outputs data to the host when $\overline{RD}$ is also low.

To configure the registers in the AMC1210, the host process issues a $\overline{RD}$ signal together with $\overline{WR}$ low to indicate that valid data is available on the bus. With the rising edge of the $\overline{RD}$ signal, the data is latched into the AMC1210. The address is latched into AMC1210 when the signal ALE is set high. The $\overline{CS}$ signal can stay low between two consecutive writes or reads.

Figure 6 provides a detailed timing diagram of Parallel Mode 3.

In all parallel modes, each address can be accessed sequentially without writing a new address to the AMC1210. When an address is set by the user, a pointer is also set to that address. After each successive read or write operation, the address is incremented by one in the register map.

FILTER MODULE

The filter module consists of the control block unit, the comparator filter unit, the sinc filter unit, a time measurement unit and a demodulator/integrator unit. Each unit can be individually programmed for several different modes of operation. Figure 13 shows a block diagram of one filter module. The four filter modules are identical and are able to be configured independently.

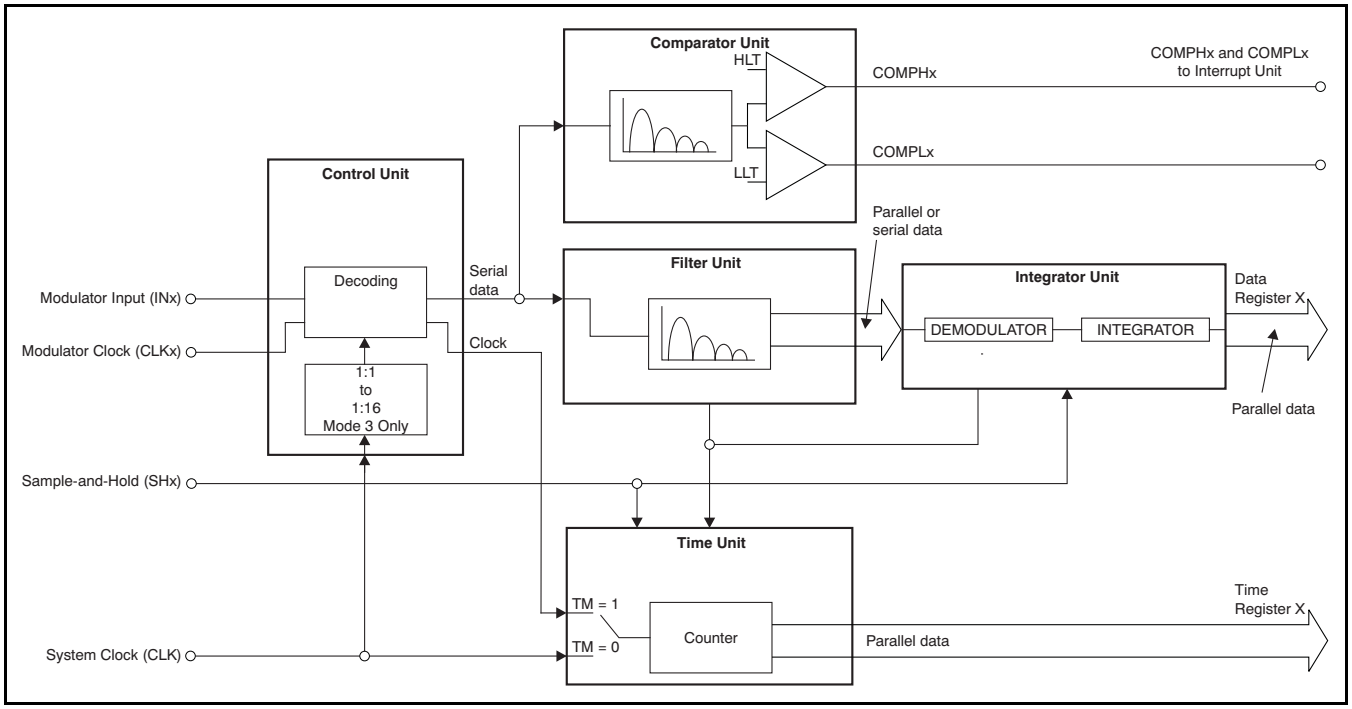

Figure 13. AMC1210 Filter Module

Control Unit

The control unit translates the modulator input data and the corresponding clock so that it can be used by the AMC1210. Four input options are available, depending on the mode of the modulator. These options are selected through the bits MOD1 and MOD0 in the Control Parameter Register. Table 6 describes each input mode. A detailed diagram of the timing of each of these modes can be found in the Timing Characteristics section; see Figure 1.

Table 6. Interface Modes

MODULATOR MODE	MOD1	MOD0	DESCRIPTION
0	0	0	The modulator clock is running with the modulator data rate. The modulator data is strobed at every rising edge of the modulator clock.
1	0	1	The modulator clock is running with half of the modulator data rate. The modulator data is strobed at every edge of the modulator clock.
2	1	0	The modulator clock is off and the modulator data is Manchester-encoded.
3	1	1	The modulator clock is running with double of the modulator data rate. The modulator data is strobed at every other positive modulator clock edge.

In Modulator Mode 2, the data is Manchester-encoded. An automatic calibration is continuously performed to achieve optimum decoding performance. The status of this calibration can be checked in the Control Parameter Register bits MS10–MS0 and in the Status Register bits MALx and MAFx. The clock input CLKx is ignored in this mode.

Input Clocking

The filter module clock is separate from the system clock (except when using Modulator Mode 3). This design permits the filter module to run asynchronously from the control module, allowing two different speeds for input data and control block timing. The clock setup is different for each input mode. See Table 7.

Table 7. Clock Operation in Each Interface Mode

INPUT MODE	CLOCK FUNCTIONALITY
0	The clock for the filter module is fed by the CLKx input, which can be either external or driven by the modulator. The frequency is the same.
1	Each edge of CLKx generates a pulse, which clocks the filter module.
2	The clock for the filter module is generated by the Manchester decoder.
3	The clock source is the system clock, from the CLK pin. This clock can be divided down by a programmed number between 1 and 8 by bits MD2–MD0 in the Clock Divider Register. This clock can also be fed to the CLKx pin to drive the modulator clock if the bit CD in the Control Parameter Register is set to '1'.

Note that as long as the input data is clocked in correctly, all of the filter module functions (sinc filter unit, comparator unit, etc.) will be clocked at the same rate.

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Manchester Decoding

Manchester signaling is a method of encoding a data signal in such a way that it can be retrieved without the need of a separate clock line. When configured in Mode 2, the AMC1210 can translate a Manchester-encoded signal on the INx pin into a clock signal and a data signal. An automatic calibration is continuously performed to optimize the decoding of the data.

The calibration mechanism follows this sequence:

1. The modulator data is sampled at the frequency of the system clock (CLK).
2. The number of CLK cycles between transitions is counted and recorded for 1024 consecutive transitions.
3. The resulting array will have a '1' in the bit location that corresponds to the number of CLK cycles counted between transitions. For example, the sequence shown in Table 8 means that there was at least one instance where three and four, as well as seven and eight, CLK cycles occurred between two transitions. This array is stored in the bits MS10–MS0 in the Control Parameter Register.
4. An algorithm looks for a group of zeros that has ones before and after it. If this pattern is not found, the bits MALx and MAFx in the Status Register are set high.
5. If the algorithm is successful, it will use the location of the first '0' as the number of CLK cycles needed to determine the frequency and which transitions are valid in the Manchester code.
6. The algorithm starts over from Step 2 automatically.

Table 8. Example Control Parameter Register

VALUE	0	0	0	1	1	0	0	1	1	0	0
BIT	MS10	MS9	MS8	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0
CLK CYCLES	11	10	9	8	7	6	5	4	3	2	1

The MALx bit shows the status of the previous Manchester decoder calibration cycle. If it is high, the decoder calibration has failed on the previous calibration cycle. The MAFx bit shows if any failures have occurred since the last read of the Status Register. Any MALx failure will cause MAFx to go high. MAFx is reset to low when the Status Register is read.

The decoding procedure is performed continuously when the AMC1210 is configured for Modulator Mode 2. Note that the CLK frequency must be at least six times the Manchester data rate for the decoder to perform properly.

Comparator Unit

An independent comparator unit allows the user to monitor input conditions with a fast settling time without sacrificing input measurement resolution. The filter of the comparator unit is similar to the sinc filter unit, with OSR values ranging continuously between 1 and 32. Setting the OSR to 32, a maximum 15-bit output width of 32,768 can be achieved. The output of the filter is compared with two programmed threshold levels to detect over- and under-value conditions. These threshold levels are programmed in the high and low level Threshold Registers for each individual filter module. When an over- or under-value condition occurs, it signals the interrupt unit to set an interrupt signal and store the conditions in the Interrupt Register. The Interrupt Register can then be polled to see which condition caused the interrupt signal. It is not possible to read out the value of the comparator filter.

This filter, together with the comparators, is generally used to detect over-currents. It is necessary to decide on an OSR given the desired resolution/settling time combination. This programming will be discussed in more detail in the Applications Information section.

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The comparator filter unit and the sinc filter unit differ in the way they handle input data. The comparator filter unit translates a low input signal to a '0' and a high input signal to a '1', whereas the sinc filter unit uses '–1' and '1'. The resulting calculations give only positive values for the output of the comparator filter. The data representation is straight binary. Table 9 and Figure 14 show the different full-scale values that the comparator filter can store using different oversampling ratios.

Table 9. Peak Data Values for Different OSR/Filter Combinations

OSR	Sinc^1	Sinc^2	Sinc^3	Sincfast
x	0 to x	0 to x^2	0 to x^3	0 to $2x^2$
4	0 to 4	0 to 16	0 to 64	0 to 32
8	0 to 8	0 to 64	0 to 512	0 to 128
16	0 to 16	0 to 256	0 to 4096	0 to 512
32	0 to 32	0 to 1024	0 to 32,768	0 to 2048

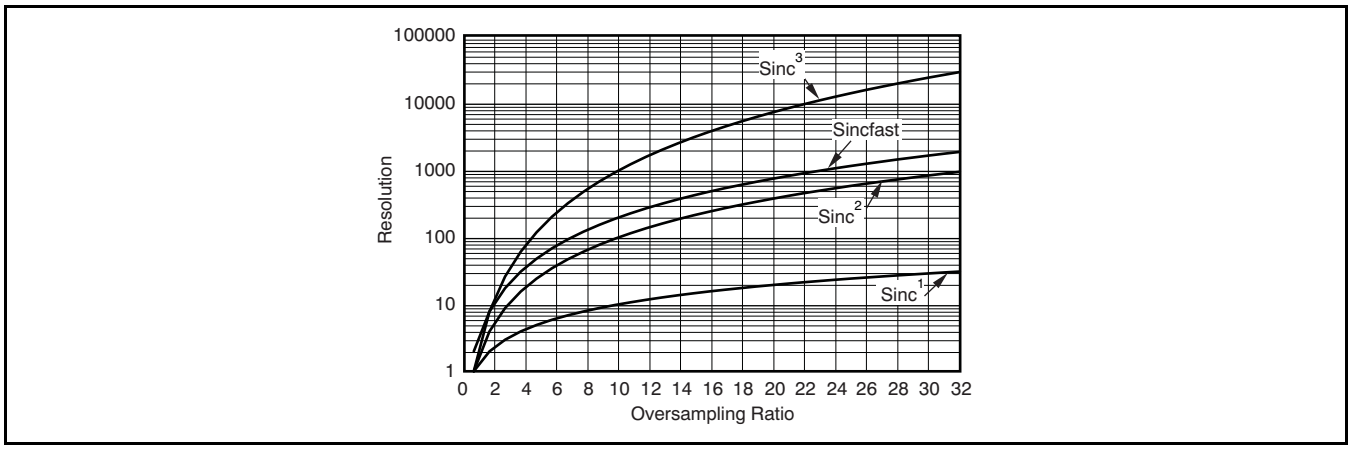

Figure 14. Comparator Filter Resolution

The maximum resolution yields the peak values in Table 9 (15 bits binary, 32,768 decimal). Note that in order to achieve the maximum value, the delta-sigma modulator is operated at absolute maximum positive or negative full-scale, which is outside of the recommended full-scale range of 80% of most delta-sigma modulators.

Sinc Filter Unit

The AMC1210 utilizes a standard integration/decimation/differentiation scheme to achieve the sinc filter. It can be configured as a Sinc^1, Sinc^2, Sinc^3 or Sincfast filter with oversampling ratios (OSRs) continuously between 1 and 256. Figure 15 illustrates the frequency response of each type of filter.

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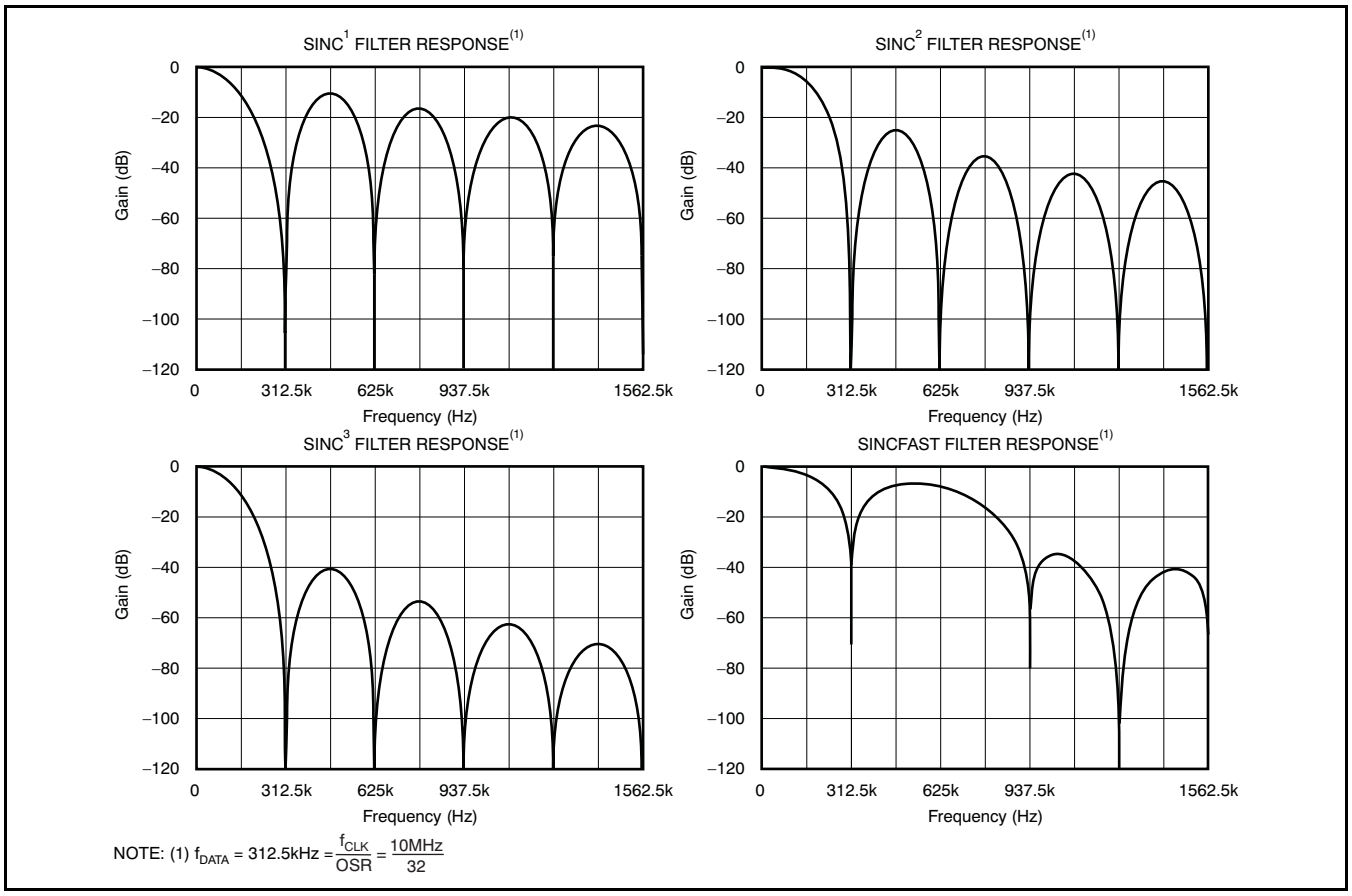

Figure 15. AMC1210 Frequency Responses with Various Sinc Filters

These figures show the digital filter frequency response for one oversampling ratio (SOSR = 32) and a modulator rate of 10MHz.

The general purpose of the digital filter is to average the input modulator data. Achieving higher resolution requires additional samples for averaging, thereby increasing the total samples necessary to accurately represent an abrupt change. It also requires additional clock cycles to complete a single sample. The ratio of clock cycles to output samples is controlled by the SOSR value (the oversampling ratio for the sinc filter unit) in the Sinc Filter Parameter Register. Table 10 and Figure 16 show the maximum resolution given different filter structures and SOSR values.

Table 10. Peak Data Values for Different SOSR/Filter Combinations

SOSR	Sinc^1	Sinc^2	Sinc^3	Sincfast
x	x	x^2	x^3	$2x^2$
4	–4 to 4	–16 to 16	–64 to 64	–32 to 32
8	–8 to 8	–64 to 64	–512 to 512	–128 to 128
16	–16 to 16	–256 to 256	–4096 to 4096	–512 to 512
32	–32 to 32	–1024 to 1024	–32,768 to 32,768	–2048 to 2048
64	–64 to 64	–4096 to 4096	–262,144 to 262,144	–8192 to 8192
128	–128 to 128	–16,384 to 16, 384	–2,097,152 to 2,097,152	–32,768 to 32,768
256	–256 to 256	–65,536 to 65,536	–16,777,216 to 16,777,216	–131,072 to 131,072

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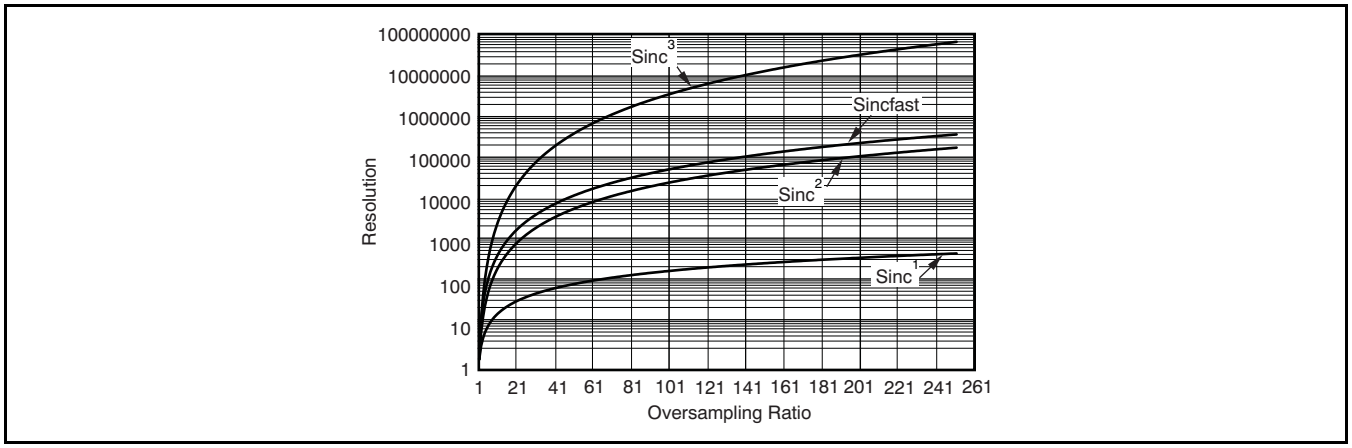

Figure 16. Sinc Filter Resolution

The sinc filter has a bit width of 25 bits and a signed two's complementary data representation. The maximum possible resolution gives a 26-bit word (±16,777,216). Note that this value is only reached if the delta-sigma modulator is operated at absolute maximum positive or negative full-scale, which is beyond the recommended full-scale range of 80% of most delta-sigma modulators. This value also does not represent the resolution of the signal. The signal resolution is determined by the modulator, and increasing the filter bit width will not offer any improved noise performance beyond the modulator capabilities.

Figure 17 shows how a typical application would use the digital filter. When the filter is enabled, it is continuously processing data and generating output words. When an output word is ready to read, the processor is first triggered by a rising edge on the ACK pin. Then the Interrupt Register is read to check which filter module generated new data. Once all valid data registers have been read, the ACK pin goes low.

The data registers can be up to 32 bits.

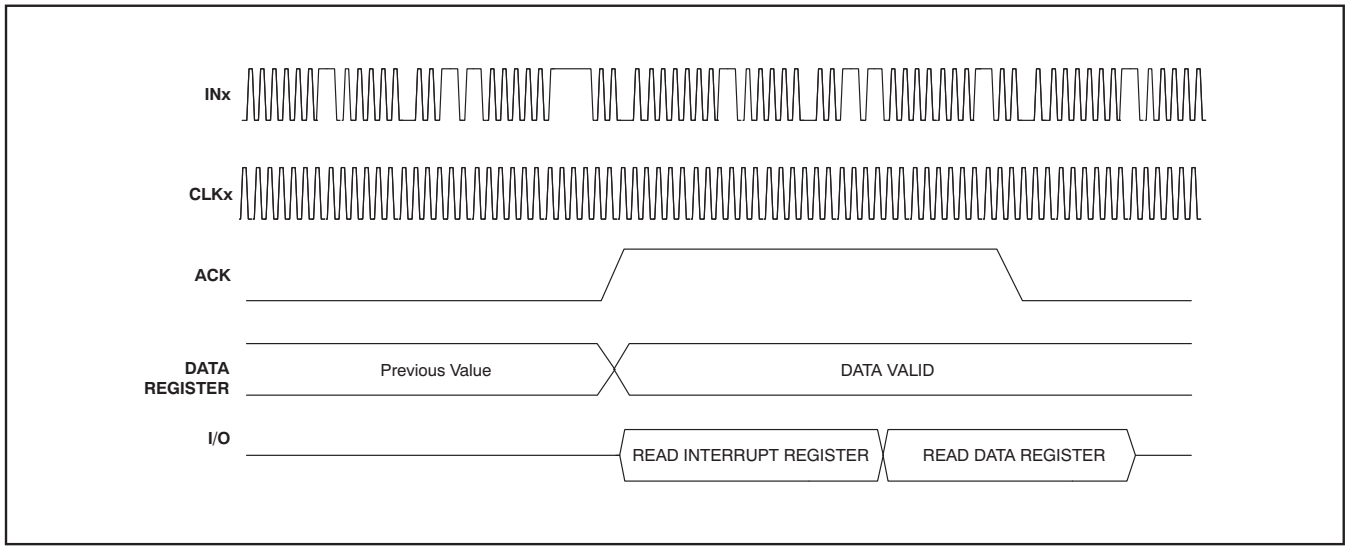

Figure 17. Typical Data Read Sequence

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Integrator Unit

The integrator allows digital integration (summation) of the filter output data or the direct modulator input data when the sinc filter unit is bypassed. It consists of a parameterized integrator and a data shift unit. The integrator is a simple 32-bit binary two's complement accumulator. The time of integration is determined by either the IOSR value or an external sample-and-hold signal. The bit IMOD in the Integrator Parameter Register determines which mode is used.

The integrator is enabled by setting the bit IEN in the Integrator Parameter Register to high. When IEN is low, the integrator is disabled, reset, and bypassed.

The input to the integrator is fed by the sinc filter unit. This can be adjusted to allow the input to feed directly into the integrator. See Bypassing the Sinc Filter Unit.

Sample-and-Hold Mode (IMOD = 1)

If Sample-and-Hold Mode is selected, the SHS bit in the Control Parameter Register determines which sample-and-hold signal is used to determine the total integration time. When a rising edge occurs on the selected sample-and-hold pin, the resulting integrator value is stored in the Data Register and the integrator is reset.

Oversampling Mode (IMOD = 0)

In Oversampling Mode, the integrator sums a preset number of samples from the sinc filter unit, determined by an oversampling ratio value (IOSR) in the Integrator Parameter Register. The integrator can be configured with oversampling ratios continuously between 1 and 128. The integrator is sampled at the data output rate of the sinc filter unit. Table 11 shows the different full-scale values that the integrator can store with different oversampling ratios, assuming that the sinc filter unit is set to SOSR = 256 at the full-scale output.

Table 11. Peak Data Values for Different IOSR Values

IOSR	INTEGRATOR OUTPUT MAX (with a Sinc^3 Structure)
x	–(SOSR^3)(x) to (SOSR^3)(x)
4	–67,108,864 to 67,108,856
8	–134,217,728 to 134,217,712
16	–268,435,456 to 268,435,424
32	–536,870,912 to 536,870,848
64	–1,073,741,824 to 1,073,741,696
128	–2,147,483,648 to 2,147,483,648

The start of an integrator cycle in Oversampling Mode is controlled by the sinc filter unit. A new integrator cycle is started when the sinc filter is enabled. The bit MFE in the Clock Divider Register can be used to synchronize the integrator unit in all four of the filter modules. Following the rising edge of the MFE bit, the integrator will begin to accumulate data in all four modules. When the same data output rate is used on all sinc filters, synchronous timing is achieved.

Integrator Overflow

Meeting or exceeding the maximum values will trigger an integrator overflow (IOx goes high). This overflow condition is only possible in Oversampling Mode when the sinc filter is set to a Sinc^3 structure and it outputs only full-scale values.

In Sample-and-Hold Mode, the integrator flag will go high if the maximum integrator value is exceeded (–2,147,483,648 or 2,147,483,648). This event will occur if the sample-and-hold signal SHx is held in the active state longer than the overflow time.

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Equation 1 calculates the time it takes for the integrator to overflow:

$$t_{OVERFLOW} = \frac{(INT_{MAX} \cdot SOSR)}{(FILT_{OUT} \cdot f_{INPUT})} \quad (1)$$

where:

- INT_{MAX} = the maximum integrator value (–2,147,483,648 if $FILT_{OUT}$< 0, 2,147,483,648 otherwise)
- $FILT_{OUT}$ = Average Sinc filter output value (from $–FILT_{MAX}$ to $+FILT_{MAX}$; see Table 10)
- SOSR = oversampling ratio of the Sinc filter
- f_{INPUT} = modulator data rate

For example, if the sinc filter outputs an average code value of 100,000 at a rate of 39.06kHz (f_{INPUT} = 10.0MHz/SOSR = 256), it will take 549.8ms for an integrator overflow flag to occur.

When integrator overflow occurs, the integrator value is reset and integration continues.

16-Bit Data Shifting

If 16-bit data representation is chosen (DR is low), the shift control bits SH in the Integrator Parameter Register control which 16-bit part of a 32-bit data word is sent to the register map. The shift control bits are the number of left shifts in the 32-bit data word to achieve the maximum 16-bit value range. For example, if the sinc filter runs with a $Sinc^3$ structure and an oversampling ratio of 256, the data values will be in the range of –16,777,216 to 16,777,216. To get a maximum 16-bit range of –32,767 to 32,767, the shift control bits should be set to 9. In this case, 9 LSBs of the 25-bit word are lost. The sign bit is not affected by the shift, which means the sign is always correct, regardless of the shift control bits.

Table 12 shows an example. The first column shows the original 32-bit word, the second column shows the SH bits value, and the last column shows which bits of the 32-bit word will be output in 16-bit mode.

Table 12. 16-Bit Representation Example

32-BIT WORD	SH VALUE	16-BIT REPRESENTATION
b31–b0	1	b16–b1
	9	b24–b9
	14	b29–b14

Bypassing the Sinc Filter Unit

If the integrator is used without the sinc filter unit, the bit FEN has to be set high, the sinc filter structure has to be set to $Sinc^1$, and the sinc filter OSR has to be set to '1'. In this case, the integrator will sum the direct input data from the modulator.

Demodulation

Obtaining the resolver position from the AM-modulated resolver input signal requires mathematical demodulation. This calculation is performed by the AMC1210 after phase calibration. Modulation is enabled by setting the DEN bit in the Integrator Parameter Register high. For more information, see the Signal Generator Unit description and the Applications Information.

Time Measure Unit

The time measure unit provides two modes of measuring times, depending on the TM bit in the Control Parameter Register. A counter is implemented in the time measure unit that counts clock cycles from the modulator clock input or the system clock.

The maximum measured time, t_{MAX}, is calculated with the formula shown in Equation 2. f_{CLK} is either the modulator clock speed or the system clock speed.

$$t_{MAX} = \frac{65536}{f_{CLK}} \quad (2)$$

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Mode 1 (TM = 1)

In Mode 1, the time measure unit updates the Time Register with the elapsed amount of incoming modulator clock cycles between two rising edges of the selected sample-and-hold signal (selected by the SHS bit of the Control Parameter Register). This mode can be used to measure the speed of the modulator clock or determine the number of input bits that have been clocked into the filter module. Each time a positive edge of the selected sample-and-hold is detected, the Time Register will be updated with the time counter value, and the time counter will be reset. Figure 18 shows an example of a typical functional timer sequences in Mode 1.

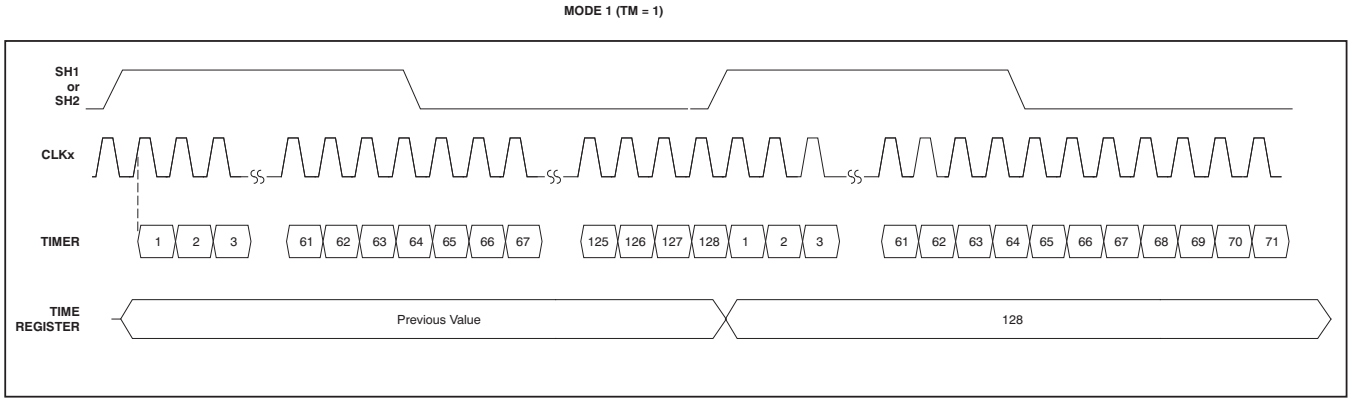

Figure 18. Typical Functional Timer Sequence, Mode 1 (TM = 1)

Mode 2 (TM = 0)

In Mode 2, the time measure unit updates the Time Register with the elapsed amount of system clock cycles from the last available data to the next rising edge of the selected sample-and-hold signal. Each time data is available, that is, when the sinc filter or the integrator has new data, the timer will reset. The timer continuously counts when a rising edge of the selected sample-and-hold signal occurs. At this point, the Time Register is updated with the time counter value, and the time counter will be reset. Figure 19 shows an example of a typical functional timer sequence in Mode 2.

Since the Time Register is a 16-bit register, the maximum time measured is 65,536 clock cycles. The bit TOx in the Status Register is set to high when the time counter receives an overflow (that is, when the counter changes from 0xFFFF to 0x0000). This status bit is reset when the Status Register is read.

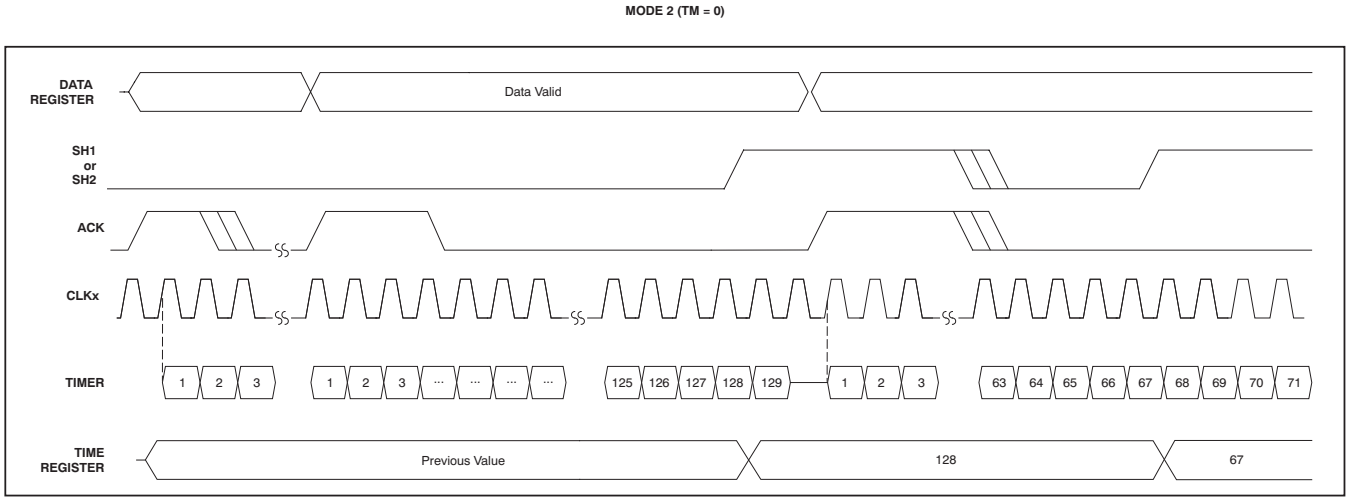

Figure 19. Typical Functional Timer Sequence, Mode 2 (TM = 0)

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CONTROL AND INTERRUPT MODULE

The control and interrupt module consists of a Signal Generator unit, a comprehensive interrupt unit and a register map. The register map contains all control parameters, output data and status bits for the AMC1210. A detailed description of each register is available in the Register Map section.

Signal Generator Unit

The signal generator (see Figure 20) provides a 5V Pulse Width Modulated (PWM) signal at pin PWM1 and a complementary signal at PWM2. The output of PWM1 to PWM2 is a 5V differential signal that can be externally low-pass-filtered to generate a carrier signal with a predefined clock frequency.

The signal generator is a shift register with a length between 1 and 1024. The shift register is programmed through the Pattern Register (bits SP). On the first write command to the bits SP, the first 16 bits of the shift register are loaded. Each following write command causes the data in the shift register to shift 16 bits *upwards*, and the 16 bits from the Pattern Register are placed in the LSBs of the shift register. For example, if 874 bits of predefined pattern are to be stored in the shift register, 55 writes to the Pattern Register must be issued (with MSB first and LSB last), and the value 873 must be written into the bits PC in the Control Register.

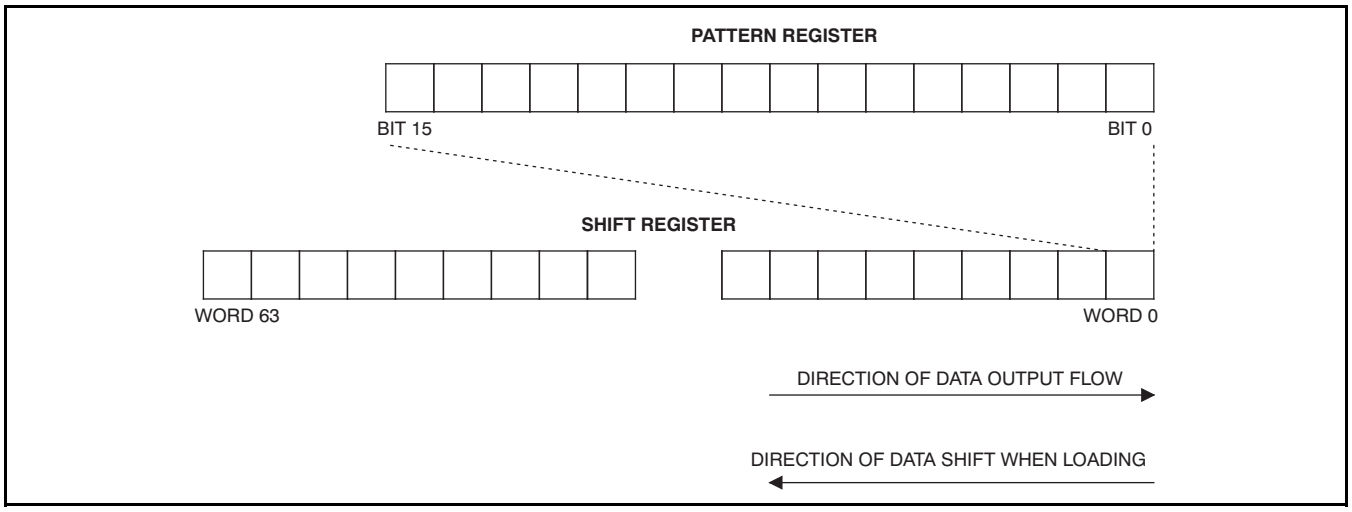

Figure 20. AMC1210 Signal Generator Unit

The output data rate of the signal generator is programmed with the Clock Divider Register (bits SD). The output data rate can be selected to be an integer division of the CLK rate. For example, if the CLK pin is operating at 40MHz with the bits SD = 4, the bit rate of the signal generator is 10MHz. The length of the pattern can be programmed with the Control Register (bits PC). A length can be chosen between 1 and 1024 bits. This signal is designed for use as the carrier frequency in resolver applications, where proper demodulation requires a completely synchronous clock to the carrier timing.

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Calibrating the Signal Generator

The Signal Generator unit also must be in phase with the total system for resolver demodulation. This condition requires a calibration to align the phase of the Signal Generator output to the sinc filter output. The phase calibration begins when the bit PCAL in the Clock Divider Register is set high. The AMC1210 performs the calibration by monitoring the polarity of both the output of the signal generator and the sinc filter. Once the polarities are defined, a demodulation signal is generated with the corresponding phase shift.

The bit PCAL controls demodulation. Initially, it is set high. The AMC1210 then outputs a low on bit PCAL when the modulation is performed correctly. The microcontroller can monitor the calibration by reading PCAL. The first calibration attempt will try to calibrate for one period of the Signal Generator. If PCAL stays high after that period, then calibration has failed. In order to restart calibration, a low must be written to PCAL in order to reset the PCAL state. Writing a subsequent high starts the calibration over.

Driving a Signal with the Signal Generator

The resolver can be driven directly from the AMC1210. If the bit HBE is set to high, the pins PWM1 and PWM2 are capable of driving 100mA directly into the resolver coils. If bit HBE = 0, the drive capability is lowered.

The pattern generator is enabled by the bit SGE in the Clock Divider Register.

Interrupt Unit

Figure 21 shows the structure of the interrupt unit.

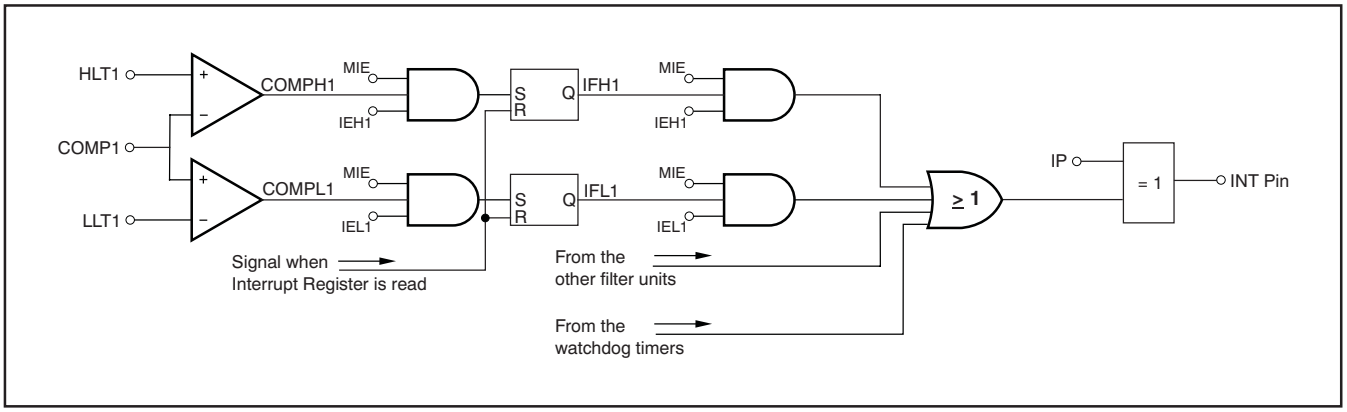

Figure 21. AMC1210 Interrupt Unit

Each comparator output is one interrupt source (COMPHx or COMPLx) creating eight total comparator outputs in the AMC1210. Each of these eight interrupt sources is stored in a flag register (IFHx or IFLx), if the master interrupt enable (MIE) and the appropriate interrupt enable (IEHx or IELx) are set to high. This flag register will be set to high if an interrupt is issued. This flag will be reset if the Interrupt Register is read and the interrupt source is no longer active. If an interrupt source is still active when the Interrupt Register is read, the appropriate flag and the INT pin will remain set. Figure 22 illustrates an example of the interrupt behavior depending on the value of the threshold registers and the corresponding read access to reset the interrupt flag.

If the modulator clock is failing (when the modulator clock is slower than 1/64th of the system clock CLK), a watchdog timer will set a flag MFx, if the appropriate modulator flag interrupt enable bit (MFIEx) and the master interrupt enable (MIE) is set. If the modulator clock is still failing when the Interrupt Register is read, the appropriate flag remains set. The flag clears if the fail condition is no longer true, and the Interrupt Register is read.

Any of the 12 interrupt bits will activate the interrupt pin INT, if enabled. The polarity of the INT pin can be chosen with the Interrupt polarity control bit (IP) in the Control Register.

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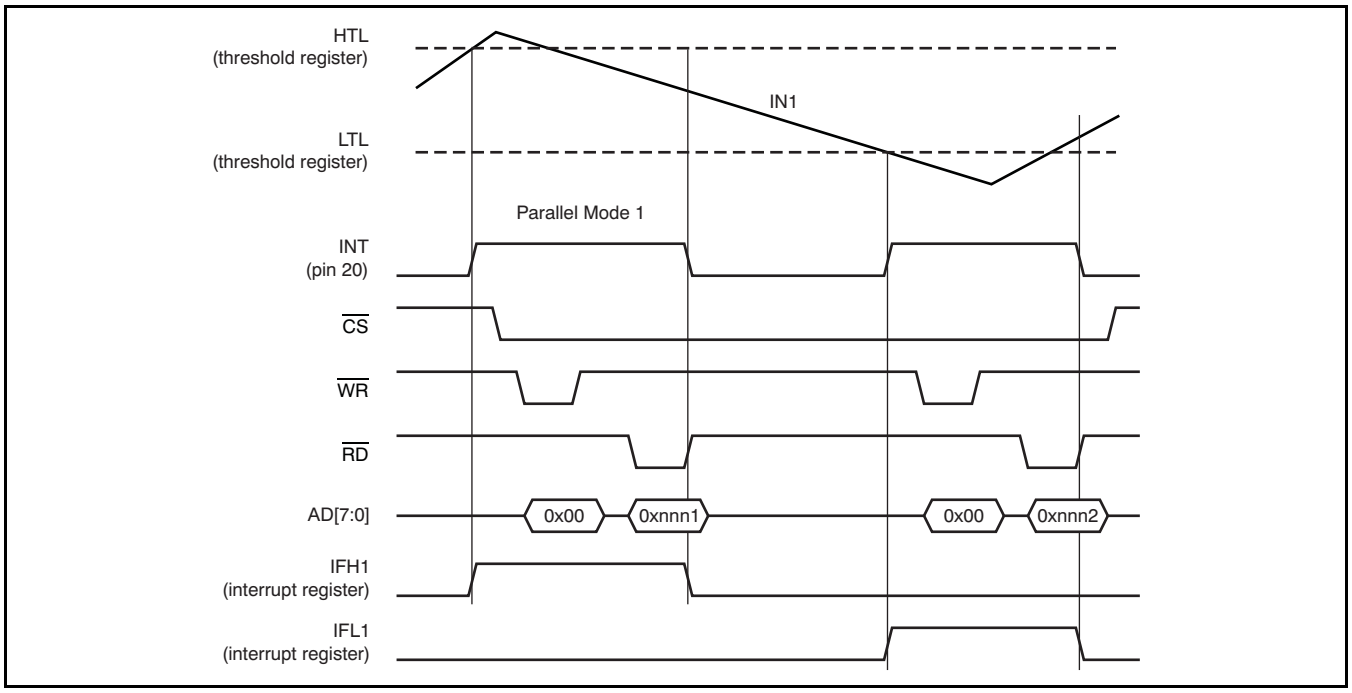

Figure 22. Interrupt Behavior

Acknowledge

The acknowledge pin ACK indicates that new data is available from one of the filter modules. When the acknowledge pin goes high, new data is available in one or more of the Data Registers. By reading the Interrupt Register, the filter module with new data can be determined. When one Data Register is read, the appropriate acknowledge flag in the Interrupt Register will be reset; when all flags are reset, the acknowledge pin is reset to low. The acknowledge pin can be inverted if the acknowledge polarity control bit (AP) in the Control Register is set high. The acknowledge flags cannot be set if both the sinc filter and the integrator are disabled. Each acknowledge flag can be disabled if the Acknowledge Enable control bit (AE) in the appropriate Sinc Filter Parameter Register is set to low. The acknowledge flag is not set when the oversampling rates of the sinc filter and the integrator are both set to '1'.

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REGISTER MAP

	ADDRESS	RESET VALUE	NAME
	0x00	0x0000	Interrupt Register
Filter Module 1	0x01	0x0000	Control Parameter Register for Filter Module 1
	0x02	0x0000	Sinc Filter Parameter Register for Filter Module 1
	0x03	0x0000	Integrator Parameter Register for Filter Module 1
	0x04	0x7FFF	High-level Threshold Register for Filter Module 1
	0x05	0x0000	Low-level Threshold Register for Filter Module 1
	0x06	0x0000	Comparator Parameter Register for Filter Module 1
Filter Module 2	0x07	0x0000	Control Parameter Register for Filter Module 2
	0x08	0x0000	Sinc Filter Parameter Register for Filter Module 2
	0x09	0x0000	Integrator Parameter Register for Filter Module 2
	0x0A	0x7FFF	High-level Threshold Register for Filter Module 2
	0x0B	0x0000	Low-level Threshold Register for Filter Module 2
	0x0C	0x0000	Comparator Parameter Register for Filter Module 2
Filter Module 3	0x0D	0x0000	Control Parameter Register for Filter Module 3
	0x0E	0x0000	Sinc Filter Parameter Register for Filter Module 3
	0x0F	0x0000	Integrator Parameter Register for Filter Module 3
	0x10	0x7FFF	High-level Threshold Register for Filter Module 3
	0x11	0x0000	Low-level Threshold Register for Filter Module 3
	0x12	0x0000	Comparator Parameter Register for Filter Module 3
Filter Module 4	0x13	0x0000	Control Parameter Register for Filter Module 4
	0x14	0x0000	Sinc Filter Parameter Register for Filter Module 4
	0x15	0x0000	Integrator Parameter Register for Filter Module 4
	0x16	0x7FFF	High-level Threshold Register for Filter Module 4
	0x17	0x0000	Low-level Threshold Register for Filter Module 4
	0x18	0x0000	Comparator Parameter Register for Filter Module 4
	0x19	0x0000	Control Register
	0x1A	0x0000	Pattern Register
	0x1B	0x0000	Clock Divider Register
	0x1C	0x0000	Status Register
Data/Time Output	0x1D	0x0000/0x00000000 (1)	Data Register for Filter Module 1 (1)
	0x1E	0x0000	Time Register for Filter Module 1
	0x1F	0x0000/0x00000000 (1)	Data Register for Filter Module 2 (1)
	0x20	0x0000	Time Register for Filter Module 2
	0x21	0x0000/0x00000000 (1)	Data Register for Filter Module 3 (1)
	0x22	0x0000	Time Register for Filter Module 3
	0x23	0x0000/0x00000000 (1)	Data Register for Filter Module 4 (1)
	0x24	0x0000	Time Register for Filter Module 4
	0x25 to 0x7F	0x0000	Not used. Read will return 0x0000

(1) The Data Registers can also be represented as 32-bit.

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All control parameters are stored in the register map. Additionally, the status of the AMC1210 is read out through the register map. The mnemonic in the succeeding register description is given in Example 1.

Example 1: Register Description Mnemonic

Bit 8	Bit 9	Bit 10	The bit position in the register.
CS1	–	SHS	The name of the register bit. A '–' means *Not Used* and therefore a write to such a bit position will get lost.
'1'	'0'	'0'	The digit is the reset value.
W	R	RW	Indicates if the bit position is a read-only (R), readable and writable (RW) or write-only (W).

REGISTER DESCRIPTIONS

This section describes the functionality of each register and its corresponding bits.

Interrupt Register (address 0x00)

The Interrupt Register contains the 12 interrupt flags together with the acknowledge flags. If an interrupt occurs (that is, when the output of the comparator filter is above the high level threshold or below the low level threshold, or when one of the modulators is not functional), the appropriate interrupt flag is set (if enabled). An interrupt flag is reset when the Interrupt Register is read and the corresponding interrupt source is no longer active. The acknowledge bits are reset when the corresponding data register is read. Table 13 describes the Interrupt Register.

Table 13. Interrupt Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1	IFL4	IFH4	IFL3	IFH3	IFL2	IFH2	IFL1	IFH1
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

BIT POSITION	BIT	DESCRIPTION
15	AF4	Acknowledge flag for Filter 4. 0: No new data available for Filter 4 1: New data available for Filter 4
14	AF3	Acknowledge flag for Filter 3. 0: No new data available for Filter 3 1: New data available for Filter 3
13	AF2	Acknowledge flag for Filter 2. 0: No new data available for Filter 2 1: New data available for Filter 2
12	AF1	Acknowledge flag for Filter 1. 0: No new data available for Filter 1 1: New data available for Filter 1
11	MF4	Modulator failure flag for Filter 4. 0: Modulator is operating normally for Filter 4 1: Modulator failure for Filter 4
10	MF3	Modulator failure flag for Filter 3. 0: Modulator is operating normally for Filter 3 1: Modulator failure for Filter 3
9	MF2	Modulator failure flag for Filter 2. 0: Modulator is operating normally for Filter 2 1: Modulator failure for Filter 2

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BIT POSITION	BIT	DESCRIPTION
8	MF1	Modulator failure flag for Filter 1. 0: Modulator is operating normally for Filter 1 1: Modulator failure for Filter 1
7	IFL4	Low-level interrupt flag for Filter 4 0: Comparator Filter 4 output is above the low limit threshold 1: Comparator Filter 4 output is equal to or below the low level threshold, if enabled
6	IFH4	High-level interrupt flag for Filter 4 0: Comparator Filter 4 output is below the high limit threshold 1: Comparator Filter 4 output is equal to or above the high level threshold, if enabled
5	IFL3	Low-level interrupt flag for Filter 3 0: Comparator Filter 3 output is above the low limit threshold 1: Comparator Filter 3 output is equal to or below the low level threshold, if enabled
4	IFH3	High-level interrupt flag for Filter 3 0: Comparator Filter 3 output is below the high limit threshold 1: Comparator Filter 3 output is equal to or above the high level threshold, if enabled
3	IFL2	Low-level interrupt flag for Filter 2 0: Comparator Filter 2 output is above the low limit threshold 1: Comparator Filter 2 output is equal to or below the low level threshold, if enabled
2	IFH2	High-level interrupt flag for Filter 2 0: Comparator Filter 2 output is below the high limit threshold 1: Comparator Filter 2 output is equal to or above the high level threshold, if enabled
1	IFL1	Low-level interrupt flag for Filter 1 0: Comparator Filter 1 output is above the low limit threshold 1: Comparator Filter 1 output is equal to or below the low level threshold, if enabled
0	IFH1	High-level interrupt flag for Filter 1 0: Comparator Filter 1 output is below the high limit threshold 1: Comparator Filter 1 output is equal to or above the high level threshold, if enabled

Control Parameter Register (addresses 0x01, 0x07, 0x0D and 0x13)

The Control Parameter Registers control several parameters for the data acquisition process. The Control Parameter Register functions include the Manchester decoder calibration status, clock pin direction control, delta-sigma modulator mode select, sample-and-hold select and time measure mode. Table 14 describes the Control Parameter Register.

Table 14. Control Parameter Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MS10	MS9	MS8	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0	CD	SHS	TM	MOD1	MOD0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW

BIT POSITION	BIT	DESCRIPTION
15–5	MS10–MS0	Manchester status
4	CD	Input clock direction. 0: Pin CLKx is an input 1: Pin CLKx is an output. The outgoing clock comes from the modulator clock divider.
3	SHS	Sample-and-hold select. 0: Signal SH1 is chosen as sample-and-hold signal 1: Signal SH2 is chosen as sample-and-hold signal
2	TM	Time measure mode. 0: The time is measured from the last filter update to the last rising edge of the selected sample-and-hold signal 1: The time is measured between two rising edges of the selected sample-and-hold signal
1–0	MOD1–MOD0	Delta-Sigma Modulator mode. 00: The clock speed is equal to the data rate from the modulator 01: The clock rate is half of the data rate from the modulator 10: The data from the modulator is Manchester decoded 11: The clock rate is twice the data rate of the modulator

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Sinc Filter Parameter Register (addresses 0x02, 0x08, 0x0E,and 0x14)

The Sinc Filter Parameter Register includes the oversampling ratio (OSR), filter enable, structure and signal mode control bits. Table 15 shows the Sinc Filter Parameter Register.

Table 15. Sinc Filter Parameter Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	SST1	SST0	AE	FEN	SOSR 7	SOSR 6	SOSR 5	SOSR 4	SOSR 3	SOSR 2	SOSR 1	SOSR 0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

BIT POSITION	BIT	DESCRIPTION
15–12	–	Unused. Always read '0'.
11–10	SST1–SST0	Sinc filter structure. 00: Sinc filter runs with a sincfast structure 01: Sinc filter runs with a $Sinc^1$ structure 10: Sinc filter runs with a $Sinc^2$ structure 11: Sinc filter runs with a $Sinc^3$ structure
9	AE	Acknowledge enable. 0: The acknowledge flag is disabled for the particular filter 1: The acknowledge flag is enabled for the particular filter
8	FEN	Filter enable. 0: The filter is disabled and no data is produced 1: The filter is enabled and data are produced in the sinc filter and/or integrator
7–0	SOSR7–SOSR0	Oversampling ratio. The actual rate is SOSR + 1. These bits set the oversampling ratio of the filter. 0xFF represents an oversampling ratio of 256.

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Integrator Parameter Register (addresses 0x03, 0x09, 0x0F and 0x15)

The Integrator Parameter Register controls the integrator functionality. It specifies the integrator oversampling ratio, mode select, shift control, integrator and demodulation enable and data representation control bits. Table 16 shows the Integrator Parameter Register.

Table 16. Integrator Parameter Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SH4	SH3	SH2	SH1	SH0	DR	DEN	IEN	IMOD	IOSR6	IOSR5	IOSR4	IOSR3	IOSR2	IOSR1	IOSR0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

BIT POSITION	BIT	DESCRIPTION
15–11	SH4–SH0	Shift control. These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	Data representation. 0: The data is stored in 16-bit two's complement 1: The data is stored in 32-bit two's complement
9	DEN	Demodulation enable. 0: The demodulation for resolver applications is disabled 1: The demodulation for resolver applications is enabled
8	IEN	Integrator enable. 0: The data from the sinc filter output is stored in the register map 1: The data from the integrator is stored in the register map
7	IMOD	Integrator mode. 0: The oversampling mode updates the data output of the integrator 1: The selected sample-and-hold signal updates the data output of the integrator
6–0	IOSR6–IOSR0	Oversampling ratio. The actual rate is IOSR + 1. These bits set the oversampling ratio of the integrator. 0x03 represents an oversampling ratio of 4.

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High-Level Threshold Register (addresses 0x04, 0x0A, 0x10 and 0x16)

The High-Level Threshold Register contains the upper level value of the interrupt threshold for the comparator filter. If the value of the comparator filter is equal to or above the high level threshold, the corresponding interrupt flag is set (if enabled). Table 17 describes the High-Level Threshold Register.

Table 17. High-Level Threshold Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	HLT14	HLT13	HLT12	HLT11	HLT10	HLT9	HLT8	HLT7	HLT6	HLT5	HLT4	HLT3	HLT2	HLT1	HLT0
'0'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'
R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

BIT POSITION	BIT	DESCRIPTION
15	–	Unused. Always read '0'.
14–0	HTL14–HLT0	Unsigned high level threshold for the comparator filter output.

Low-Level Threshold Register (addresses 0x05, 0x0B, 0x11 and 0x17)

The Low-Level Threshold Register contains the lower level of the interrupt threshold for the comparator filter. If the value of the comparator filter is equal to or below the low level threshold, the corresponding interrupt flag is set (if enabled). Table 18 describes the Low-Level Threshold Register.

Table 18. Low-Level Threshold Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	LLT14	LLT13	LLT12	LLT11	LLT10	LLT9	LLT8	LLT7	LLT6	LLT5	LLT4	LLT3	LLT2	LLT1	LLT0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

BIT POSITION	BIT	DESCRIPTION
15	–	Unused. Always read '0'.
14–0	LTL14–LLT0	Unsigned low level threshold for the comparator filter output.

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Comparator Filter Parameter Register (addresses 0x06, 0x0C, 0x12 and 0x18)

The Comparator Filter Parameter Register controls several parameters for the comparator filters. It specifies the oversampling ratio, three interrupt enables and structure control bits. Table 19 shows the Comparator Filter Parameter Register.

Table 19. Comparator Filter Parameter Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	MFIE	CS1	CS0	IEL	IEH	COSR 4	COSR 3	COSR 2	COSR 1	COSR 0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

BIT POSITION	BIT	DESCRIPTION
15–10	–	Unused. Always read '0'.
9	MFIE	Modulator failure interrupt enable. 0: The modulator failure flag as well as the output INT is disabled for this particular flag 1: The modulator failure flag is enabled
8–7	CS1–CS0	Comparator filter structure. 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a $Sinc^1$ structure 10: Comparator filter runs with a $Sinc^2$ structure 11: Comparator filter runs with a $Sinc^3$ structure
6	IEL	Low-level interrupt enable. 0: The low-level interrupt flag as well as the output INT is disabled for this particular flag 1: The low-level interrupt flag is enabled
5	IEH	High-level interrupt enable. 0: The high-level interrupt flag as well as the output INT is disabled for this particular flag 1: The high-level interrupt flag is enabled
4–0	COSR4–COSR0	Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0xFF represents an oversampling ratio of 256.

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Control Register (address 0x19)

The Control Register controls the signal pattern generator and the interrupt and acknowledge pin behavior. It specifies the interrupt and acknowledge pin polarities, the master interrupt enable and the signal pattern generator length. Table 20 shows the Control Register.

Table 20. Control Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AP	IP	MIE	–	–	–	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
RW	RW	RW	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

BIT POSITION	BIT	DESCRIPTION
15	AP	Acknowledge polarity for pin ACK. 0: New data is signaled with a '1' on the pin ACK 1: New data is signaled with a '0' on the pin ACK
14	IP	Interrupt polarity for pin INT. 0: An interrupt is signaled with a positive transition on the pin INT 1: An interrupt is signaled with a negative transition on the pin INT
13	MIE	Master interrupt enable. 0: Interrupt pin and interrupt flags are blocked (interrupt pin INT always inactive). 1: Interrupt pin and interrupt flags are not blocked and can be set and reset (if individually enabled).
12–10	–	Unused. Always read '0'.
9–0	PC9–PC0	Pattern count. Defines the length of the shift register for the signal generator

Pattern Register (address 0x1A)

The shift register of the signal generator is written through the Pattern Register. Each time this register is written, the shift register is shifted 16 bits upwards and the written data is stored in the 16 LSBs of the shift register. The Pattern Register is a write-only register; a read always returns 0x0000. Table 21 describes the Pattern Register.

Table 21. Pattern Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

BIT POSITION	BIT	DESCRIPTION
15–0	SP15–SP0	Shift register pattern.

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Clock Divider Register (address 0x1B)

The Clock Divider Register sets up the signal generator, the modulator clock division and the signal generator clock. Table 22 shows the Clock Divider Register.

Table 22. Clock Divider Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	HBE	MFE	SGE	PCAL	SCS1	SCS0	MD2	MD1	MD0	SD3	SD2	SD1	SD0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

BIT POSITION	BIT	DESCRIPTION
15–13	–	Unused. Always read '0'.
12	HBE	Signal Generator High-Current Output. 0: The high current option for pins PWM1 and PWM2 is disabled 1: The PWM1 and PWM2 outputs are in High Current Mode
11	MFE	Master Filter Enable. Functionally AND'ed with bit FEN in the Sinc Filter Parameter Register. 0: Sinc filter units of all filter modules are disabled. 1: Sinc filter units can be enabled if bit FEN is '1'.
10	SGE	Signal Generator enable. 0: Signal generator is disabled 1: Signal generator is enabled
9	PCAL	Start of phase correction. Writing a '1' to this bit starts the phase calibration. Reading this bit shows the phase calibration status: 1: The phase calibration is performing 0: No phase calibration is performing
8–7	SCS1–SCS0	Signal generator Control Select (necessary for Phase Calibration and Demodulation on the selected channel). 00: The phase calibration is performed on filter module 1 01: The phase calibration is performed on filter module 2. 10: The phase calibration is performed on filter module 3. 11: The phase calibration is performed on filter module 4.
6–4	MD2–MD0	Modulator clock divider. The coding is equal to the first eight codes in SD; see below.
3–0	SD3–SD0	Signal generator clock divider. 0000: Clock divider is off, outgoing clock equals incoming clock 0001: Outgoing clock is divided by 2 0010: Outgoing clock is divided by 3 0011: Outgoing clock is divided by 4 0100: Outgoing clock is divided by 5 0101: Outgoing clock is divided by 6 0110: Outgoing clock is divided by 7 0111: Outgoing clock is divided by 8 1000: Outgoing clock is divided by 9 1001: Outgoing clock is divided by 10 1010: Outgoing clock is divided by 11 1011: Outgoing clock is divided by 12 1100: Outgoing clock is divided by 13 1101: Outgoing clock is divided by 14 1110: Outgoing clock is divided by 15 1111: Outgoing clock is divided by 16

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Status Register (address 0x1C)

The Status Register shows the overflow conditions of the timer and the integrator, and the locked status of the Manchester Decoder. When the Status Register is read, the flags MAFx, TOx and IOx are reset. Table 23 describes the Status Register.

Table 23. Status Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MAL4	MAL3	MAL2	MAL1	MAF4	MAF3	MAF2	MAF1	TO4	IO4	TO3	IO3	TO2	IO2	TO1	IO1
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

BIT POSITION	BIT	DESCRIPTION
15	MAL4	Manchester locked status for filter module 4. 0: The automatic Manchester encoder calibration is working properly 1: The automatic Manchester encoder calibration has not been able to perform a successful calibration
14	MAL3	Manchester locked status for filter module 3. 0: The automatic Manchester encoder calibration is working properly 1: The automatic Manchester encoder calibration has not been able to perform a successful calibration
13	MAL2	Manchester locked status for filter module 2. 0: The automatic Manchester encoder calibration is working properly 1: The automatic Manchester encoder calibration has not been able to perform a successful calibration
12	MAL1	Manchester locked status for filter module 1. 0: The automatic Manchester encoder calibration is working properly 1: The automatic Manchester encoder calibration has not been able to perform a successful calibration
11	MAF4	Manchester failure status for filter module 4. 0: The automatic Manchester encoder calibration has worked properly since last read access 1: The automatic Manchester encoder has detected problems since last read access
10	MAF3	Manchester failure status for filter module 3. 0: The automatic Manchester encoder calibration has worked properly since last read access 1: The automatic Manchester encoder has detected problems since last read access
9	MAF2	Manchester failure status for filter module 2. 0: The automatic Manchester encoder calibration has worked properly since last read access 1: The automatic Manchester encoder has detected problems since last read access
8	MAF1	Manchester failure status for filter module 1. 0: The automatic Manchester encoder calibration has worked properly since last read access 1: The automatic Manchester encoder has detected problems since last read access
7	TO4	Time counter overflow for filter module 4. 0: No overflow has occurred 1: An overflow occurred in the time measurement unit in filter module 4
6	IO4	Integrator overflow for filter module 4. 0: No overflow has occurred 1: An overflow occurred in the integrator unit in filter module 4
5	TO3	Time counter overflow for filter module 3. 0: No overflow has occurred 1: An overflow occurred in the time measurement unit in filter module 3
4	IO3	Integrator overflow for filter module 3. 0: No overflow has occurred 1: An overflow occurred in the integrator unit in filter module 3
3	TO2	Time counter overflow for filter module 2. 0: No overflow has occurred 1: An overflow occurred in the time measurement unit in filter module 2
2	IO2	Integrator overflow for filter module 2. 0: No overflow has occurred 1: An overflow occurred in the integrator unit in filter module 2
1	TO1	Time counter overflow for filter module 1. 0: No overflow has occurred 1: An overflow occurred in the time measurement unit in filter module 1
0	IO1	Integrator overflow for filter module 1. 0: No overflow has occurred 1: An overflow occurred in the integrator unit in filter module 1

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Data Registers (addresses 0x1D, 0x1F, 0x21 and 0x23)

The Data Registers store the latest data from either the sinc filter or the integrator output for each filter module. The data is presented in two's complement 16-bit or 32-bit format. The bit DR in the Integrator Parameter Register controls the bit width of the Data Register. It takes two bytes to read the 16-bit formatted data and four bytes to read the 32-bit formatted data. The acknowledge flag for the appropriate filter module is cleared when reading the Data Register. Table 24 describes the Data Register in 16-bit formatting.

Table 24. Data Register (16-Bit Format)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

BIT POSITION	BIT	DESCRIPTION
15–0	D15–D0	Data from the sinc filter or the integrator filter in 16-bit formatting.

Table 25 describes the Data Register in 32-bit formatting.

Table 25. Data Register (32-Bit Format)

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

BIT POSITION	BIT	DESCRIPTION
31–0	D31–D0	Data from the sinc filter or the integrator filter in 32-bit formatting.

Time Registers (addresses 0x1E, 0x20, 0x22 and 0x24)

The Time Registers store the latest time information for each filter module. The data is presented in straight binary 16-bit format. The bit TMx in the Control Parameter Register controls the mode of the time measure unit. Table 26 describes the Time Registers.

Table 26. Time Registers

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TD15	TD14	TD13	TD12	TD11	TD10	TD9	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

BIT POSITION	BIT	DESCRIPTION
15–0	TD15–TD0	Data from the time measure unit.

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APPLICATION INFORMATION

The AMC1210 is designed for use in motor control systems utilizing delta-sigma modulators, particularly the ADS120x family of modulators.

Resolver Applications

Resolvers are used in motor control to determine the angular position and speed of the motor. The resolver consists of three coils, one connected to the rotor and the other two situated orthogonally on the stator. By supplying a sine wave carrier signal to the rotor coil, a voltage is magnetically coupled onto the stator coils, of which the amplitude of the signal is directly proportional to the position of the rotor. By digitizing the stator signals, the exact position of the rotor can be mathematically calculated.

Figure 23 shows a block diagram of a standard resolver application.

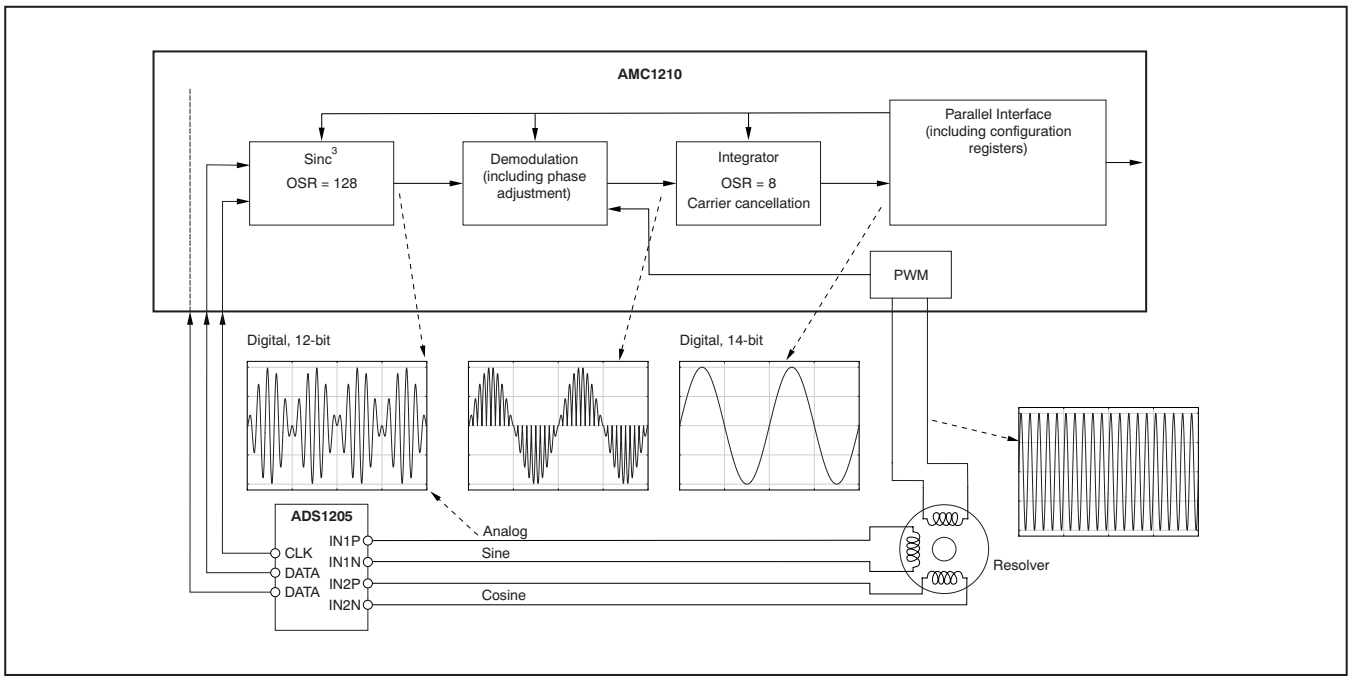

Figure 23. Typical Resolver Application with AMC1210

The AMC1210, along with the ADS120x family of modulators, provides a high-resolution resolver-to-digital converter. The user can program a carrier signal that is synchronous with the data rate of the modulator. The modulators digitize the resulting sine and cosine signals from the resolver. The AMC1210 then filters the modulator data with the sinc filter. The resulting data can then be passed to the integrator, where demodulation occurs.

The demodulated signal first gets multiplied by the polarity of the carrier signal. If the integrator is programmed with the correct OSR, it sums a clock cycle of the rectified signal. The resulting signal is the *baseband* signal of the sine or cosine wave. These values can then be processed by a microcontroller to obtain the actual digital representation of the motor position.

Several factors need to be considered for a high-performance resolver design. The first item of importance is to establish the timing of the motor control loop. This timing is the rate at which the microcontroller updates the motor driving circuitry. A typical application synchronizes the frequency of the carrier signal to the motor control loop frequency. With a known motor control frequency and a system clock frequency, the user can determine how to set up the AMC1210 for optimal performance. Example 2 shows how the AMC1210 would be set up with a carrier frequency of 8kHz and a system clock frequency of 32MHz.

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Example 2: AMC1210 Configuration with 8kHz Carrier Frequency and 32MHz System Clock Frequency

Motor control loop frequency = $f_{CARRIER}$ = 8kHz (3)

f_{CLK} = 32MHz (4)

The carrier frequency is generated using the signal generator, which uses the CLK signal for timing. In order to achieve optimal resolution on the carrier signal, it is recommended to use the largest number of bits possible, up to 1024, for a single cycle of the carrier signal. In this example, the length of the signal generator (PC9–PC0 in the Control Register) was chosen to be 1000. This length means the carrier frequency will be:

$$f_{CARRIER} = \frac{f_{CLK}}{(N_{CDiv} \cdot N_{PAT})} = \frac{32MHz}{(N_{CDiv} \cdot 1000)} \quad (5)$$

Now the Clk_divider value for the signal generator (SD3–SD0 in the Clock Divider Register) can be calculated:

$$CLK_Divider = \frac{f_{CLK}}{(f_{CARRIER} \cdot N_{PAT})} = \frac{32MHz}{(8kHz \cdot 1000)} = 4 \quad (6)$$

Therefore, the user can generate a carrier frequency of 8kHz using a CLK speed of 32MHz, and programming bits PC9–PC0 to 999 (1000 – 1) and bits SD3–SD0 to 3 (4 – 1).

The next matter of importance is to determine the optimal speed versus resolution tradeoff on the modulator. Figure 24 shows the tradeoff in performance for speed on the ADS1205 modulator. A higher OSR can provide increased ENOB (effective number of bits); however, it requires more data from the converter, resulting in an increased filter delay.

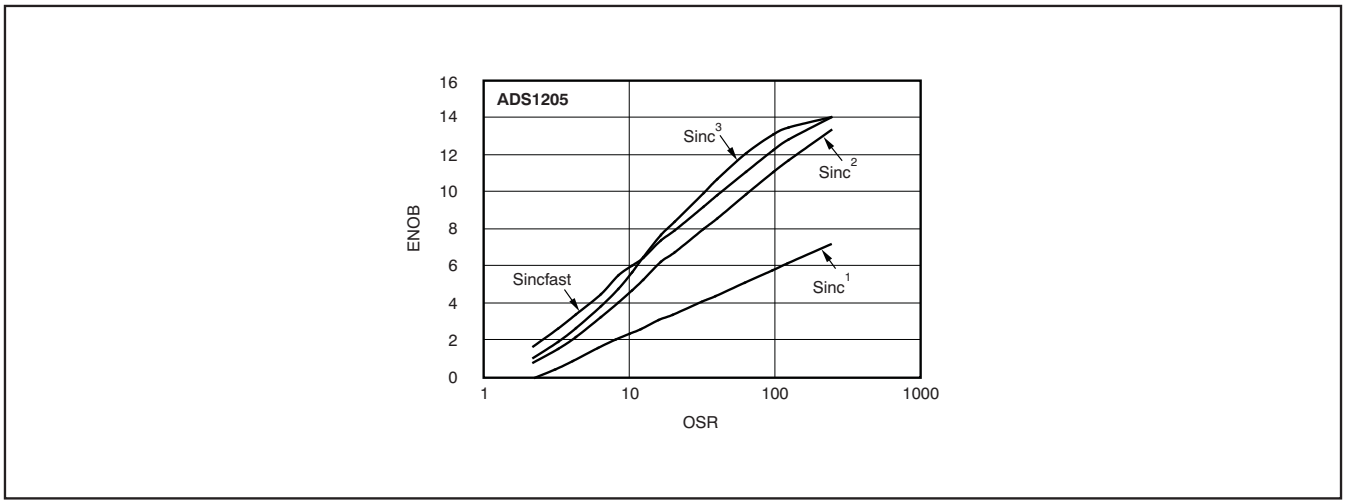

Figure 24. Effective Number of Bits vs Oversampling Ratio (ADS1205)

For maximum resolution, it is best to run the modulator as fast as possible. The speed of the modulator determines what oversampling ratio is needed on the sinc filter and the integrator. In order to synchronize to the motor control loop, the modulator must be decimated down by an integer divisor of the modulator frequency. This relationship is given in Equation 7.

$$f_{MODULATOR} = (f_{CARRIER} \cdot SOSR \cdot ISOR)/N_{INT} \quad (7)$$

Where $\boldsymbol{N_{INT}}$ is the number of carrier signal cycles that will be integrated over. This value is usually set to 1; refer to the application note *Using the AMC1210 in Resolver Motor Control Systems* (SBAA144) for more detail.

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For this example, running the ADS1205 at 16MHz works well. Equation 8 gives the total OSR.

$$SOSR \cdot ISOR = \frac{f_{MODULATOR}}{f_{CARRIER}} = 2000 \quad (8)$$

At this point, the sinc filter oversampling ratio (SOSR) and the integrator oversampling ratio (IOSR) can be defined. From Figure 15, we can see that the best value for ENOB for equivalent OSR values comes from the $Sinc^3$ filter. Therefore, it makes the most sense to choose the $Sinc^3$ filter with a high OSR value. To satisfy Equation 8, the product of the SOSR and ISOR must be 2000. Choosing a $Sinc^3$ filter with an SOSR value of 125 and an ISOR value of 16 produces this result, and gives the following ENOB:

$$ENOB = ENOB_Sincfilter + ENOB_Integrator = 14 + 2 = 16 \quad (9)$$

With these values, we can calculate the frequency of data coming out of the $Sinc^3$ filter:

$$f_{SINC^3} = \frac{f_{MODULATOR}}{SOSR} = 128kHz \quad (10)$$

and the frequency of data coming out of the integrator:

$$f_{INTEGRATOR} = \frac{f_{SINC^3}}{IOSR} = 8kHz \quad (11)$$

The demodulation function allows the integrator to sum a full rectified cycle of the carrier signal. When choosing IOSR = 16, the integrator will sum 16 samples of the digital filter. The demodulation causes a loss of ENOB of approximately 0.5LSB. This demodulation error gives a total system ENOB = 15.5.

In order for this function to work correctly, the phase must be properly aligned between the carrier frequency and the modulator. To perform phase calibration, the carrier frequency, resolver and modulator must be running at the desired rate.

Calculating the angle from two separate channels requires both channels integrating over the same period of time. To ensure that the integrators in separate channels are triggered at the same point in time, the bit MFE in the Clock Divider Register can be used. When MFE is low, all sinc filters are disabled. Conversely, when MFE goes high, all sinc filters that have bit FEN in the Sinc Filter Parameter register high are enabled. The integrator period, when in oversampling mode, is triggered by enabling the sinc filter. Therefore, when MFE goes high, all integrator periods are started simultaneously. This event only works if every other set-up procedure is done before MFE is set high.

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If the drive current needed for the PWM1 or PWM2 pin is in excess of 100mA, or if filtering is desired for a cleaner signal, extra circuitry is required. Figure 25 shows a typical schematic using the AMC1210 and ADS1205 in a resolver application.

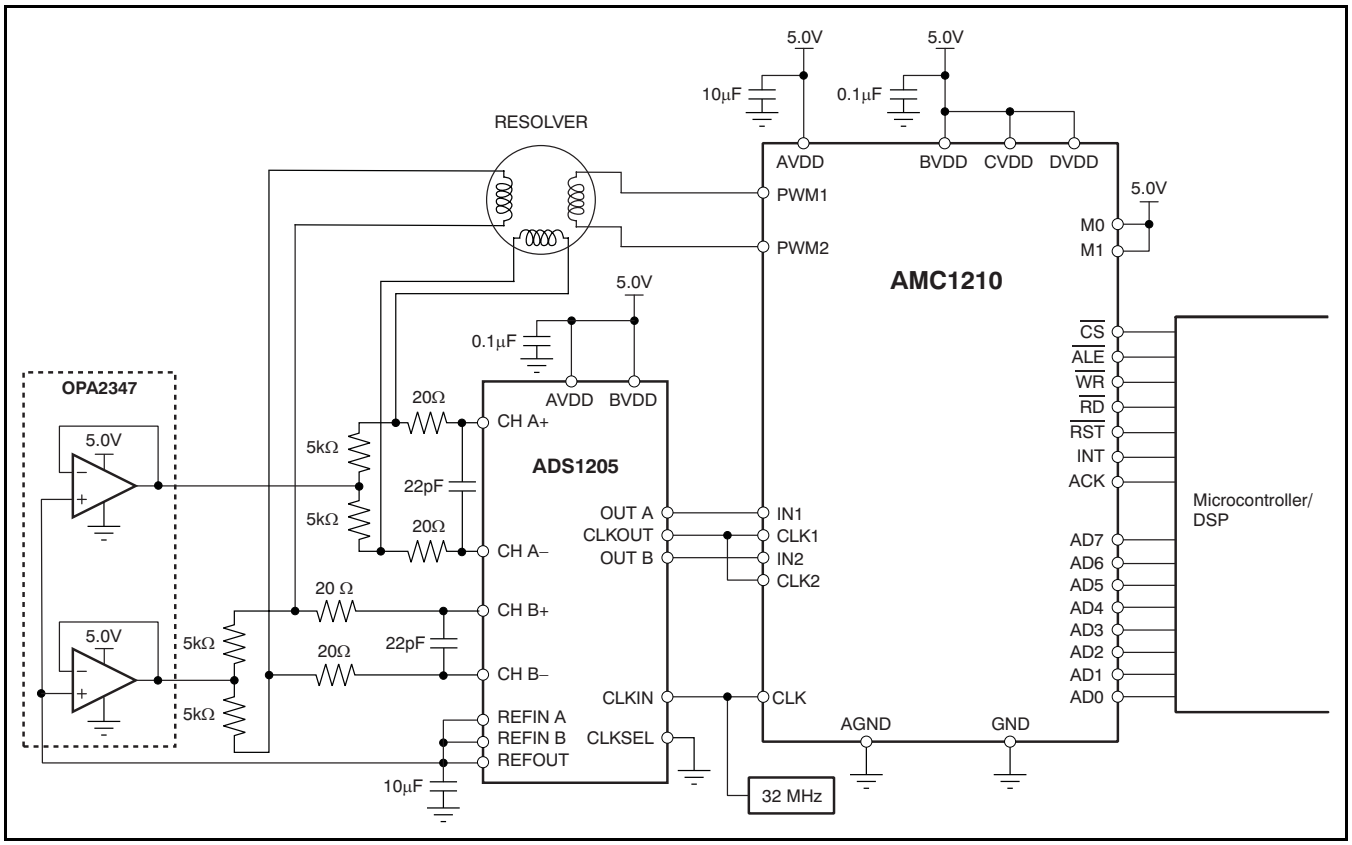

Figure 25. Typical Schematic for Resolver Application

Current Measurement

The AMC1210 can also serve as a stand-alone digital filter for modulator signals coming from current-shunt measurements. Performing the digital filtering in the AMC1210 frees resources in the microcontroller or DSP from having to perform the constant processing required to ensure nonstop monitoring of the motor currents. For example, a common application may require both real-time monitoring of motor over-current situations as well as constant high-resolution data to monitor motor speed. A single filter module in the AMC1210 can perform both high-resolution data filtering as well as provide a fast response, programmable over-current interrupt flag.

Current Shunt Measurement

Current shunt measurements require a small differential signal range (< 1V) and high voltage isolation. This configuration can be incorporated with the AMC1210 with a delta-sigma modulator on the shunt side and a digital isolation device providing common-mode voltage isolation; see Figure 26.

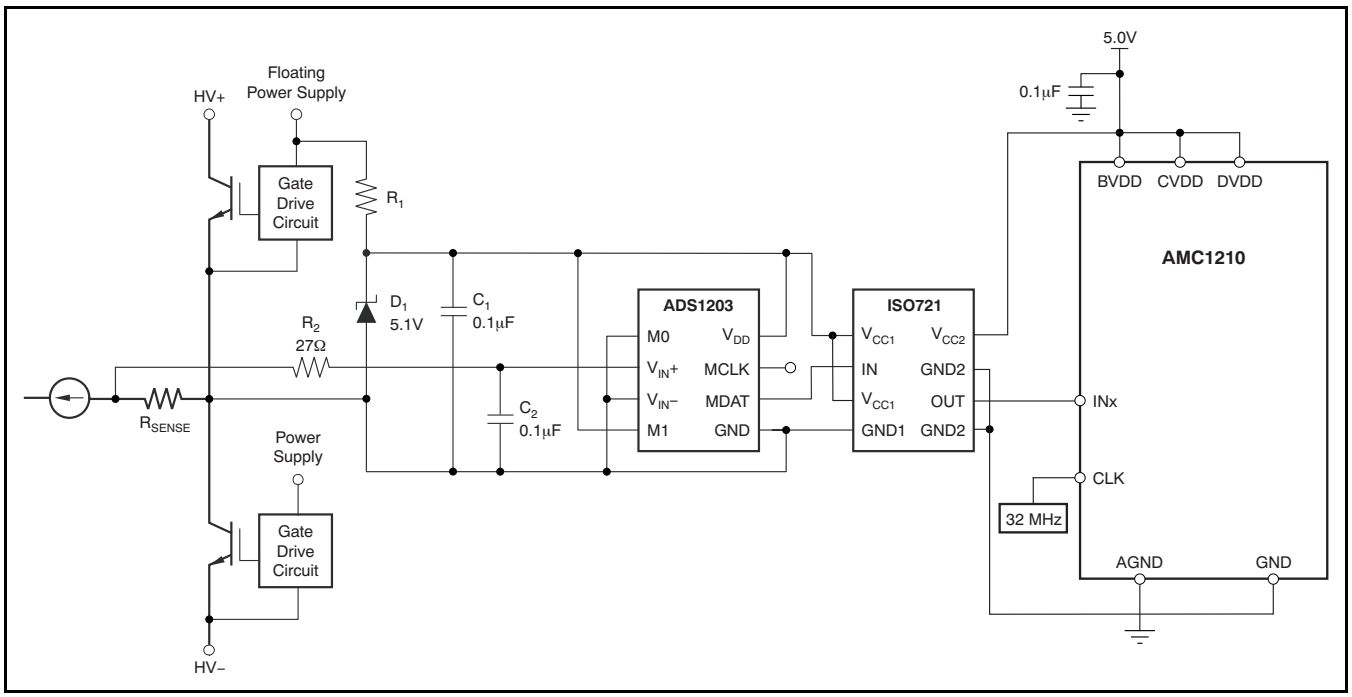

Figure 26. Application Diagram—Isolated Current Measurement

The AMC1210 offers two different ways of current measurement from a modulator. For stable currents, using the modulator along with the Sinc^3 filter offers up to 18.9 effective bits of resolution at an OSR = 256 at a modulator rate of 10MHz.

For unstable currents, the integrator can be used in place of (or in combination with) the digital filter to give an average filter value. When used with the time measurement unit, the integrator provides additional filtering (averaging). This averaging is achieved by using the timer in Mode 2 and the integrator in Sample-and-Hold Mode. On a rising edge of the selected Sample-and-Hold signal, both the integrator and the timer store their current values, reset and begin again. These values, once read from their respective registers, are used to calculate the average value by simply dividing the integrator value by the timer value. Figure 27 illustrates this functionality.

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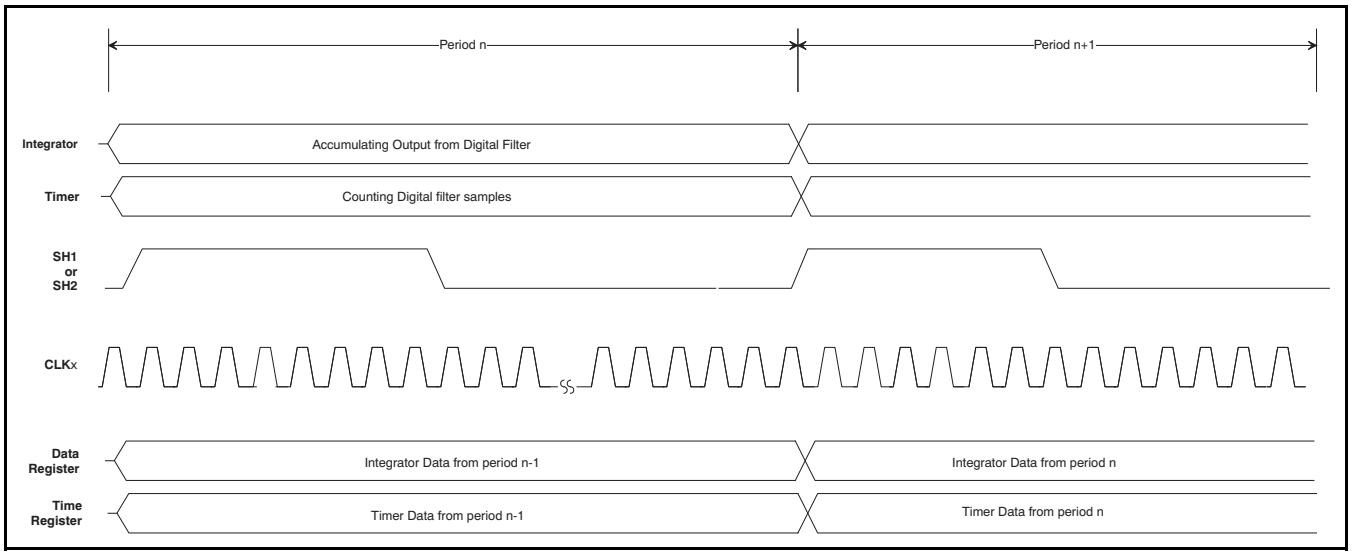

Figure 27. Typical Integrator Sequence

Using the integrator with a digital filter provides improved noise performance for a marginal amount of delay. For example, a $Sinc^2$ filter with an SOSR of 16, combined with an integrator with an IOSR of 64, offers three bits of ENOB improvement at the cost of 1.6µs delay.

The integrator and modulator can also be used together to calculate an average value of high bits (1) and low bits (–1) coming from the modulator in a floating point factor between –1 and 1. Through bypassing the sinc filter unit, the modulator output can be summed directly by the integrator. By setting up the timer and the integrator in the same way as discussed in the previous example (TM = 1, IMOD = 1), an external signal (SHx) triggers the integrator and timer to run simultaneously. Dividing the resulting integrator data by the time data generates a value between –1 and 1. This calculation represents a ratio of high or low bits to the total number of samples, where –1.0 is all low bits, 0.0 is an even number of high and low bits, and 1.0 is all high bits.

Over-Current Measurement

Configuring the AMC1210 for successful over-current measurement requires an understanding of the necessary design conditions. The first parameter to keep in mind is the settling time. Once the user has established a maximum settling time for an over-current event (the time between the over-current event and the first data sample that exceeds the comparator threshold) that the system can tolerate, a corresponding digital filter can be chosen.

Figure 28 shows settling times with the ADS1203 operating at 10MHz. As the allowable settling time is increased, the amount of data that is filtered is increased, resulting in a higher ENOB. In this example, a modulator rate of 10MHz is used. However, it should be noted that the user can also run the ADS1203 at 16MHz. This speed will decrease the settling time by a factor of 1.6; however, power consumption will be increased.

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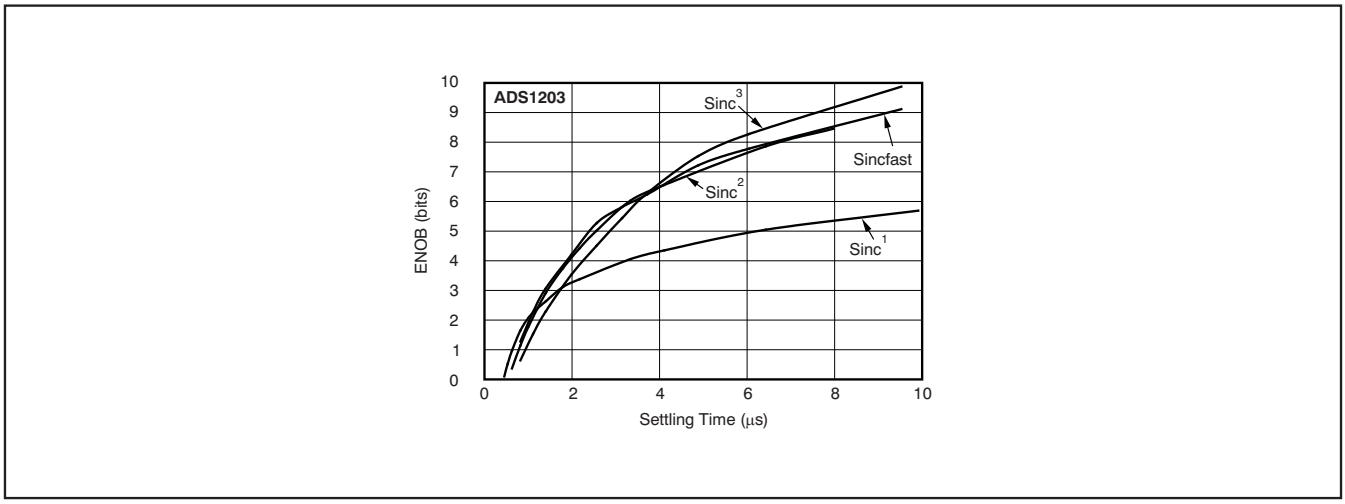

Figure 28. Effective Number of Bits vs Settling Time (ADS1203)

The user should choose a digital filter that gives the maximum ENOB for the desired settling time. If a 3.2µs settling time is assumed, the user should select a $Sinc^2$ filter. For any delay greater than 4µs, the user should choose a $Sinc^3$ filter.

The total delay can be represented by Equation 12:

$$Group_Delay = Order_of_Filter \cdot \frac{OSR}{f_{MODULATOR}} \quad (12)$$

We can then calculate what OSR is necessary to achieve a delay time of 3.2µs by using Equation 13.

$$OSR = \frac{Group_Delay \cdot f_{MODULATOR}}{Order_of_Filter} = \frac{3.2\mu s \cdot 10MHz}{2} = 16 \quad (13)$$

A $Sinc^2$ comparator filter with an OSR of 16 satisfies the settling time requirements for this example system. A high and low comparator value can be chosen by referring to Table 9. For the present example, the comparator filter is capable of a span of 256 codes (from 0 to 256). If an over-current situation is defined at ±25% of the modulator full-scale range, the High Level Threshold level (HLT15–0) and Low Level Threshold level (LLT15–0) should be set to a maximum value of 64 from the full-scale values, or 64 to 192. It may also be necessary to lower this value to avoid an accidental over-current situation. If a 5% guardband is presumed, the threshold levels should be set to 60 and 196.

Hall Sensor Measurement

The AMC1210 can be used directly with the ADS120x family of modulators to interface with Hall sensors in order to provide magnetic field strength measurements. The ADS1208 is a 16-bit, second order, delta-sigma modulator with Hall element biasing circuitry. By connecting the MCLK and MDATA lines of the ADS1208 to the INx and CLKx lines, the AMC1210 needs only a system clock to provide filtered data from the modulator.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2007) to Revision D **Page**

- Updated front page graphic to reflect AMC1203 instead of joint ADS1203 and ISO721 1
- Corrected Table 5 to reflect 24-bit transfer 13
- Updated Equation 7 and added application note reference 39

Changes from Revision B (July 2007) to Revision C **Page**

- Added note under pin out in Device Information. 4

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1210IRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	AMC 1210I
AMC1210IRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	AMC 1210I
AMC1210IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	AMC 1210I
AMC1210IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	AMC 1210I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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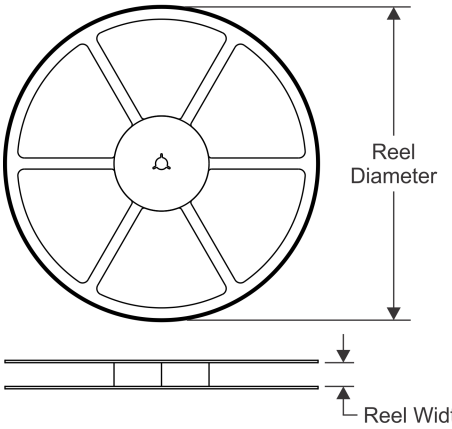
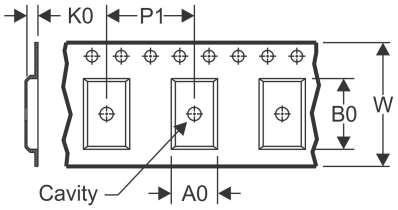
TAPE AND REEL INFORMATION

REEL DIMENSIONS

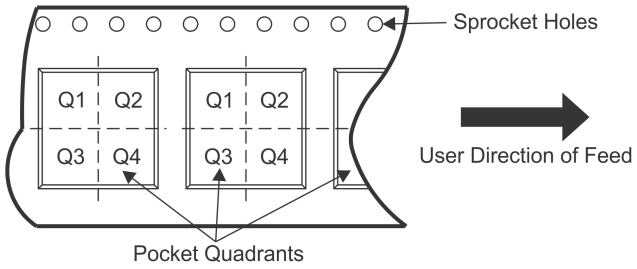


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

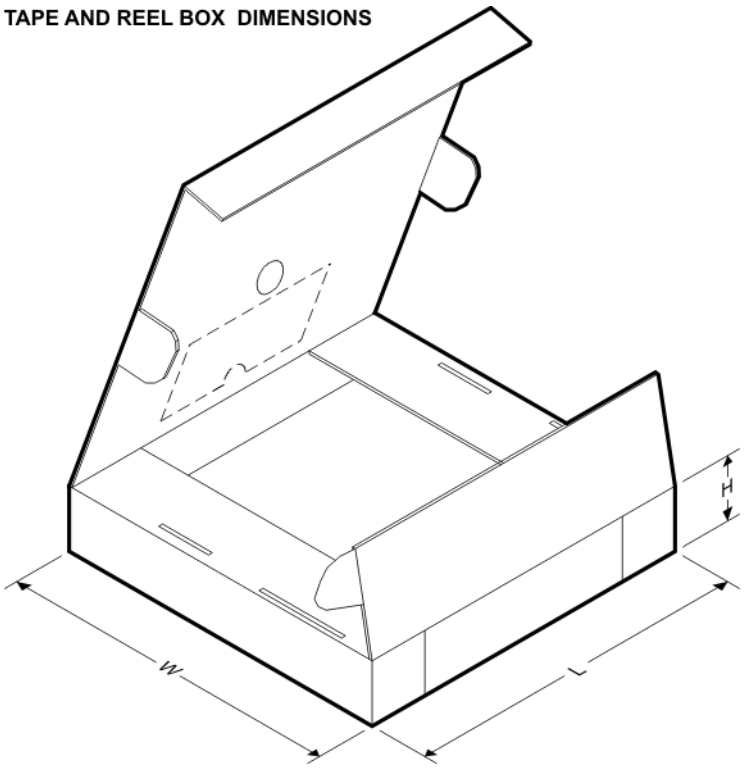
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1210IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1210IRHAR	VQFN	RHA	40	2500	350.0	350.0	43.0

GENERIC PACKAGE VIEW

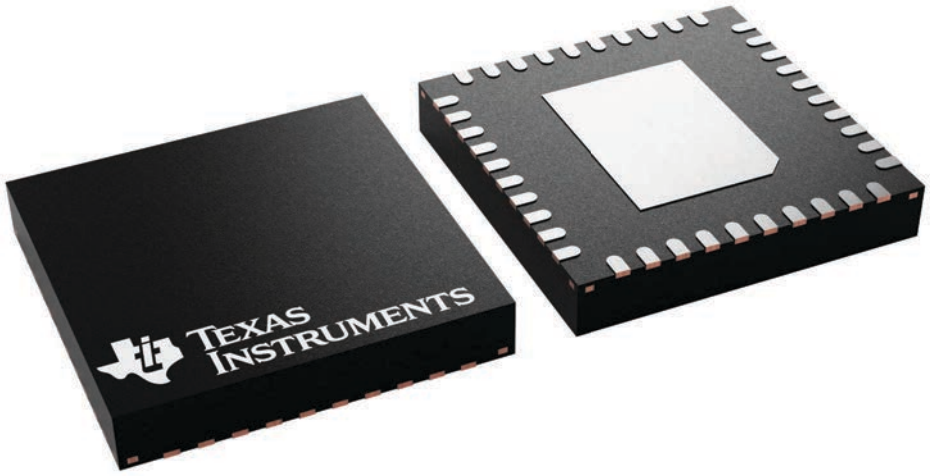
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



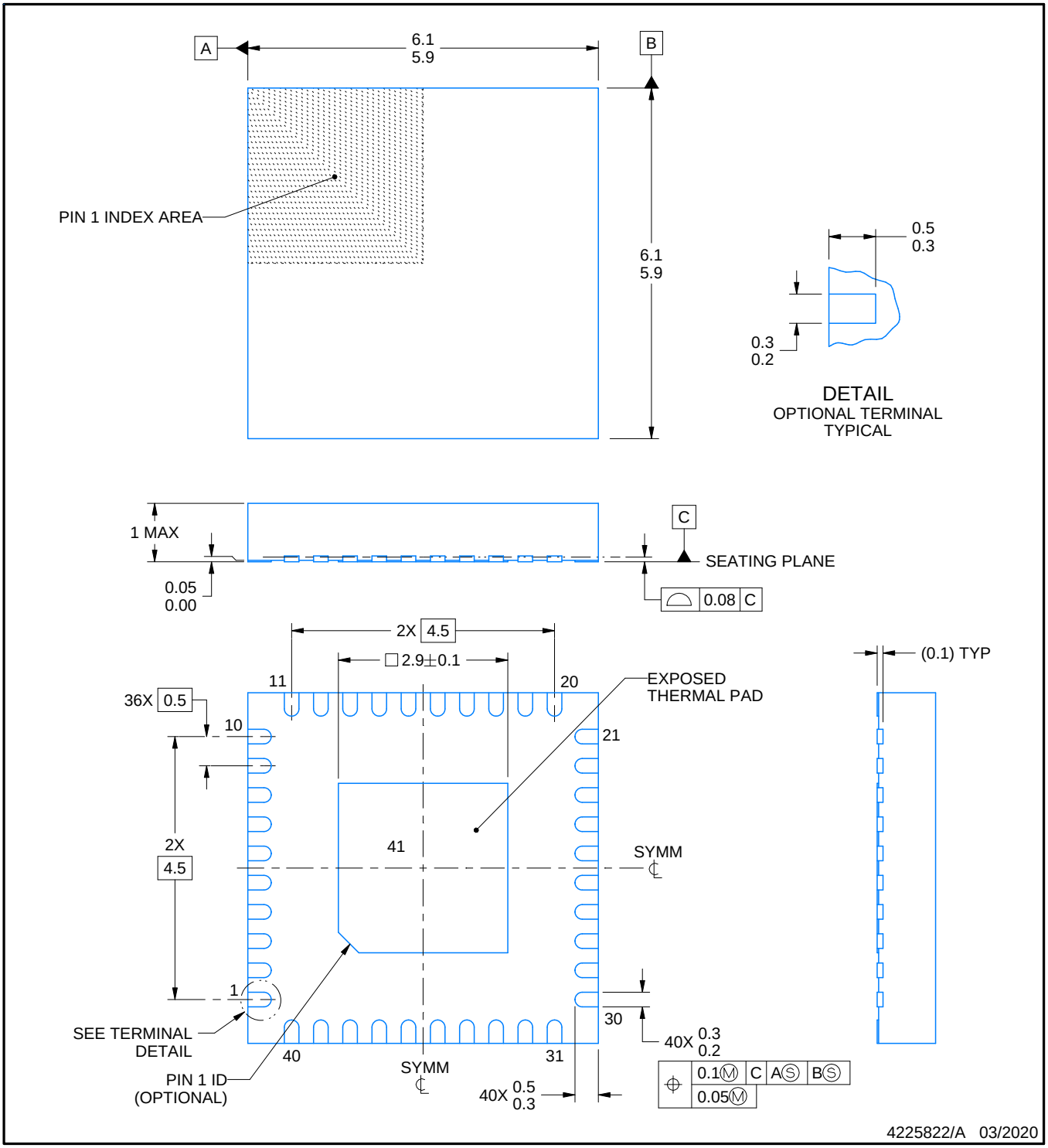
4225870/A

PACKAGE OUTLINE

RHA0040D

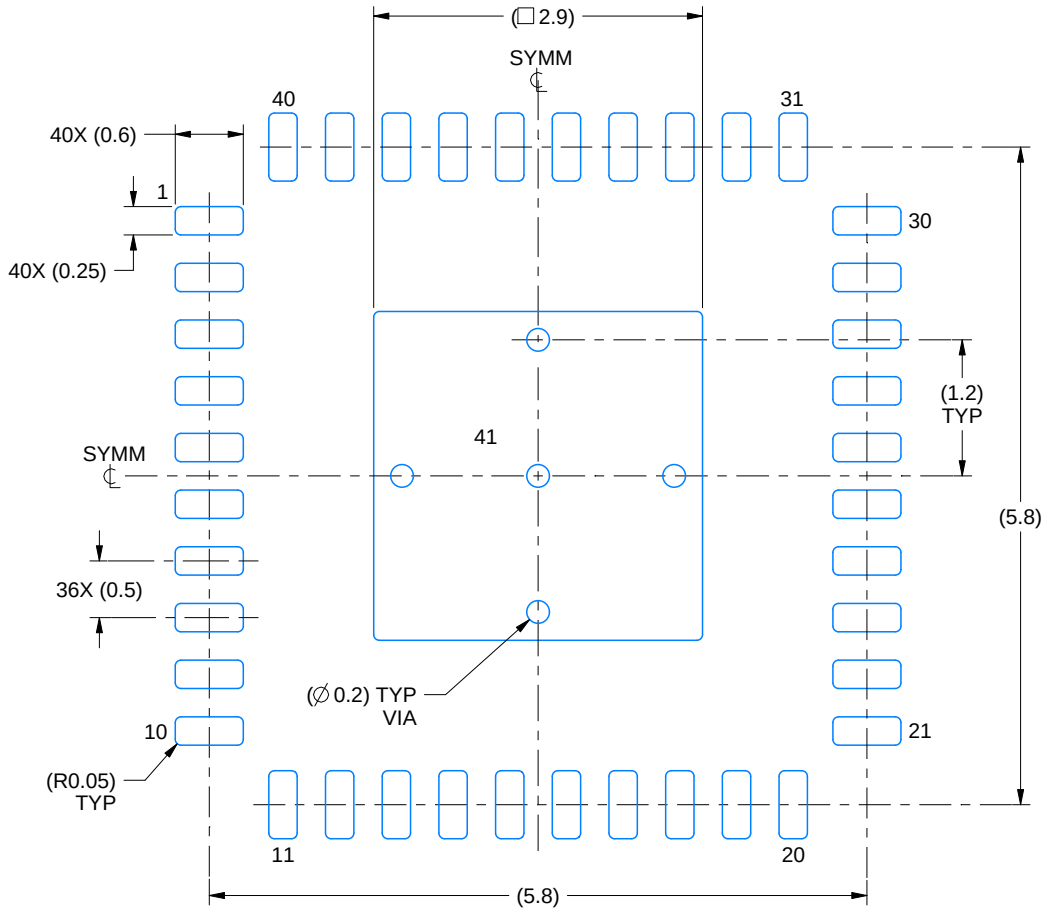
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

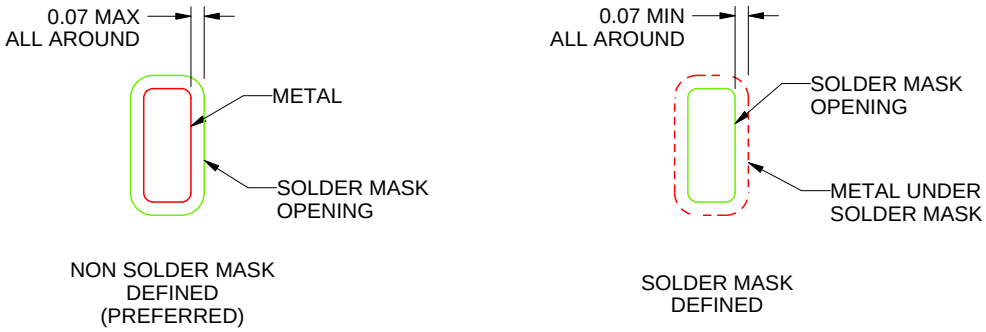


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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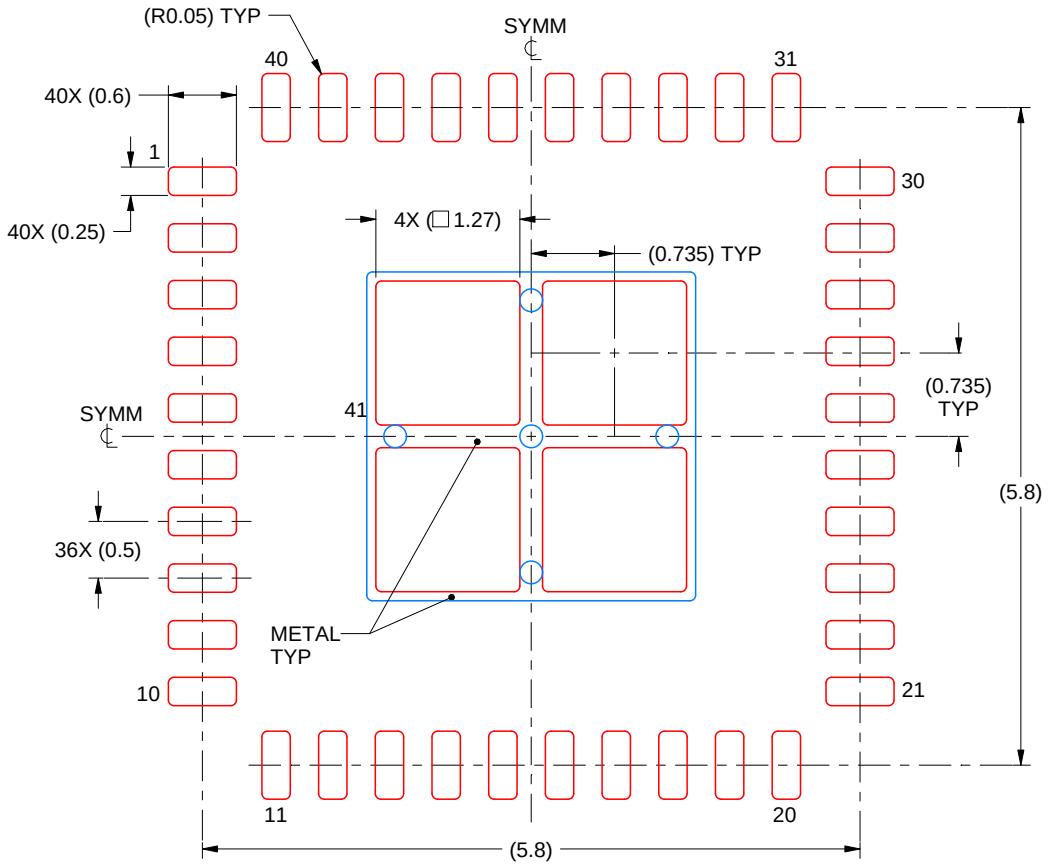
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
76.46% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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