

ABSTRACT

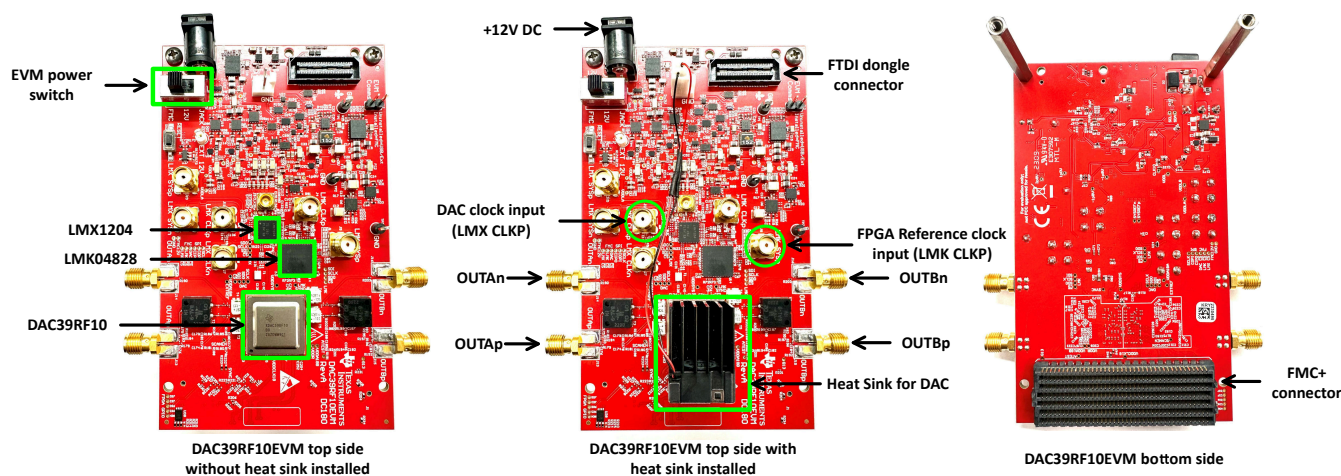
The DAC39RF10EVM is an evaluation board used to evaluate the DAC39RF10, digital-to-analog converters (DAC) from Texas Instruments. The DAC39RF10 is a family of single and dual channel digital-to-analog converter (DAC) with 16-bit resolution. The devices can be used as single channel or dual channel non-interpolation DACs. The device can also be used as interpolating DACs in either direct RF sampling mode or baseband mode. The maximum input data rate is 20.48 GSPS in single channel mode or 10.24 GSPS in dual channel mode or baseband mode. The device can generate signals of up to 10, 7.5, and 5 GHz signal bandwidth (8, 12, and 16-bit input resolution) at carrier frequencies exceeding 8 GHz enabling direct sampling through C-band and into X-band. This evaluation board also includes the following important features:

- Transformer-coupled signal output network allowing a single-ended signal output with an option to bypass the transformer and use the outputs differentially.
- The LMX1204 clock chip distributes the DAC sampling clock
- The LMK04828, clock generator generates SYSREF and FPGA reference clocks for the high-speed serial interface
- Transformer-coupled clock input network to test the DAC performance with an external low-noise clock source
- High-speed serial data output over a High Pin Count FMC+ interface connector

Note

To improve signal routing quality, serial lane polarity is inverted with respect to the standard FMC VITA-57 signal mapping. Signal mapping and polarity is shown in [Table 7-1](#).

- Device register programming through USB connector and FTDI USB-to-SPI bus translator with option to program from FPGA using SPI through FMC+ connector

DAC39RF10EVM KEY COMPONENTS**Figure 1-1. EVM Orientation**

DAC39RF10EVM can be used with the TSW14J59EVM board (pattern generator board). TSW14J59EVM can quickly and easily interface with the DAC39RF10EVM.

Note

For now only 64b/66b encoding modes from serdes data rate from 6Gbps to 12.8Gbps are supported by the TSW14J59EVM. The support for 8b/10b modes and lower serdes rate will be added to future release of HSDCpro software.

The High-Speed Data Converter Pro (HSDC Pro) software is used to communicate with the TSW14J59EVM and is used to generate the data pattern for DAC39RF10.

The TSW14J59EVM takes the generated data pattern, encodes the data, stores the data in memory, and then sends to DAC39RF10EVM through the high-speed serial data link (JESD interface).

With proper hardware selection in the HSDC Pro software, the TSW14J59 board is automatically configured to support a wide range of operating speeds of the DAC39RF10EVM, but the TSW14J59EVM board may not cover the full operating range of the DAC device.

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1 Trademarks

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2 Required Equipment

The following equipment and documents are included in the DAC39RF10EVM kit:

- Evaluation board (EVM)
- Mini-USB cable
- Power cable
- Type C USB cable
- FTDI dongle to program the DAC EVM with FTDI.

The following equipments are **not** included in the DAC39RF10EVM kit, but are required for evaluation of this product:

- TSW14J59EVM data capture board and related items
- High-Speed Data Converter Pro software.
- PC computer running Microsoft® Windows® 10
- Low-noise signal generator for DEVCLK (Sampling clock) . TI recommends the following generators:
 - Rohde & Schwarz® SMA100B
- Signal-path cables, SMA or BNC (or both SMA and BNC)

By default, the DAC39RF10EVM uses LMX1204 clocking chip to distribute the external clock signal to DAC39RF10 and also to LMK04828 to generate necessary clocks needed for the TSW14J59EVM. A few board modifications enables user to test the DAC39RF10 with other clocking options. The other clocking option are discussed in the Appendix section of the uses guide.

3 Setup Procedure

This section describes how to setup the DAC and TSW14J59 EVMs on the bench with the proper equipment to evaluate the performance of the DAC device.

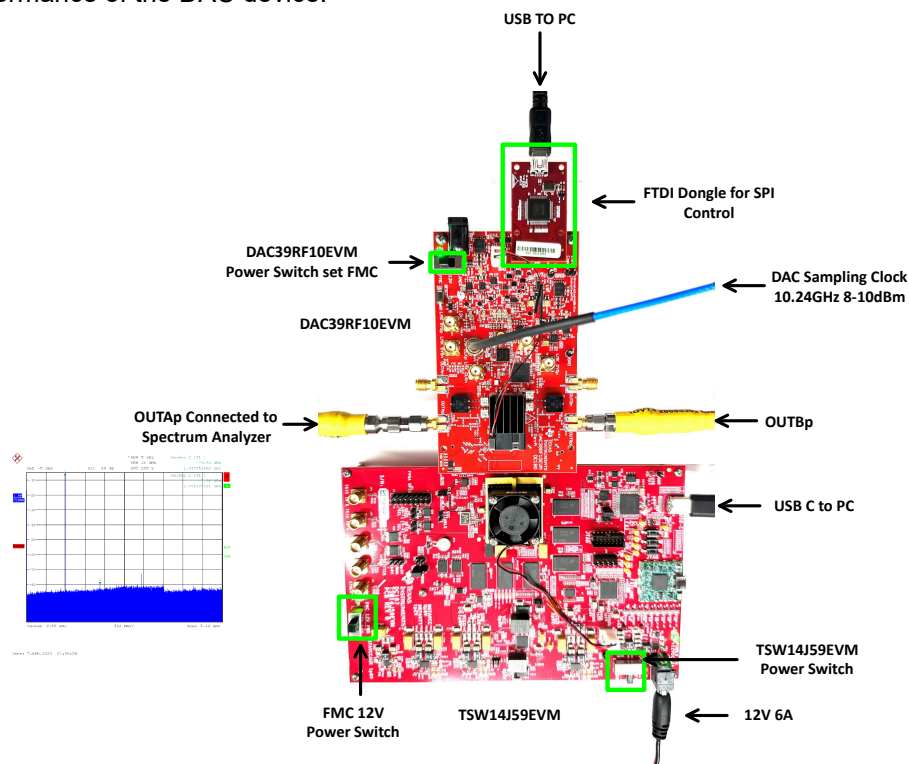


Figure 3-1. DAC39RF10EVM Test Setup

Note

The HSDC Pro software must be installed before connecting the TSW14J59EVM to the PC for the first time.

3.1 Installing the High Speed Data Converter (HSDC) Pro Software

1. Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.

3.2 Installing the DAC39RF10EVM Configuration GUI Software

1. If installing the DAC gui for the first time, please download and install the FTDI drivers from [FTDI website](#).
Restarting the PC may be required after installing the driver.
2. Download the Configuration GUI software from the EVM tool folder at [DAC39RF10EVM GUI](#).
3. Extract files from the .zip file.
4. Run the executable file (DAC39RF10.exe).

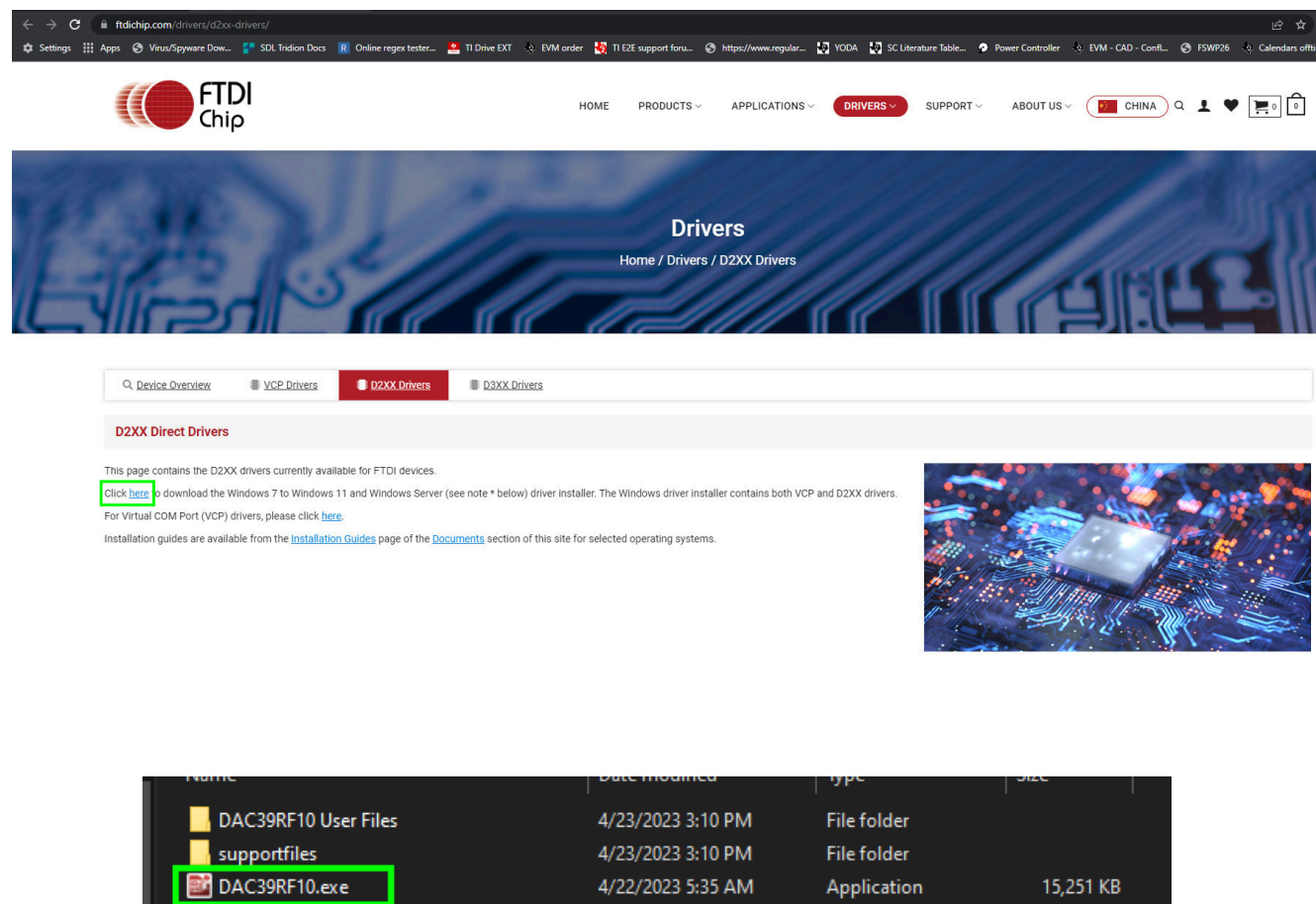


Figure 3-2. FTDI website to download and install the driver.

3.3 Connect the DAC39RF10EVM and TSW14J59EVM

1. With the power off, connect the DAC39RF10EVM to the TSW14J59EVM through the FMC+ connector as shown in [DAC39RF10EVM Test Setup](#). Make sure that the standoffs provide the proper height for robust connector connections.

3.4 Connect the Power Supplies to the Boards (Power Off)

1. Confirm the power switch on the TSW14J59EVM is in off position. Connect the power cable to a 12-V DC (minimum 6A) power supply. Make sure the proper supply polarity by confirming the outer surface of the barrel connector is GND and the inner portion of the connector is 12 V. Connect the power cable to the TSW14J59EVM power connector.
2. DAC39RF10EVM can be powered with 12-V DC(minimum 2 A) though the connector jack(J1) on the DAC39RF10EVM or it can be powered from the TSW14J59EVM via FMC+ connector. There is a switch(SW1) which can be used to select power from the barrel jack on the DAC EVM or from TSW14J59EVM through FMC+ connector. Confirm that the power switch for the DAC39RF10EVM's power supply is set to the opposite position(jack) from which it should be drawing power. If using barrel jack option connect the power cable to a 12-V DC (minimum 2 A) power supply. Make sure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12 V. Connect the power cable to the EVM power connector. The [Table](#) can be used as a reference to power the DAC EVM.

Table 3-1. Powering the DAC39RF10EVM

DAC39RF10 Powered from	DAC39RF10 Power Switch position	TSW14J59EVM FMC switch position	Power supply needed
TSW14J59EVM via FMC+ connector	FMC(Default option)	ON	12V 6A for TSW14J59EVM
External Supply with jack on DAC39RF10EVM	JACK	OFF	12V 5A for TSW14J59 and 12V 2A for DAC39RF10EVM

CAUTION

Make sure the power connections to the EVMs are the correct polarity. Failure to do so may result in immediate damage. Leave the power switches in the off position until directed later.

3.5 Connect the Spectrum Analyzer to the EVM

Connect a spectrum analyzer to the Aoutp (J13) SMA connector of the DAC39RF10EVM .

When LMX->DACCLK | LMX/LMK->FPGA Clocking option is Used (Default)

1. Connect a signal generator to the LMX CLKp input of the EVM. This signal generator must be a low-noise signal generator. Configure the signal generator for the desired clock frequency in the range of 0.8 to 10.24 GHz (for this example 10.24 GHz is used). For best performance when using an RF signal generator, the power input to the LMX CLKp SMA connector must be 8-10 dBm (2 Vpp into 50 Ω).
2. This step is only need if third clocking option(EXT-> DACCLK | LMK->FPGA) is used otherwise skip to next step. Connect a signal generator to the LMK CLKp input of the EVM at SMA (J5). This signal is used to generate the necessary FPGA clock signal. Configure the signal generator for the desired (160 MHz) clock frequency. Set the output power to approximately 5–7 dBm.

Note

- a. The FPGA REF clock frequency can be obtained from the DAC39RF10EVM GUI. Once the DAC39RF10EVM GUI is configured to the desired JMODE mode and clock rate. The Reference Clock frequency required by the EVM is displayed on first page of the GUI shown in [Configuration of DAC39RF10EVM GUI](#)
- b. Make sure that the DEVCLK and Reference clock sources are frequency-locked using a common 10-MHz reference to for functionality.
- c. Do not turn on the RF output of any signal generator at this time.

3.6 Turn On the TSW14J59EVM Power and Connect to the PC

1. Turn on the power switch to the TSW14J59EVM.
2. Connect a USB-C cable from the PC to the TSW14J59EVM.
3. If this is the first time connecting the TSW14J59EVM to the PC, follow the on-screen instructions to automatically install the device drivers. See the [TSW14J59EVM user's guide](#) for specific instructions.

3.7 Turn On the DAC39RF10EVM Power Supplies and Connect to the PC

1. The default option uses the power from FMC+ connector on TSW14J59EVM. For this option, the FMC power switch on TSW14J59EVM should be set to on position and power switch on the DAC39RF10EVM should be set to FMC(defalut). If external power supply is used to power the DAC EVM. Then turn on the 12-V power supply connected to the barrel jack on the DAC EVM and set the power switch position on DAC39RF10EVM to JACK position.

The green LED(D3) on DAC EVM should turn on, indicating DAC EVM is getting power.

2. Connect the DAC EVM to the PC with the mini-USB cable via the FTDI DONGLE provide with the EVM.

3.8 Turn On the Signal Generator RF Outputs

Turn on the RF signal output of the signal generator connected to LMX CLKp. If external clocking option is used, turn on the RF signal outputs connected to LMK CLKp(FPGA reference clock).

3.9 Launch the DAC39RF10EVM GUI and Program the DAC EVM

The DAC39RF10EVM configuration GUI is installed separately from the HSDC Pro installation and is a stand-alone GUI.

Note

The max clock rate supported by DAC39RF10EVM is 10240 MHz

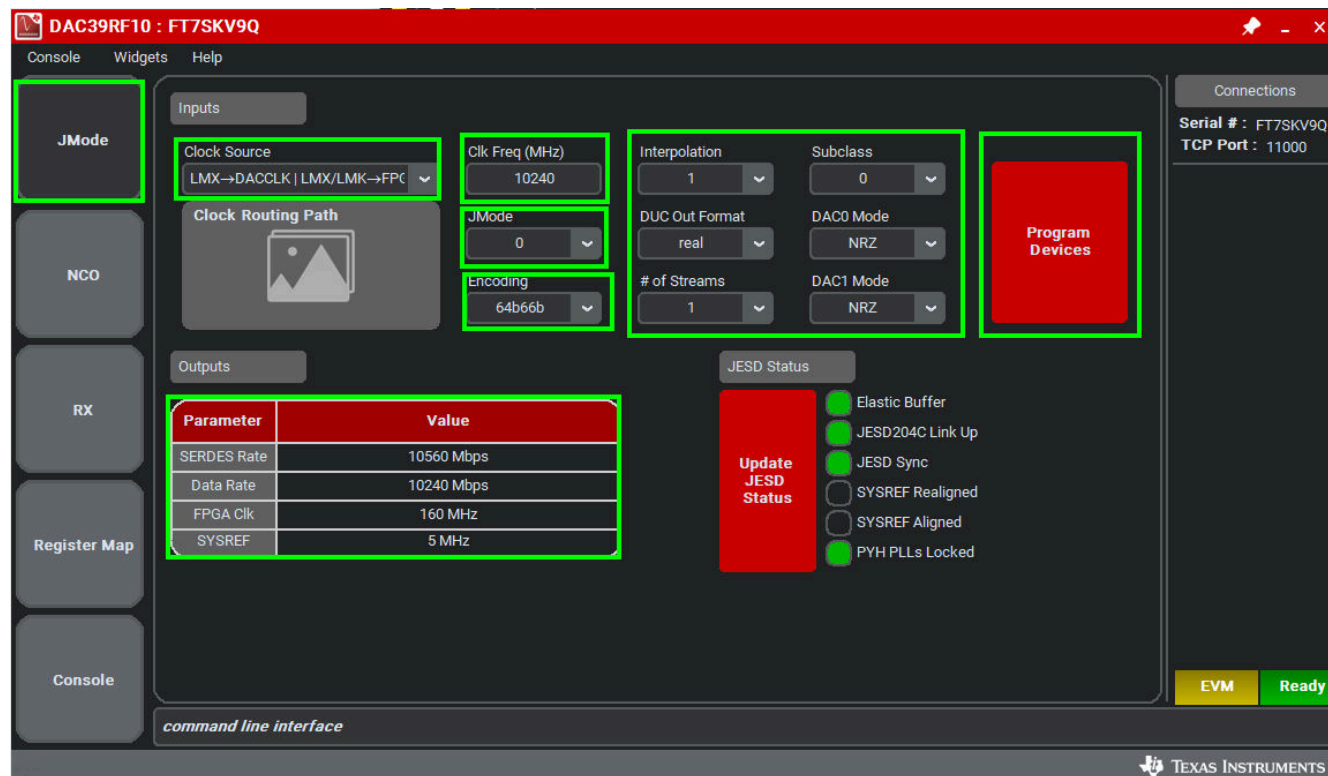


Figure 3-3. Configuration of DAC39RF10EVM GUI

Figure 3-3 and Figure 3-4 show the GUI opened to the JMODE tab and NCO tab respectively. Tabs at the left of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has three configurable devices, namely the DAC39RF10, LMX1204 and LMK04828. The register map for each device is provided in the device data sheet ([DAC39RF10](#), [LMK04828B](#), and [LMX1204](#), respectively).

1. Launch the DAC39RF10EVM GUI.
2. Select the LMX->DACCLK | LMX/LMK->FPGA as the clock source.
3. Enter Clk Freq 10240 MHz.
4. Select JMODE0 for JMODE option.
5. Select 64b66b for Encoding option.
6. The other option can be left to default settings.
7. Click *Program Devices* (Note: This action overwrites any previous device register settings.)

3.10 Programming the NCO

The following steps are only needed when DAC is programmed to JMODE 1 to 7. For JMODE0 the NCO configuration can be skipped to the section [HSDCpro section](#). For JMODEs 1 to 7 when number of streams M is greater than or equal to 2 and interpolation factor is also set to greater than or equal to 2, the NCO(numerically controlled oscillator) can be used to mix I/Q baseband signal to generate a higher output frequency signal from the output of the DAC.

[Table 3-2](#) describes the relationship of interpolation factor and number of streams to number of DUCs (Digital up converter) that can be used.

Table 3-2. Supported Interpolation Factors vs Number of DUCs Enabled

Number of Streams	Interpolation Factors	DUCs Enabled
2	2-256x	DUC0
4	4-256x	DUC0, DUC1
6	8-256x	DUC0, DUC1, DUC2
8	8-256x	DUC0, DUC1, DUC2, DUC3

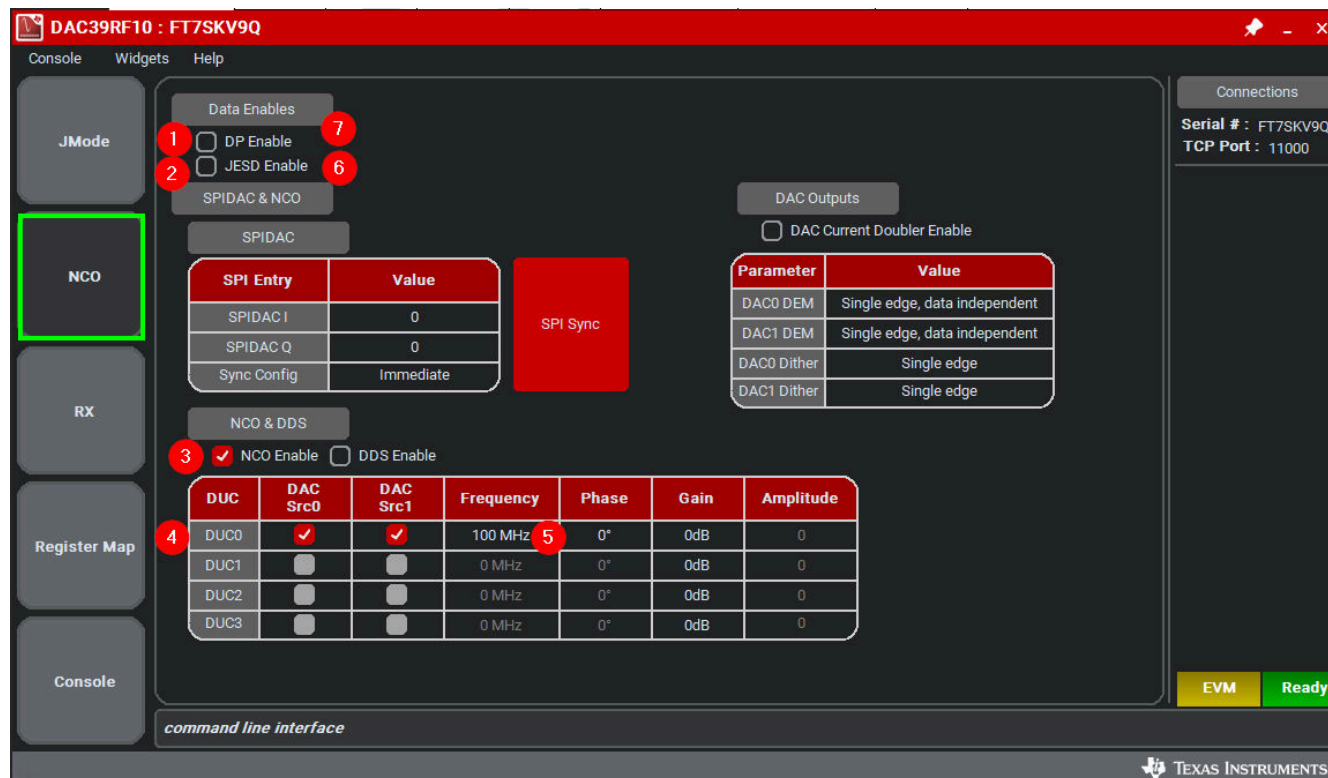


Figure 3-4. NCO TAB CONTROLS

With the EVM gui open on the PC, navigate to NCO tab on upper left side of the GUI.

1. To set the NCO uncheck the DP Enable
2. Uncheck the JESD Enable
3. Check the NCO Enable
4. In this example, JMODE was set to 1 and number of stream is set to 2. The interpolation factor is set to 2. In [Supported Interpolation Factors vs Number of DUCs Enabled](#) only DUC0 can be used, and other DUCs have been grayed out. The data from DUC0 is routed to DAC0 and DAC1
5. Enter the Frequency in MHz
6. Check the JESD Enable
7. Check the DP Enable.

3.10.1 SPIDAC(NCO only) Operation

The DAC can also be configured in SPIDAC Operation (NCO only mode). In NCO only mode, data streamed from JESD is ignored and DUCs inputs are driven by SPIDAC I and SPIDAC Q. This mode can be enabled when JESD Enable is set to 0, interpolation factor is greater than or equal to 2 and DP Enable is set to 1, the DAC is configured in NCO only mode. Following [Table 3-2](#), the correct combination of number of streams and interpolation factor should be selected to enable the desired number of DUCs and setting the desired outputs from respective DACs.

In the Example, all the four DUCs are enabled. DUC0 and DUC1 are routed to DAC0 and DUC2 and DUC3 are routed to DAC1. If more than one DUC is routed per DAC, the DUC data into the DAC must be attenuated to prevent the DAC from saturating.

The NCO only mode can be configured through the GUI by following steps.

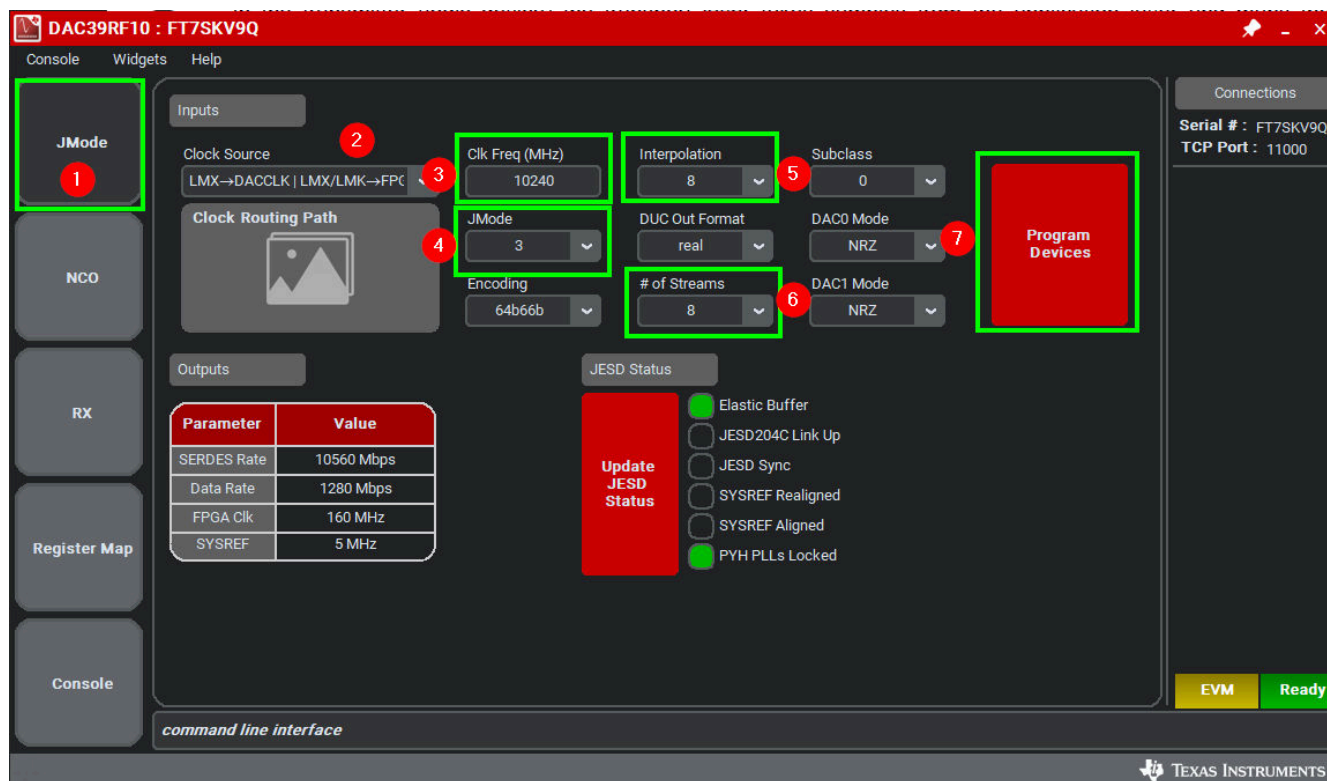


Figure 3-5. NCO only JMODE settings for GUI.

1. Launch the DAC39RF10EVM GUI.
2. Select the LMX->DACCLK | LMX/LMK->FPGA as the clock source.
3. Enter Clk Freq 10240 MHz.
4. Select JMODE3 for JMODE option.
5. Select 8 for Interpolation
6. Select 8 for number of streams
7. Click the button Program Devices.
8. On the NCO tab uncheck the DP Enable
9. Uncheck the JESD Enable
10. For SPIDAC I enter the value of 32767 for full scale output power.
11. Check the NCO Enable
12. Select the correct DUC routing(DUC0 and DUC1 routed to DAC0 and DUC2 and DUC3 routed to DAC1).
Since two DUC are routed to single DAC The gain value should be adjusted to -6dB to prevent the DAC from saturating.
13. Enter the desired frequency
14. Check the DP Enable.
15. The DAC should have outputs on both channels.

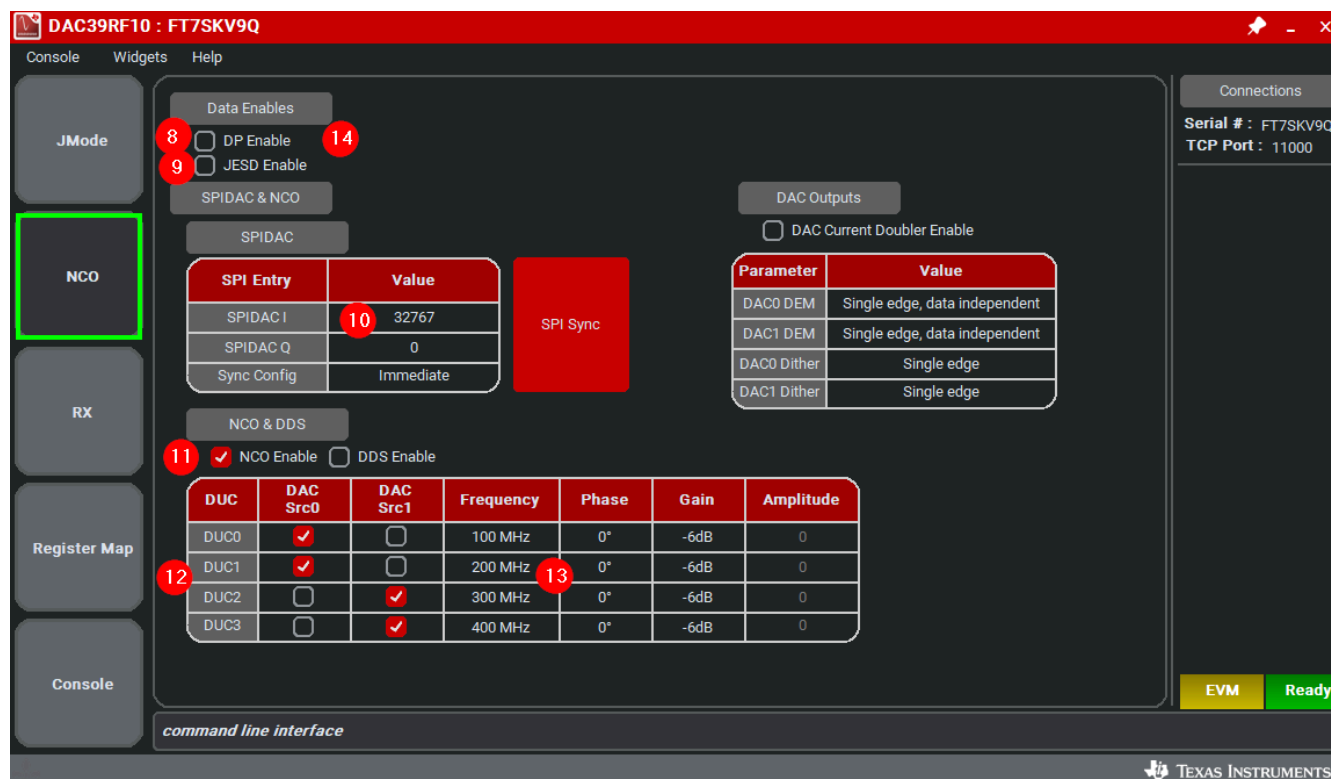


Figure 3-6. NCO only mode GUI settings

Similar to SPI DAC mode, the DDS mode can be used as a lower power option. To enable DDS mode, the following steps are used.

1. Follow steps 1-9.
2. Skip step 10.
3. For 11 step select DDS Enable.
4. Follow step 12 according to requirements.
5. Follow step 13.
6. For Amplitude(Two DUCs routed to single DAC, amplitude reduced by 6 dB from max value of 32767 to 16384) program 16384.
7. Follow step 14.
8. The DAC should have outputs on both channels.

3.11 Launch the HSDCpro Software and Load the FPGA Image to the TSW14J59EVM

1. Launch the HSDCpro 5.303 or later software.
2. Click OK to confirm the serial number of the TSW14J59EVM device. If multiple TSWxxxxx boards are connected, select the model and serial number for the one connected to the DAC39RF10EVM.
3. For Device select DAC from drop down menu.

If the pop up says No Firmware. Please select a device to load firmware into the board click **OK** proceed to next step.

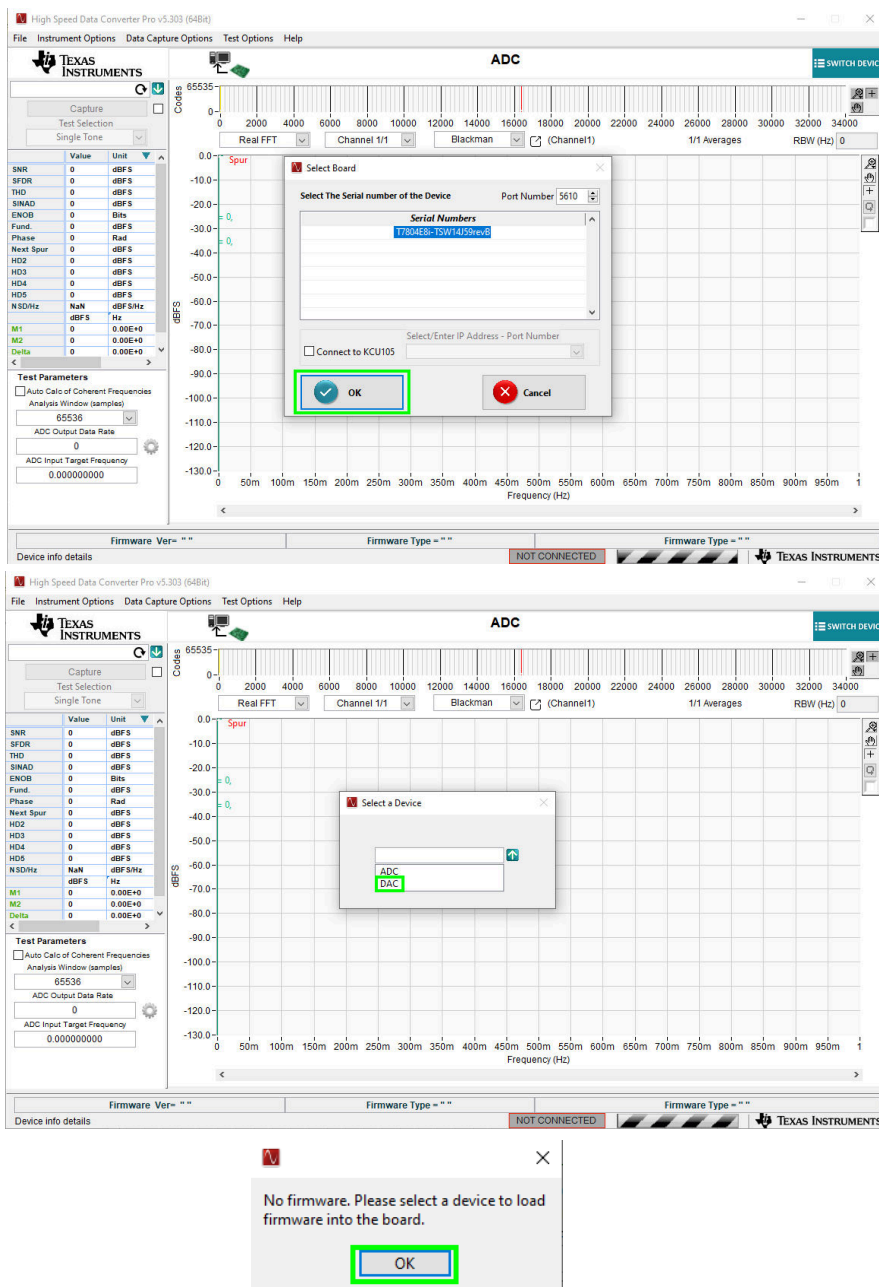


Figure 3-7. Launching HSDCpro and Setup

4. Select the DAC39RF1x_JMODE0 device from the DAC select drop-down in the top left corner.
5. When prompted, click Yes to update the firmware(wait for Firmware to download).

Note

If the user configures the EVM with options other than the default register values, different instructions may be required for selecting the device in HSDC Pro. See [Section 7](#) for more details.

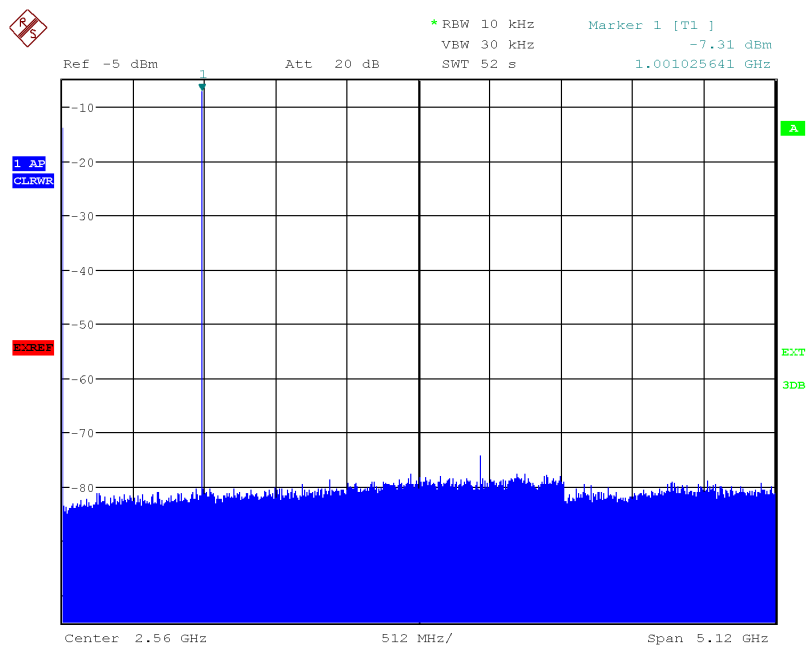


Figure 3-8. HSDCpro Setup

6. Enter the Data Rate as "10.24G" or the desired input data rate. The Data rate value can be referenced from the DAC39RF10EVM GUI. It is displayed on output parameter as shown in [Configuration of DAC39RF10EVM GUI](#).
7. For DAC Option dropdown select the "Offset Bin" option.(The DAC39RF10EVM gui always defaults to offset binary).
8. Navigate to lower left side of the HSDCpro GUI to I/Q Multitone Generator section. For # of tones enter 1, for Tone Center enter 1G(1 GHz or desired frequency), # Samples can be left 65536.
9. Tone selection should be "Real", since this is JMODE0 , the DUC/ NCO is bypassed. If other JMODE was configured, such that DUC/NCO was used the Tone selection should be "Complex".
10. Click Create Tones button and then click Send in upper left side of HSDCpro GUI. If a pop appear mentioning the SERDES RATE click OK. The DAC should be sending the programmed frequency to the outputs.



Figure 3-9. HSDCpro Generating the Tone and Sending it to the DAC.



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Figure 3-10. DAC Output Displayed on Spectrum Analyzer

4 Device Configuration

The DAC device is programmable through the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the FTDI dongle. A GUI is provided to write instructions on the bus and program the registers of the DAC device.

For more information about the registers in the ADC device, see the [DAC39RF10 device data sheet](#).

4.1 Supported JESD204C Device Features

The DAC device supports some configuration of the JESD204C interface. Due to limitations in the TSW14J59EVM firmware, all JESD204C link features of the DAC device are not supported. [Table 4-1](#) lists the supported and non-supported features.

Table 4-1. Supported and Non-Supported Features of the JESD204C Device

JESD204C Feature	Supported by DAC Device	Supported by TSW14J59EVM
Number of lanes per link (L)	L = 1, 2, 3, 4, 6, 8, 12, 16 ⁽¹⁾	L = 1, 2, 3, 4, 6, 8, 12, 16 supported
Scrambling	Supported	Supported
Test patterns	PRBS7, PRBS9, PRBS15, PRBS31	Not Supported
Speed	Lane rates from 0.75 to 12.8 Gbps	Lane rates from 2 to 17.16 Gbps $f_{\text{(SAMPLE)}}$ parameter must be properly set in HSDC Pro GUI.

(1) Dependent on bypass or decimation mode and output rate selection. Always disable the JESD204 block before changing any of the JESD204C settings. Once the settings are changed, re-enable the JESD204 block.

4.2 Tab Organization

Control of the DAC device features are available in the JMode, NCO and RX tabs.

4.3 Register Map and Console Control

The *Register Map* tab, illustrated in [Figure 4-1](#), allows configuration of the devices at the bit-field level. At any time, the controls in [Table 4-2](#) can be used to configure or read from the device.

The Console tab logs all the SPI reads and writes which are performed when various devices are programmed on the DAC EVM. The config files can be saved and loaded from the console tab.

Table 4-2. Register Map and Console Controls

Control	Description
Register map summary	Displays the devices on the EVM, registers for those devices, and the states of the registers <ul style="list-style-type: none"> Clicking on a register field allows individual bit manipulation in the register data cluster The value column shows the value of the register at the time the GUI was last updated The LR column shows the value of the register at the time the register was last read
Write register button	Write to the register highlighted in the register map summary with the value in the <i>Write Data</i> field
Write all button	Update all registers shown in the register map summary with the values shown in the <i>Register Map</i> summary
Read register button	Read from the register highlighted in the <i>Register Map</i> summary and display the results in the <i>Read Data</i> field Can be used to re-synchronize the GUI with the state of the hardware
Read-all button	Read from all registers in the <i>Register Map</i> summary and display the current state of the hardware
<i>Load Configuration</i> button	Load a configuration file from disk and register address/data values in the file
<i>Save Configuration</i> button	Save a configuration file to disk that contains the current state of the configuration registers
<i>Register Data</i> cluster	Manipulate individual accessible bits of the register highlighted in the register map summary
Individual register cluster with read or write register buttons	Perform a generic read or write command to the device shown in the <i>Block</i> drop-down box using the address and write data information

DAC39RF10 : FT7SKV9Q

Console Widgets Help

Register Map

Register Name	Address	Default	Mode	Size	Value
DAC39RF10					
CONFIG_A	0x0000	0x30	R/W	8	0x30
DEVICE_CONFIG	0x0002	0x00	R/W	8	0x00
CHIP_TYPE	0x0003	0x00	R	8	0x00
CHIP_ID	0x0004	0x00	R	8	0x00
CHIP_ID	0x0005	0x00	R	8	0x00
CHIP_VERSION	0x0006	0x00	R	8	0x00
VENDOR_ID	0x000C	0x00	R	8	0x00
VENDOR_ID	0x000D	0x00	R	8	0x00
SYSREF_CTRL	0x0080	0x40	R/W	8	0x40
SYSREF_POS	0x0090	0x00	R	8	0x00
SYSREF_POS	0x0091	0x00	R	8	0x00
SYSREF_POS	0x0092	0x00	R	8	0x00
SYSREF_ALIGN	0x00A0	0x00	R/W	8	0x00
SYSREF_CFG	0x00A1	0x00	R/W	8	0x00
JESD_EN	0x0100	0x00	R/W	8	0x00
JMODE	0x0101	0x00	R/W	8	0x00
JESD_M	0x0102	0x01	R/W	8	0x01
JCTRL	0x0103	0x03	R/W	8	0x03
SHMODE	0x0104	0x00	R/W	8	0x00
KM1	0x0105	0x1F	R/W	8	0x1F
RBD	0x0106	0x00	R/W	8	0x00
JESD_STATUS	0x0107	0x00	R/W	8	0x00
REFDIV	0x0108	0x30	R/W	8	0x30
MPY	0x0109	0x14	R/W	8	0x14

Register : CONFIG_A [0x0000]

Block: DAC39RF10

Register Address: 0x0000 Register Value: 0x30

Register Name: CONFIG_A

Current Register: Write Read All Block Registers: To Default Read All

Register Description: CONFIG_A [0x0000]

Configuration A (default: 0x30)
[7] SOFT_RESET
Setting this bit causes a full reset of the chip and all SPI registers (including CONFIG_A). This bit is self-clearing and will always read zero. After writing this bit, the part may take up to 150ns to reset. During this time, do not perform any SPI transactions.

Serial #: FT7SKV9Q
TCP Port: 11000

EVM Ready

command line interface

TEXAS INSTRUMENTS

DAC39RF10 : FT7SKV9Q

Console Widgets Help

Load File Save File Clear Log

Console

```

LMK04828.write(0x140,0xFF)
LMK04828.write(0x11C,0x22)
LMK04828.write(0x11F,0x11)
LMK04828.write(0x11E,0xF0)
LMX1204.write(0x09,0x0010)
LMX1204.write(0x10,0x1200)
DAC39RF10.write(0x0000,0x80)
time.sleep(0.1)
DAC39RF10.write(0x0101,0x03)
DAC39RF10.write(0x0102,0x08)
DAC39RF10.write(0x0103,0x13)
DAC39RF10.write(0x0108,0x20)
DAC39RF10.write(0x0109,0x21)
DAC39RF10.write(0x010A,0x00)
DAC39RF10.write(0x010B,0x00)
DAC39RF10.write(0x0103,0x13)
DAC39RF10.write(0x0103,0x11)
DAC39RF10.write(0x01C2,0x01)
DAC39RF10.write(0x02E1,0x05)
DAC39RF10.write(0x02E3,0x00)
DAC39RF10.write(0x02E4,0x11)
DAC39RF10.write(0x02E8,0x00)
DAC39RF10.write(0x0723,0x1F)
DAC39RF10.write(0x0724,0x0F)
DAC39RF10.write(0x0725,0x1F)
DAC39RF10.write(0x0726,0x0F)
DAC39RF10.write(0x072E,0x14)
DAC39RF10.write(0x072F,0x14)
DAC39RF10.write(0x0739,0x14)
DAC39RF10.write(0x0100,0x01)
DAC39RF10.write(0x02E0,0x01)
  
```

LOG OF REGISTER WRITES

Serial #: FT7SKV9Q
TCP Port: 11000

EVM Ready

command line interface

TEXAS INSTRUMENTS

Figure 4-1. Register Map Tab

5 Troubleshooting the DAC39RF10EVM

Table 5-1 lists some troubleshooting procedures.

Table 5-1. Troubleshooting

Issue	Troubleshoot
General problems	<ul style="list-style-type: none"> Verify the test setup shown in Figure 3-1, and repeat the setup procedure as described in this document. Check power supply to EVM and TSW14J59EVM. Verify that the power switch is in the on position. Check signal and clock connections to EVM. Visually check the top and bottom sides of the board to verify that nothing looks discolored or damaged. Make sure the board-to-board FMC+ connection is secure. Try pressing the CPU_RESET button on the TSW14J59EVM. Also try clicking <i>Instrument Options</i> → <i>Reset Board</i> after changing the DAC configuration. Try power-cycling the external power supply to the EVM, and reprogram the DAC, LMX and LMK devices.
TSW14J59 LEDs are not correct	<ul style="list-style-type: none"> Verify the settings of the configuration switches on the TSW14J59EVM. Verify that the clock going to the CLK input is connected and the appropriate LEDs are blinking. Verify that the DAC device internal registers are configured properly. If LEDs are not blinking, reprogram the DAC EVM devices. Try pressing the CPU_RESET button on the TSW14J59EVM. Try clicking SEND button in HSDC Pro again.
Configuration GUI is not working properly	<ul style="list-style-type: none"> Verify that the USB cable is plugged into the EVM and the PC. Check the computer device manager and verify that a <i>USB serial device</i> is recognized when the EVM is connected to the PC. Verify that the yellow EVM <i>Status</i> LED light in the lower right corner of the GUI is lit. If it is not lit, try restarting the GUI and reconfiguring the devices.
Configuration GUI is not able to connect to the EVM	<ul style="list-style-type: none"> Use the free FT_PROG software from FTDI chip and verify that the onboard FTDI chip is programmed with the product description <i>ADC12DJxx00RF</i>.
DAC output looks incorrect, distorted or there is no output.	<ul style="list-style-type: none"> Verify that the TSW14J59EVM is properly connected to the PC with a USB-C cable and that the board serial number is properly identified by the HSDC software. Check that the proper DAC device mode is selected. The mode should match in HSDC Pro and the DAC GUI. Check that the configuration parameters are properly configured. Select <i>Instrument Options</i> → <i>Download Firmware</i> and download 'TSW14J59REVB_DAC_64B66B_FIRMWARE.bit'. Try to send again.
Output power looks low	<ul style="list-style-type: none"> Check that the spectrum analyzer is set to proper settings. SMA connector is properly connect to the DAC output and Spectrum analyzer.

6 References

This section provides references to technical documents and user's guides.

6.1 Technical Reference Documents

- [DAC39RF10 device data sheet](#)
- [TSW14J59EVM user's guide](#)
- [High-Speed Data Converter Pro GUI User's Guide](#), also available in the help menu of the software
- [LMK04828 data sheet](#)
- [LMX1204 data sheet](#)
- FTDI USB to Serial Driver Installation Manual (www.ftdichip.com/Support/Documents/InstallGuides.htm)

6.2 TSW14J59EVM Operation

Refer to the [TSW14J59EVM user guide](#) for configuration and status information.

7 Appendix

This appendix provides settings for optional ADC device configuration in HSDC Pro.

7.1 Customizing the EVM for Optional Clocking Support

The DAC39RF10EVM can be clocked using 3 different methods: LMX->DACCLK | LMX/LMK-> FPGA option, EXT->DACCLK | LMX/LMK-> FPGA option and EXT->DACCLK | LMK-> FPGA option.

7.1.1 LMX->DACCLK | LMX/LMK-> FPGA option (Default)

By default, the EVM is configured to use LMX->DACCLK | LMX/LMK->FPGA clock option. The user provide a single high frequency(8-10dBm) signal to an SMA labeled LMX CLKp. This signal is routed to LMX1204 which generates the buffered DACCLK signal, low frequency DAC SYSREF signal, FPGA reference clocks and FPGA SYSREF signal. The FPGA reference clocks and FPGA SYSREF signal are feed into the CLKIN1 and CLKIN0 of LMK04828. The LMK04828 is used in clock distribution mode and provides several copies/divided down version of FPGA reference clock and FPGA SYSREF signal.

The EVM can be configured to use LMX->DACCLK | LMX/LMK->FPGA clock option with the following steps:

1. Modify the hardware:
 - a. Remove C136 and C139, populate C141 and C142.
 - b. Remove C134 and C135, populate C138 and C140
 - c. Remove C75 and C76, populate C73 and C74

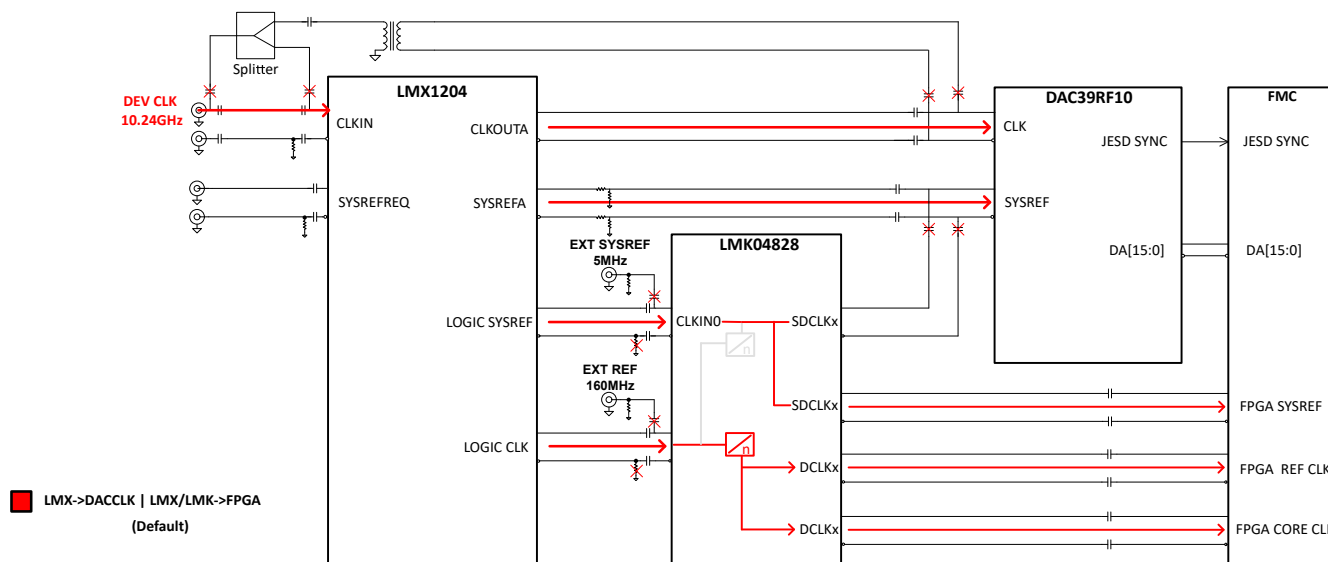


Figure 7-1. LMX->DACCLK | LMX/LMK->FPGA Clocking System Block Diagram

7.1.2 EXT->DACCLK | LMX/LMK-> FPGA Clocking Option

The DAC39RF10EVM can be configured to use EXT->DACCLK | LMX/LMK-> FPGA Clocking option. Similar to above use case The user provide a single high frequency (10-15 dBm) signal to an SMA labeled LMX CLKp. This signal is routed through the splitter to Balun and LMX1204. The Balun converts the single ended signal into differential and is used to clock the DAC. The second output from the splitter is used by LMX1204 which generates the low frequency DAC SYSREF signal, FPGA reference clocks and FPGA SYSREF signal. The FPGA reference clocks and FPGA SYSREF signal are feed into the CLKIN1 and CLKIN0 of LMK04828. The LMK04828 and is used in clock distribution mode and provides several copies/divided down version of FPGA reference clock and FPGA SYSREF signal. **Figure 7-2** shows the block diagram of clocking option:

The EVM can be configured to use onboard clocking option with the following steps:

- Remove C141 and C142, populate C136 and C139
- Remove C138 and C140, populate C134 and C135
- Remove C75 and C76, populate C73 and C74

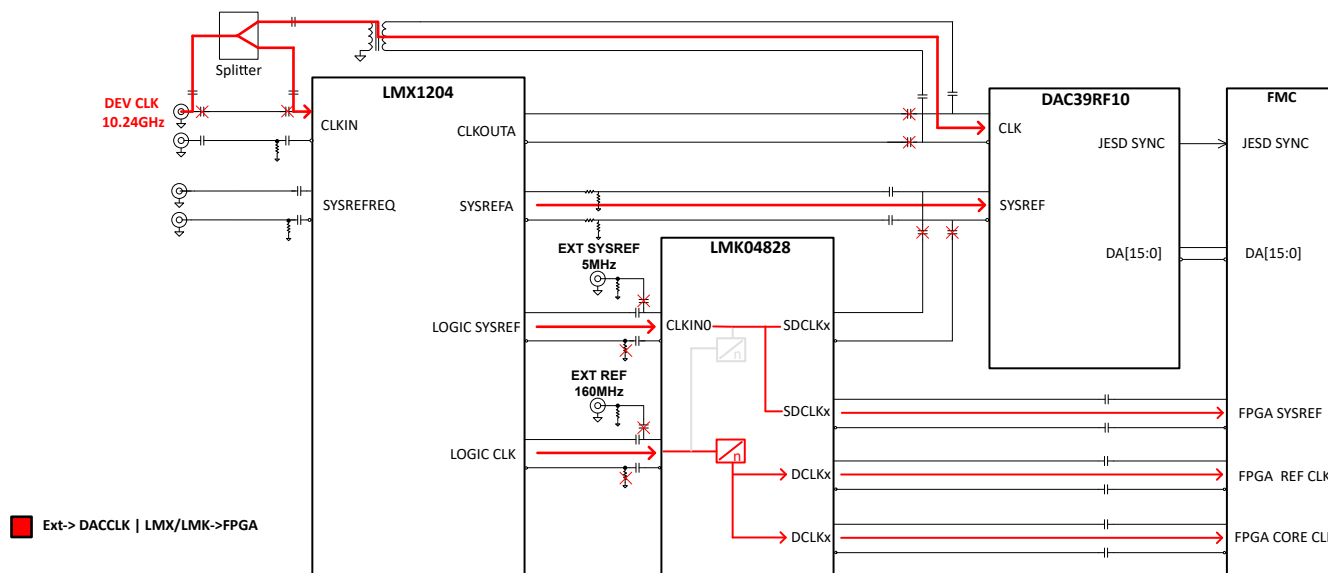


Figure 7-2. EXT->DACCLK | LMX/LMK-> FPGA Clocking System Block Diagram

7.1.3 EXT->DACCLK | LMK-> FPGA Clocking Option

The DAC39RF10EVM can be configured to use EXT->DACCLK | LMK-> FPGA Clocking option. In this use case, the user provide a two clock signal. A high frequency(10-15dBm) signal to an SMA labeled LMX CLKp. This signal is routed though the splitter to Balun and LMX1204. The Balun converts the single ended signal into differential and is used to clock the DAC. The second low frequency signal is CLKIN1 input of LMK04828. The LMK04828 is used to generates the low frequency DAC SYSREF signal, FPGA reference clocks and FPGA SYSREF signal. The LMK04828 is used in clock distribution mode and provides several copies/divided down version of FPGA reference clock and FPGA SYSREF signal. Figure 7-3 shows the block diagram of external reference clocking option:

The EVM can be configured to use external reference clocking option with the following steps:

- Remove C141 and C142, populate C136 and C139
- Remove C138 and C140, populate C134 and C135
- Remove C65 and R64, populate C64 and R66
- Remove C73 and C74, populate C75 and C76

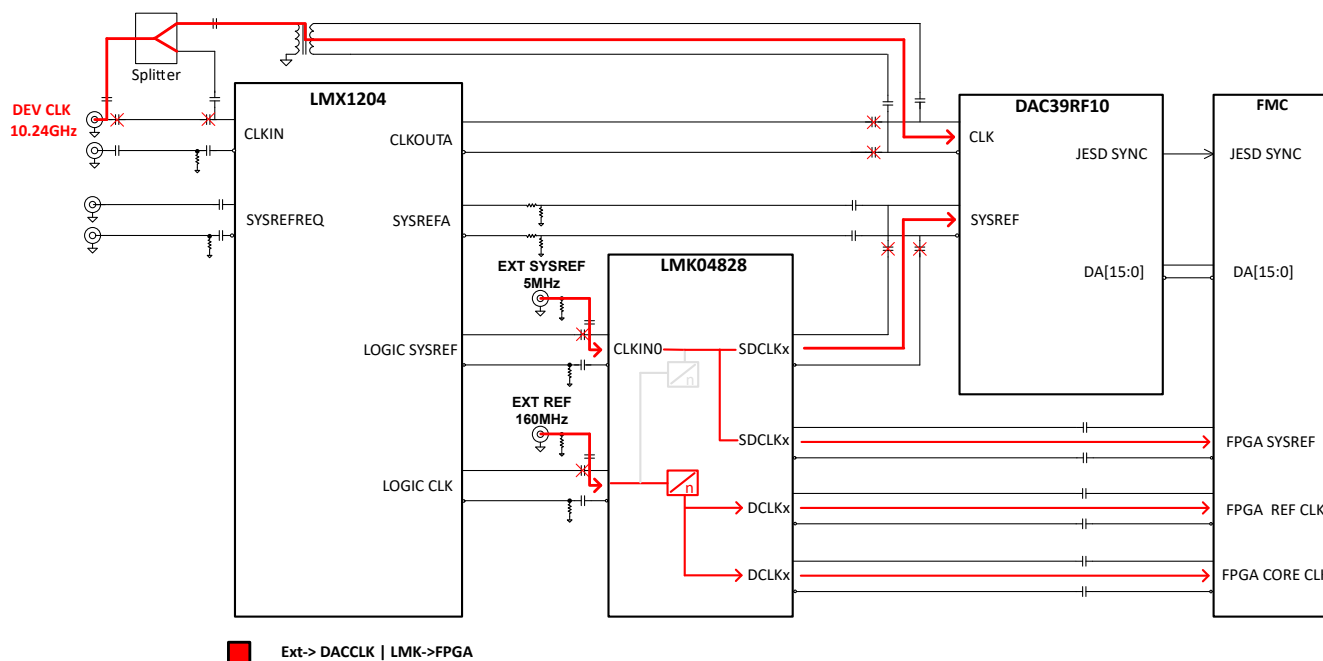


Figure 7-3. External Reference Clocking System Block Diagram

7.2 Signal Routing

Table 7-1 provides the signal routing details for the DAC39RF10EVM.

Table 7-1. DAC39RF10EVM Signal Routing

JESD204C Inputs	FMC(+) Pi	FMC(+) Signal Names ⁽¹⁾
Lane0	A38,A39	DP5_C2M_INV
Lane1	B36,B37	DP6_C2M_INV
Lane2	B32,B33	DP7_C2M_INV
Lane3	A34,A35	DP4_C2M_INV
Lane4	Y30,Y31	DP13_C2M_INV
Lane5	A30,A31	DP3_C2M_INV
Lane6	Z28,Z29	DP12_C2M_INV
Lane7	B28,B29	DP8_C2M_INV
Lane8	Y6,Y7	DP21_C2M_INV
Lane9	C2,C3	DP0_C2M_INV
Lane10	Z8,Z9	DP20_C2M_INV
Lane11	A22,A23	DP1_C2M_INV
Lane12	Z24,Z25	DP10_C2M_INV
Lane13	B25,B26	DP9_C2M_INV
Lane14	Y26,Y27	DP11_C2M_INV
Lane15	A26,A27	DP2_C2M_INV

(1) Red items with _INV in the signal name are inverted with respect to standard FMC polarity.

7.3 Analog Outputs

Table 7-2 provides the different settings for setting the analog inputs path.

Table 7-2. Analog Output Path

Coupling	Output	SMA to Use	Installed componets	DNI components
AC (default)	S/E Balun (500kHz to 9GHz)	OUTAp and OUTBp	R180, R185, R193, R198 = 8.33 Ω and C176, C184 = 0.1 μ F	R178, R179, R189,R190, R191,R192, R202,R203
AC	Differential	OUTAp, OUTAn, OUTBp and OUTBn	R178, R179, R189,R190, R191,R192, R202,R203 = 0.1 μ F	R180, R185, R193, R198 C176, C184

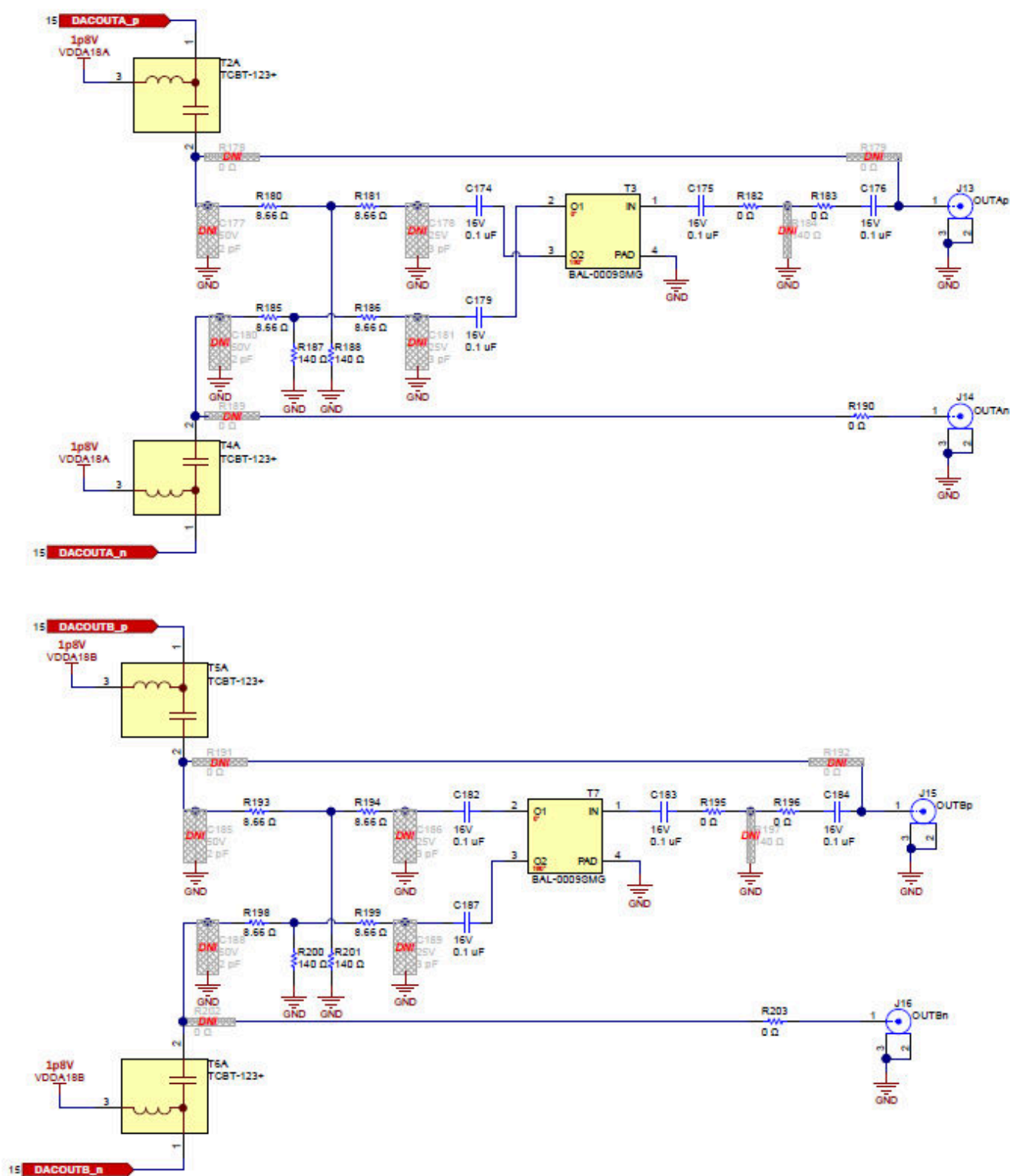


Figure 7-4. Analog Outut Path

A 3 dB attenuation pad is added between the inputs and the ADC. The 3 dB pad helps with the flatness of the frequency response.

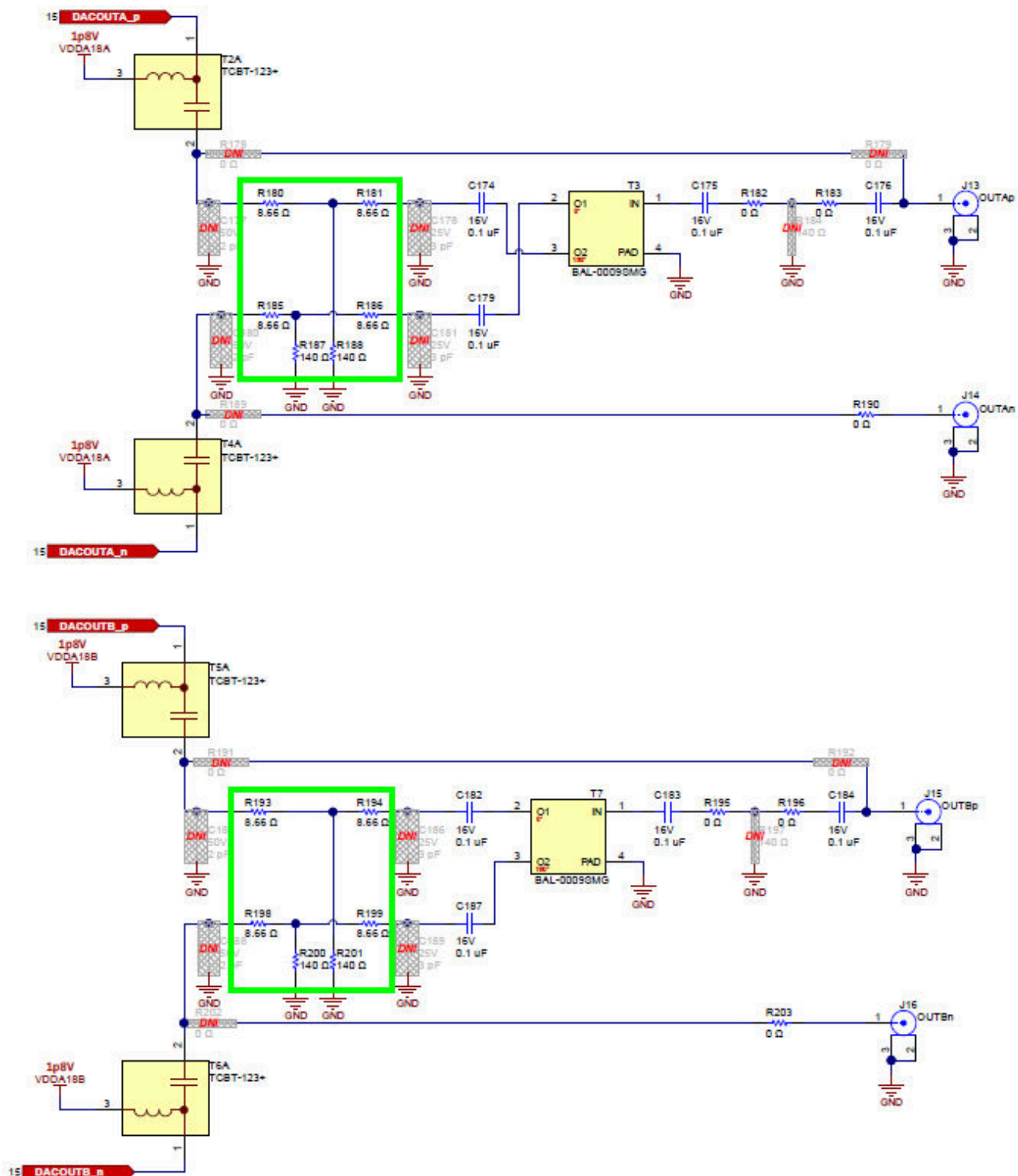


Figure 7-5. 3 dB attenuation pad

7.4 Jumpers and LEDs

[Table 7-3](#) shows the jumper settings and [Table 7-4](#) shows the LED functionality.

Table 7-3. Jumper Settings

Label	Description	Function
J12	Selects the source for SPI signals	Uninstalled(default): SPI signals to various device on the EVM are controlled by the FTDI dongle board. Installed: SPI signals from FMC+ connector are controlling the devices on the EVM(This feature will be supported on next rev of the board).

Table 7-4. LEDs

Label	Function
D3	12 V power indicator

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FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

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This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

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Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
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