

ADS1282 Performance Demonstration Kit Evaluation Module



Description

The ADS1282EVM-PDK is a platform for evaluating the performance of the ADS1282, a high performance, 31-bit, 2-channel, 4kSPS Delta-Sigma analog to digital converter (ADC) with a programmable gain amplifier (PGA). The ADS1282 board includes the ADS1282 and all the peripheral analog circuits and components required to extract optimum performance from the ADC. The evaluation kit includes the ADS1282 evaluation board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over universal serial bus (USB) for data capture, configuration, and analysis.

Get Started

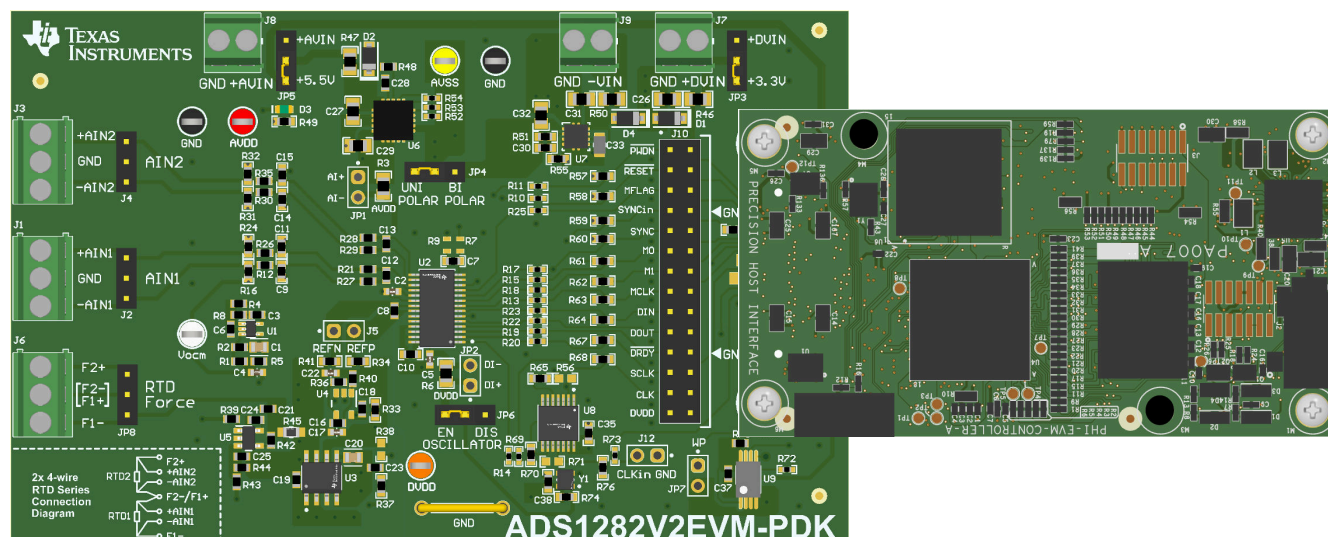
1. Order ADS1282EVM-PDK from ti.com.
2. Download and install the [ADS1282EVM-PDK-GUI](#) software.
3. Connect the ADS1282 evaluation module (EVM) to the computer with the included USB cable.
4. Launch the ADS1282 EVM GUI from the start menu.
5. Refer to the [ADS1282 datasheet](#) for device details.
6. Visit the [E2E™ forums](#) for support and questions.

Features

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS1282
- The PHI controller provides a convenient communication interface and power to the ADS1282 over USB 2.0 (or higher) for digital input and output
- Easy-to-use evaluation software for 64-bit Microsoft® Windows® 10 or 11 operating system
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis
- Input terminal blocks that enable easy measurement of many types of differential analog sensors, bridge sensors and resistance temperature detectors (RTDs)

Applications

- Energy exploration
- Seismic monitoring
- High-accuracy instrumentation



1 Evaluation Module Overview

1.1 Introduction

The ADS1282 is a high-performance, single-chip, delta-sigma analog-to-digital converter (ADC) with an integrated, low-noise programmable gain amplifier (PGA) and two-channel input multiplexer (MUX). The ADS1282 is an excellent choice for the demanding needs of energy exploration and seismic monitoring environments. The PHI board primarily serves three functions:

- Provides a communication interface from the evaluation module (EVM) to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS1282
- Supplies power to the active circuitry on the ADS1282EVM board

This user's guide describes the characteristics, operation, and use of the ADS1282EVM. The ADS1282EVM enables the evaluation of the device through a USB interface. This EVM user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1282EVM.

1.2 Performance Development Kit Contents

The ADS1282 EVM performance development kit (PDK) includes the following features (Figure 1-1):

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS1282.
- The PHI controller, which provides a convenient communication interface to the ADS1282 over USB 2.0 (or higher).
- Easy-to-use evaluation software for use with 64-bit Microsoft Windows 10 or 11 operating systems.
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, and custom configuration of the ADS1282. This suite also has a provision for exporting data to a text file for post-processing.

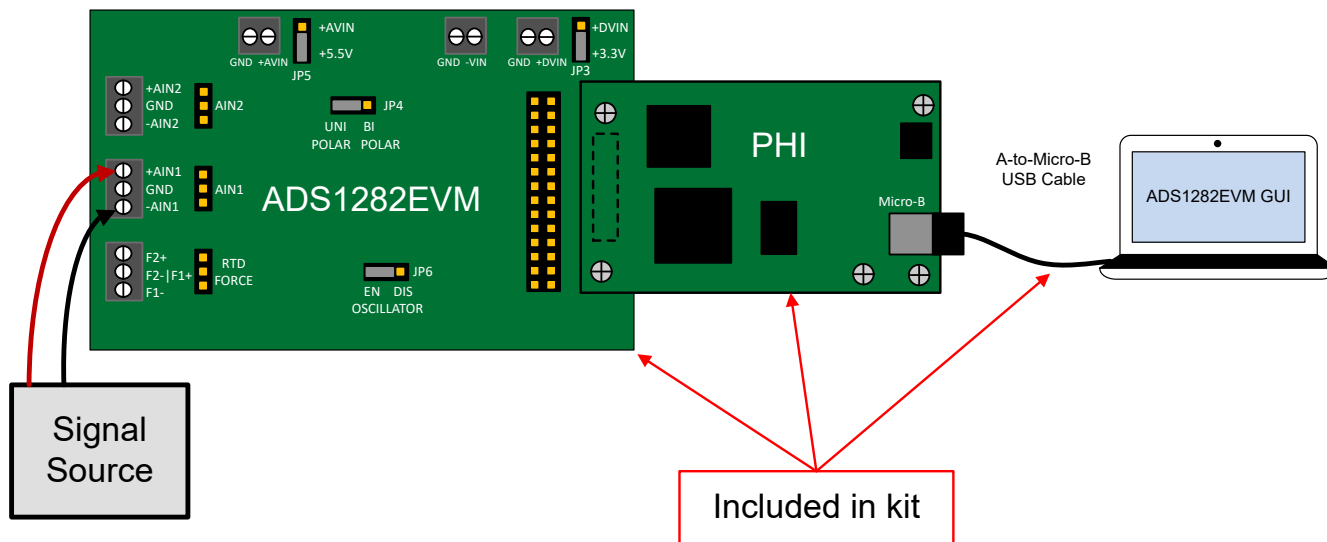


Figure 1-1. System Connection for Evaluation

1.3 Specification

The following specifications shown in [Table 1-1](#) are applicable to the ADS1282EVM and the PHI board.

Table 1-1. ADS1282EVM-PDK Specifications

PARAMETER	CONDITIONS	VALUE
Temperature	Recommended operating free-air temperature range, T_A	$15^{\circ}\text{C} \leq T_A \leq 35^{\circ}\text{C}$
Analog supply Input range	Recommended voltage range for terminal block J9 (-Vin) to GND (bipolar only) Recommended voltage range for terminal block J8 (+AVin) to GND (bipolar or unipolar)	$-6.5\text{V} \leq -\text{Vin} \leq -3\text{V}$ $5.5\text{V} \leq +\text{AVin} \leq 6.5\text{V}$
Digital supply input range	Recommended voltage range for terminal block J7 (+DVin) to GND	$1.65\text{V} \leq +\text{DVin} \leq 3.6\text{V}$
Analog input voltage (AIN1 and AIN2)	Absolute input voltage to GND (unipolar, AVDD = 5.3V, AVSS = GND)	$0.7\text{V} \leq \text{AINP} \leq 4.0\text{V}$
		$0.7\text{V} \leq \text{AINN} \leq 4.0\text{V}$
	Absolute input voltage to GND (bipolar, AVDD = +2.8V, AVSS = -2.5V)	$-1.8\text{V} \leq \text{AINP} \leq 1.5\text{V}$
		$-1.8\text{V} \leq \text{AINN} \leq 1.5\text{V}$
External clock	Recommended frequency range for J12 (f_{CLK})	2MHz to 8.192MHz

1.4 Device Information

[Table 1-2](#) shows some of the main ADS1282 specifications. Please refer to the [ADS1282 datasheet](#) for complete specifications.

Table 1-2. ADS1282 Specifications

DEVICE SPECIFICATION	VALUE
Package size	9.7mm × 6.4mm
Operating temperature range	-40°C to 85°C
AVSS to DGND supply voltage	-2.6V to 0V
AVDD to AVSS supply voltage	4.75V to 5.25V
DVDD to DGND supply voltage	1.65V to 3.6V
Reference input voltage ($V_{\text{REF}} = \text{VREFP} - \text{VREFN}$)	0.5V to $(\text{AVDD} - \text{AVSS}) + 0.2\text{V}$

[Figure 1-2](#) shows the block diagram of the ADS1282 ADC including the two-channel input MUX and PGA.

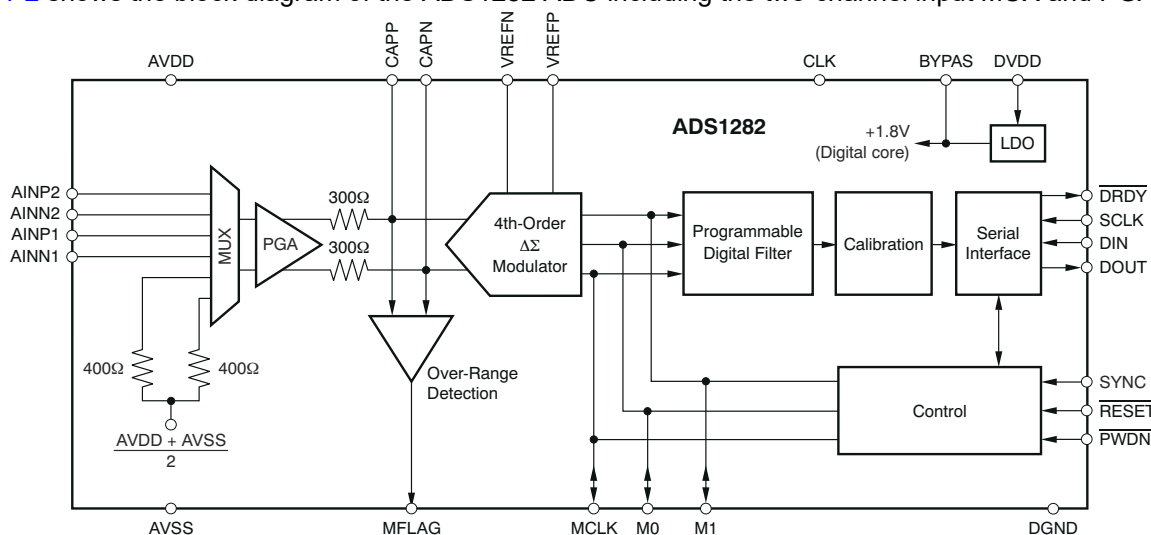


Figure 1-2. ADS1282 Block Diagram

2 Hardware

The ADS1282EVM is designed for easy interfacing with analog sources. This section covers the details of the front-end circuit, including shunt configurations for different power supply configurations, clock sources, and board connectors for signal sources.

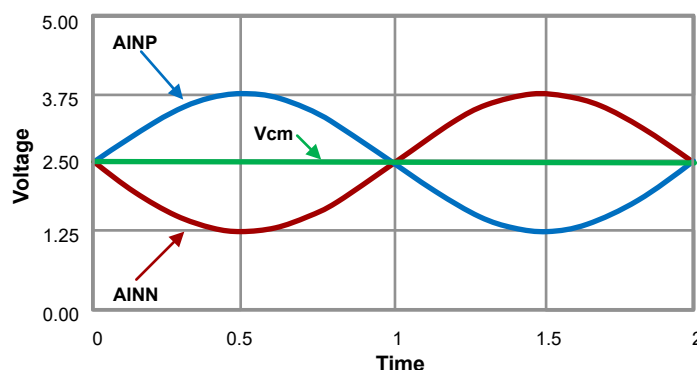
2.1 EVM Analog Input Options

Connect differential analog input signals to pins +AINx and -AINx (x denoting channels 1 and 2) on terminal blocks J3 and J1 as shown in [Figure 4-1](#). The EVM common-mode amplifier circuit shown in [Figure 2-2](#) uses 20k Ω resistors to bias the differential inputs to the correct mid-scale voltage when using a floating input source. This configuration is useful for floating sensors such as geophones and hydrophones.

Set the common-mode voltage as follows if the differential input source has an established common-mode voltage relative to GND: +2.5V for the default unipolar power configuration (AVDD = +5.3V, AVSS = GND); or 0V for the optional bipolar power configuration (AVDD = +2.8V, AVSS = -2.5V).

Each of the differential input pairs accepts up to a 5V_{PP} differential signal with a common-mode voltage of +2.5V (default unipolar supply) or 0V (optional bipolar supply). The [REF54500](#) provides the EVM default 5V reference voltage. Refer to [Figure 2-1](#) for details on the recommended voltage span for the AINP and AINN inputs with respect to GND.

Differential 5Vpp, 2.5V offset, Unipolar supply configuration



Differential 5Vpp, 0V offset, Bipolar supply configuration

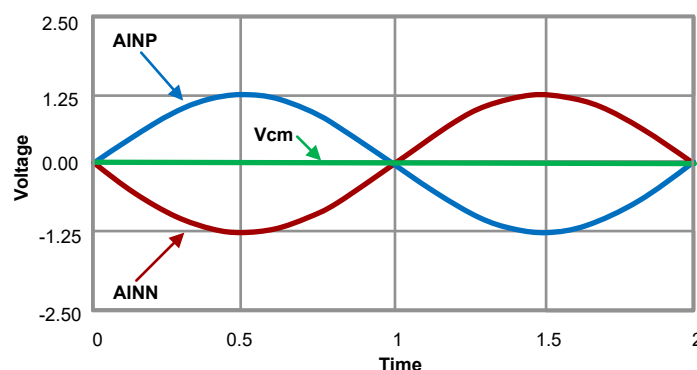


Figure 2-1. Maximum Input Signal Range ($V_{REF} = 5V$)

2.2 Common-Mode Amplifier

Figure 2-2 shows the OPA379 op-amp circuit used to generate the common-mode voltage that the ADS1282 requires from the input signals. The circuit output, V_{ocm} , provides a voltage that is mid-scale with respect to the selected input range of the ADS1282. In unipolar mode, V_{ocm} is +2.5V relative to ground. In bipolar mode, V_{ocm} is 0V relative to ground.

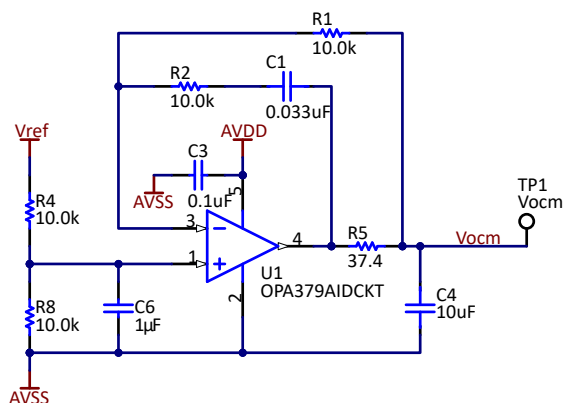


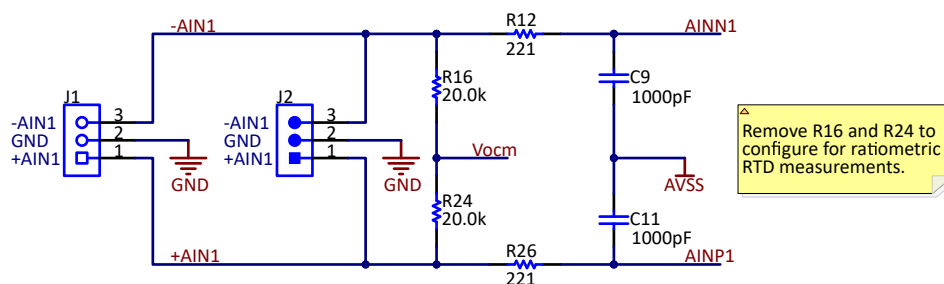
Figure 2-2. Common-Mode Amplifier

2.3 Analog Input Circuit

Figure 2-3 shows the front-end circuit to ADC inputs AIN1 and AIN2. Each of the analog inputs include common mode filters set to a cutoff frequency of 750kHz to reduce external noise.

Vocm supplies a DC shift to the differential inputs connected to terminal blocks J1 (AIN1) and J3 (AIN2), or optionally to headers J2 (AIN1) and J4 (AIN2), to establish a mid-scale input bias voltage for the ADS1282. In unipolar mode (AVDD=+5.3V, AVSS=GND), the bias Vocm is equal to +2.5V. In bipolar mode (AVDD = +2.8V, AVSS = -2.5V), the bias Vocm is equal to 0V. Use this Vocm voltage to establish the proper mid-scale common mode voltage required by the ADS1282 for differential transducers such as geophones and hydrophones.

Analog Input 1



Analog Input 2

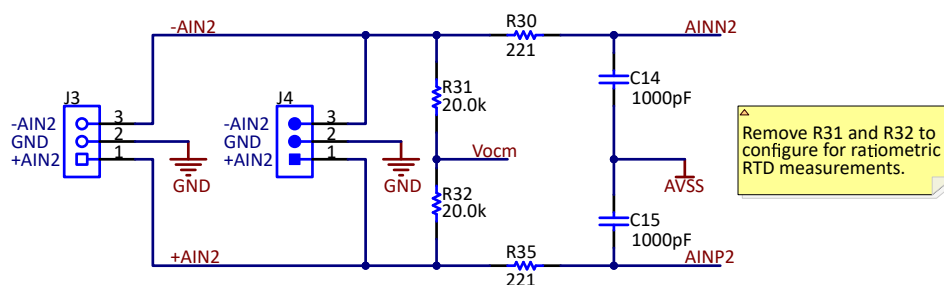


Figure 2-3. Analog Input Circuit

2.4 RTD Current Source

Figure 2-4 shows a constant 1mA current source that can be used for biasing resistance temperature detectors (RTDs) in precision temperature measurement applications. This current source is realized using amplifier U5, an OPA196 precision amplifier. Precision resistor R45 establishes a 1V reference input to the ADS1282 and sets the current level. Increase the value of resistor R45 if the system requires a lower RTD current bias. For example, changing R45 from 1k Ω to 10k Ω sets the bias current to 100 μ A.

The current source output is available on terminal block J6 or header JP8. Connect one or two RTDs in series from terminal block J6 pin 1 (F2+) to terminal block J6 pin 3 (F1-). Terminal block J6 pin 2 (F2-, F1+) is included as a convenient point to connect two RTDs in series, as shown in Figure 2-5.

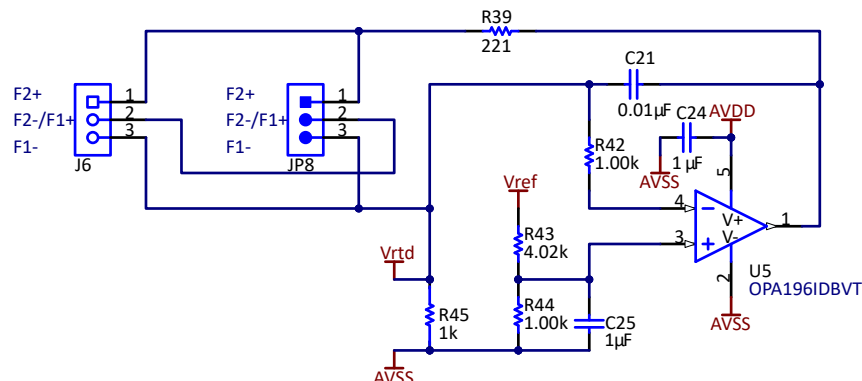


Figure 2-4. RTD Current Source

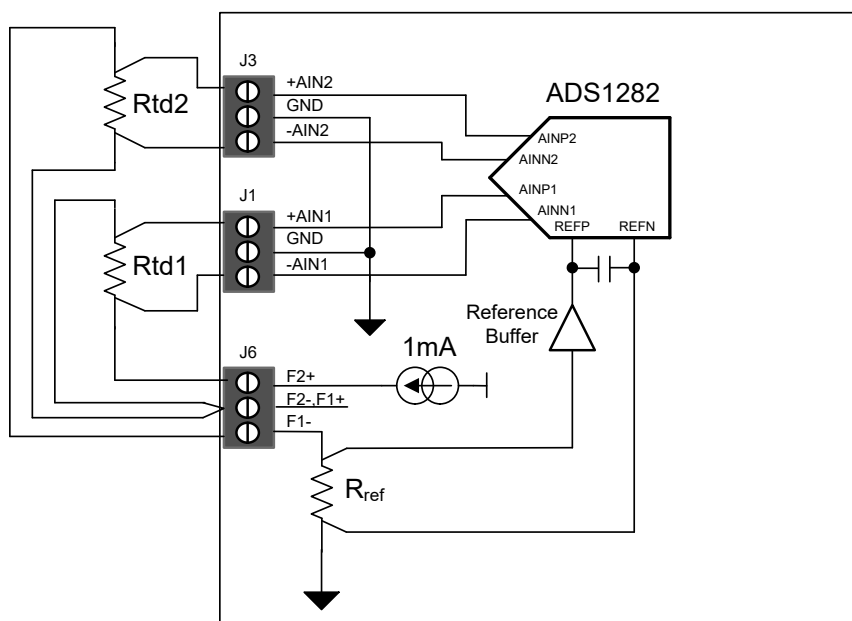


Figure 2-5. External RTD Connections

2.5 Voltage Reference

Figure 2-6 shows the REF54500 voltage reference circuit. By default, the REF54500 connects to the ADS1282 through 0Ω resistors R33, R34 and R41.

Use an external reference source in place of the REF54500 by removing resistors R34 and R41 and installing header J5. The positive terminal of the voltage reference connects to pin 2 on header J5, and the negative terminal to pin 1 on header J5. The pins of header J5 can also be used as test points for the onboard REF54500.

Install amplifier U4, OPA196, and remove resistor R33 to configure the ADS1282 EVM for ratiometric RTD measurements. This configuration uses amplifier U4 as a reference buffer with a nominal 1V level established by resistor R45. Refer to Figure 2-4 for more information.

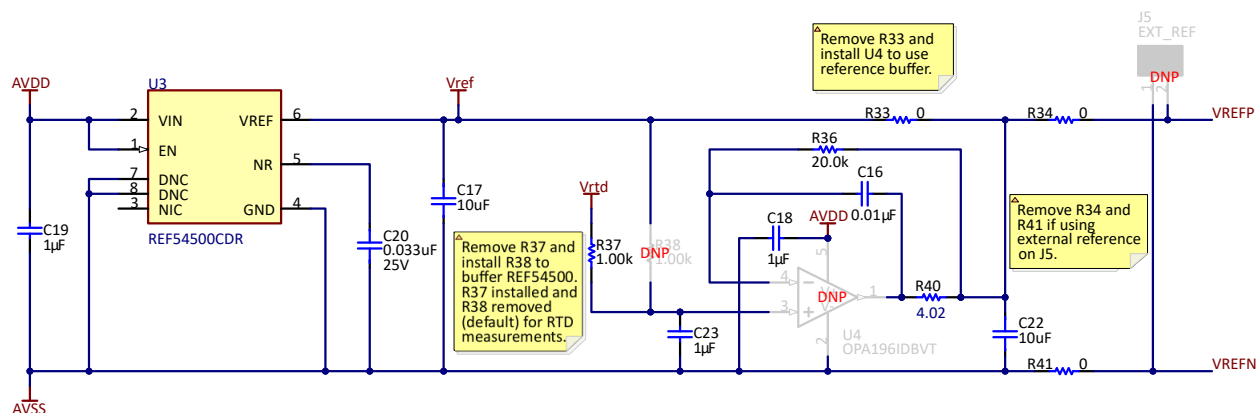


Figure 2-6. Onboard Voltage Reference

2.6 ADC Connections and Decoupling

Figure 2-7 shows all connections to the ADS1282 data converter (U2). Each power supply connection has a 10 μ F decoupling capacitor. Make sure these capacitors are physically close to the device and have a good connection to the AVSS or GND plane. AVSS is the ADS1282 analog ground that can be connected to a -2.5V supply for bipolar operation or directly to the GND plane for unipolar operation.

The supply connections also have a series 0.1 Ω resistor. These resistors facilitate current measurement for the ADC. For more accurate measurements, remove the 0.1 Ω resistors and install headers JP1 and JP2. Use a high accuracy digital multimeter (DMM) to directly measure the ADS1282 supply current using these headers.

Each digital pin has a 49.9 Ω series resistor. These resistors smooth the edges of the digital signals to provide minimal overshoot and ringing. These resistors are optional but suggested if space allows to minimize digital noise coupling into the ADC inputs.

Each of the analog inputs include a differential filter with a cutoff frequency set to 36kHz to reduce external noise.

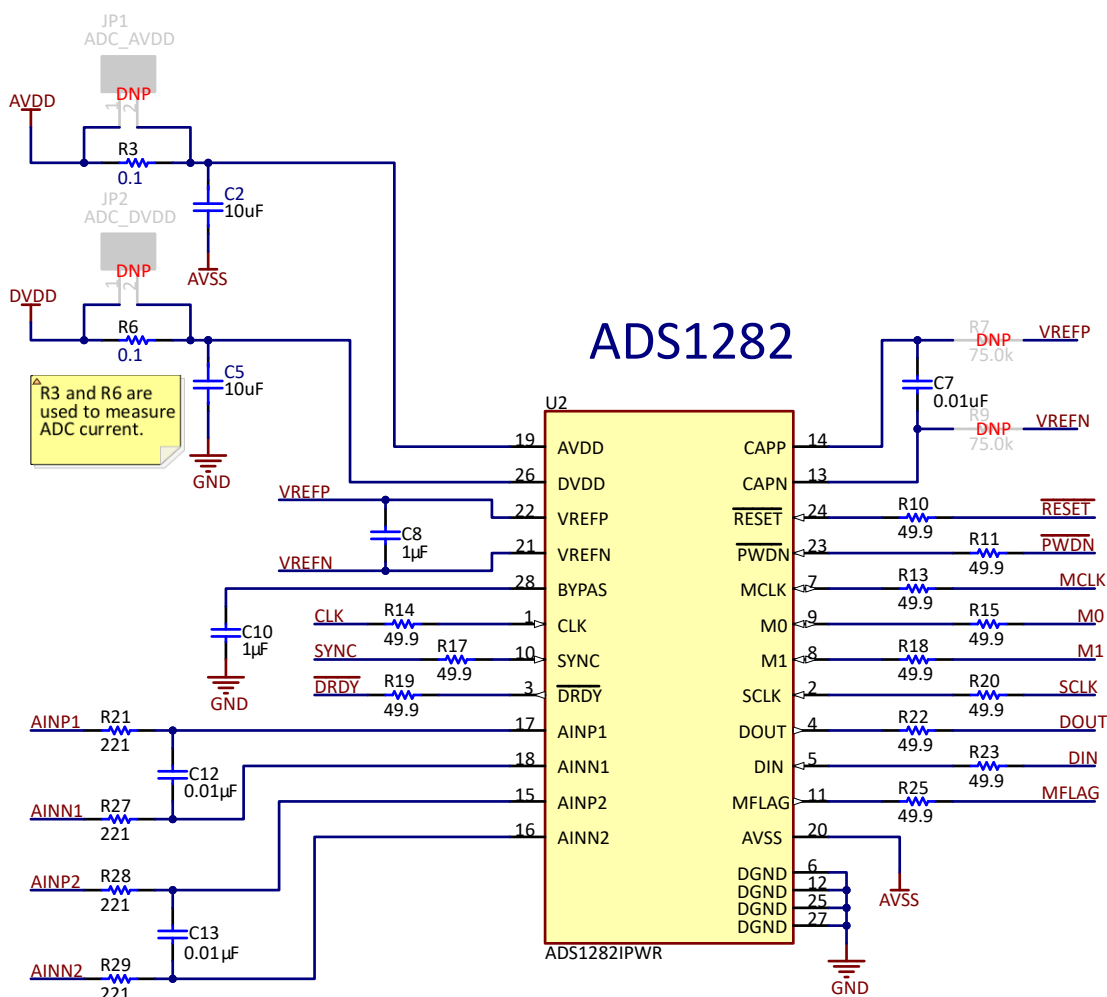


Figure 2-7. ADC Connections and Decoupling

2.7 Power Supplies

By default, the PHI powers the ADS1282 EVM circuitry from the computer power supply through USB with AVDD set to +5.3V and AVSS connected to GND. This configuration does not require an external power supply and only supports unipolar operation such that the input signals must be in the range of 0.7V to 4.0V with respect to GND.

The EVM also supports bipolar operation. Enable bipolar operation for the ADS1282 EVM by using an external power supply that can source 100mA or greater. To do so, connect +5.5V up to +6.5V to terminal block J8 (+AVIN) and -6.5V up to -3V to terminal block J9 (-VIN). Also, install a shunt to position 2-3 on header JP4 (BIPOlar) to enable bipolar operation and install a shunt to position 1-2 on header JP5 (+AVIN) to use the external supply. In this configuration, the voltage level for AVDD does not need to be changed. The +5.3V linear regulator is referenced to AVSS, so setting AVSS = -2.5V also changes AVDD to +2.8V with respect to GND. Refer to [Figure 2-8](#) and [Figure 2-9](#) for details.

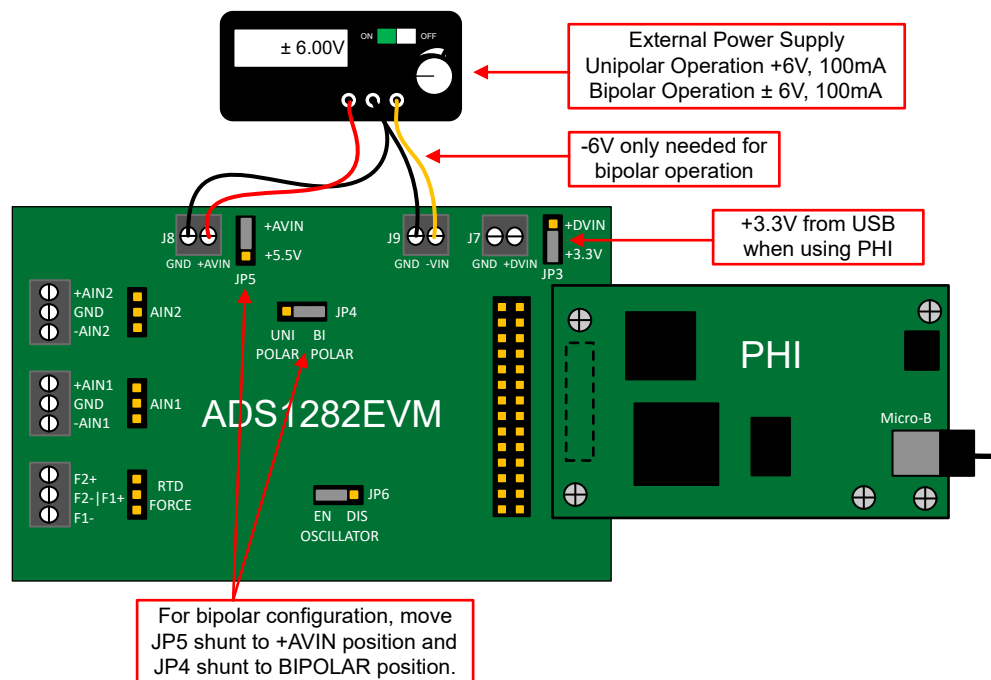
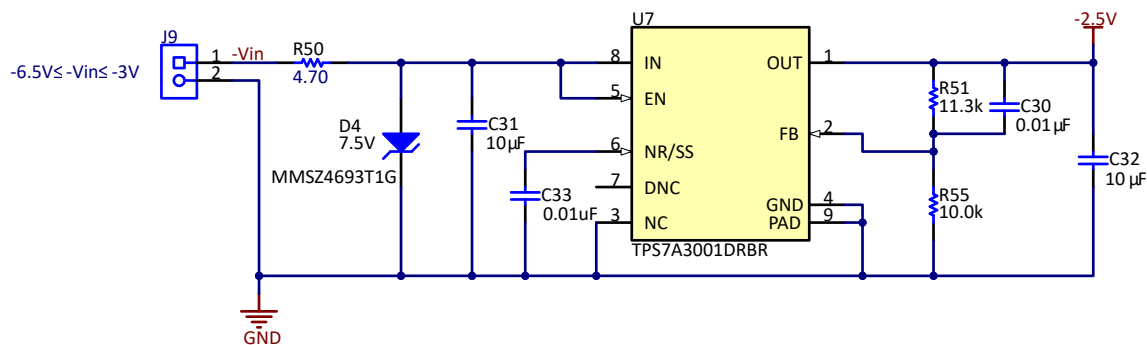


Figure 2-8. Bipolar Power Connections

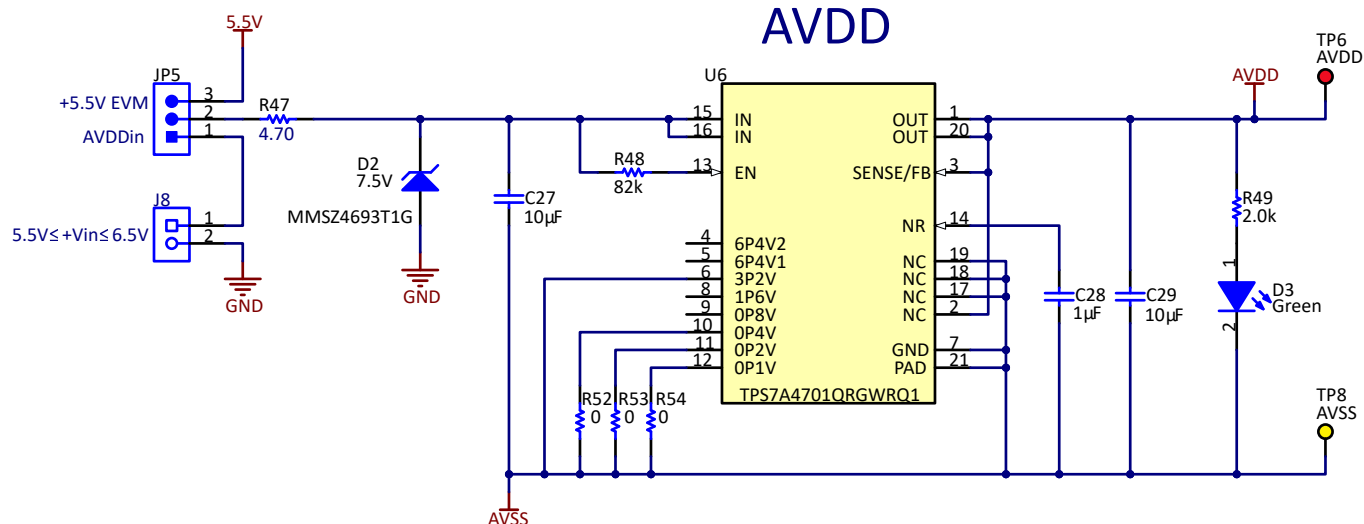
An external power supply can also be used for DVDD by connecting +1.65V up to +3.6V to terminal block J7 (+DVIN). The DVDD supply does not use an LDO and must meet the ADS1282 DVDD specifications. Install a shunt to position 1-2 of header JP3 (+DVIN) to use the external power supply.

[Figure 2-9](#) shows how the ADS1282 5.3V AVDD and -2.5V AVSS supplies are generated using low dropout (LDO) linear regulators. The [TPS7A4701](#) LDO regulates AVDD to 5.3V with respect to AVSS. The 5.3V LDO output is used for the AVDD connections and can be reprogrammed to different output voltages using R52, R53 and R54. The [TPS7A30](#) LDO generates the -2.5V rail for AVSS. This LDO is only supplied by external power on header J9 and must be used when bipolar operation is required.

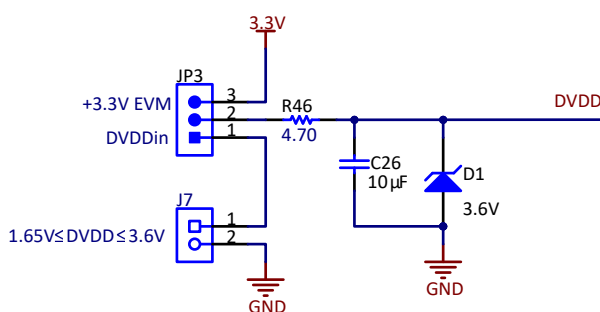
-2.5V



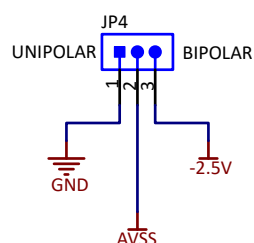
AVDD



DVDD



AVSS Select



Unipolar: AVSS=GND

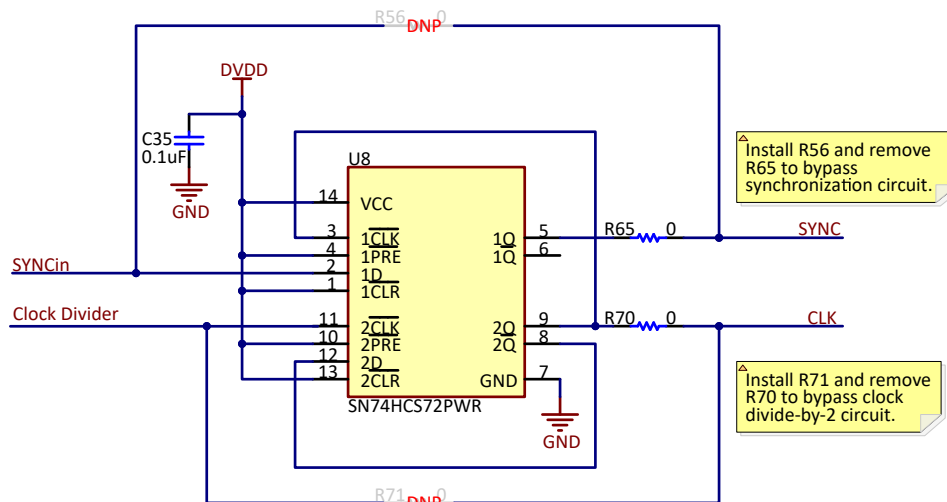
Bipolar: AVSS=-2.5V

Figure 2-9. External Power Supply Connections

2.8 SYNC / Clock Divide Circuit

Figure 2-10 shows the flip-flop circuit used for ADS1282 synchronization to external events or other ADS1282 devices. This synchronization circuit makes sure the setup and hold times of the ADS1282 SYNC input pin are met when using an asynchronous external trigger event. The circuit utilizes the SN74HCS72 Schmitt-Trigger input, negative-edge-triggered, dual D-type flip-flop (U8). The SYNCin input latches on the falling edge of the clock to meet the ADS1282 timing requirements.

The EVM uses the second D-type flip-flop as a divide-by-2 for the clock source. This configuration requires an EVM input clock source two times the desired ADC clock value, but allows for a much wider clock duty cycle when using an external clock source.



CLK DivideBy2 allows use of 8.192MHz OSC

Figure 2-10. Flip-Flop Sync Circuit

2.9 Clocking

Figure 2-11 shows the clocking circuit for the ADS1282 EVM using the low-power CDC6C (Y1) 8.192MHz oscillator. This oscillator is enabled or disabled by shunt JP6, with the default setting in the 2-3 position (ENABLE). This clock is routed through a divide-by-2 flip-flop and then to the main clock input (CLK pin) of the ADS1282, providing the recommended 4.096MHz clock source. The EVM includes a 49.9Ω series resistor on the clock output to reduce overshoot and ringing on clock transitions.

Moving shunt JP6 to the 1-2 position (DISABLE) allows an external clock to be supplied on header J12 (not populated). Use a CMOS square-wave signal with an amplitude equal to DVDD (+3.3V when using PHI) and a frequency that is 2x the specified range for the ADS1282 (2MHz up to 8.192MHz).

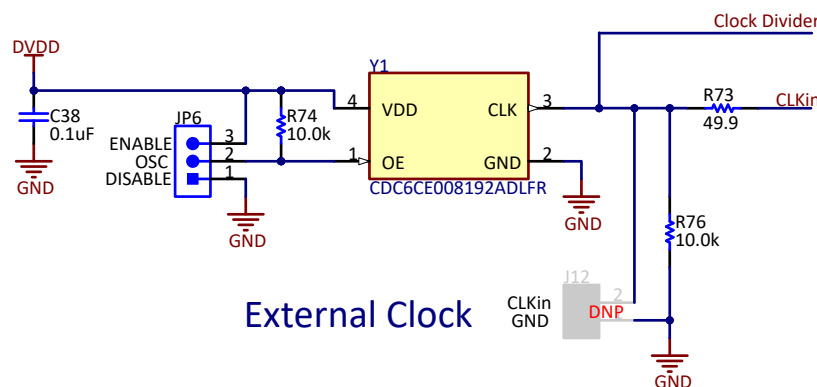


Figure 2-11. Clocking

2.10 Serial Interface

Figure 2-12 shows the digital connections between the ADS1282 and the PHI. The ADS1282 uses SPI serial communication in mode 0 (CPOL = 0, CPHA = 0) to configure the internal registers. The signal bank header J10 provides test points for the ADS1282EVM digital signals or connection to an external controller when using the ADS1282EVM without the PHI attached.

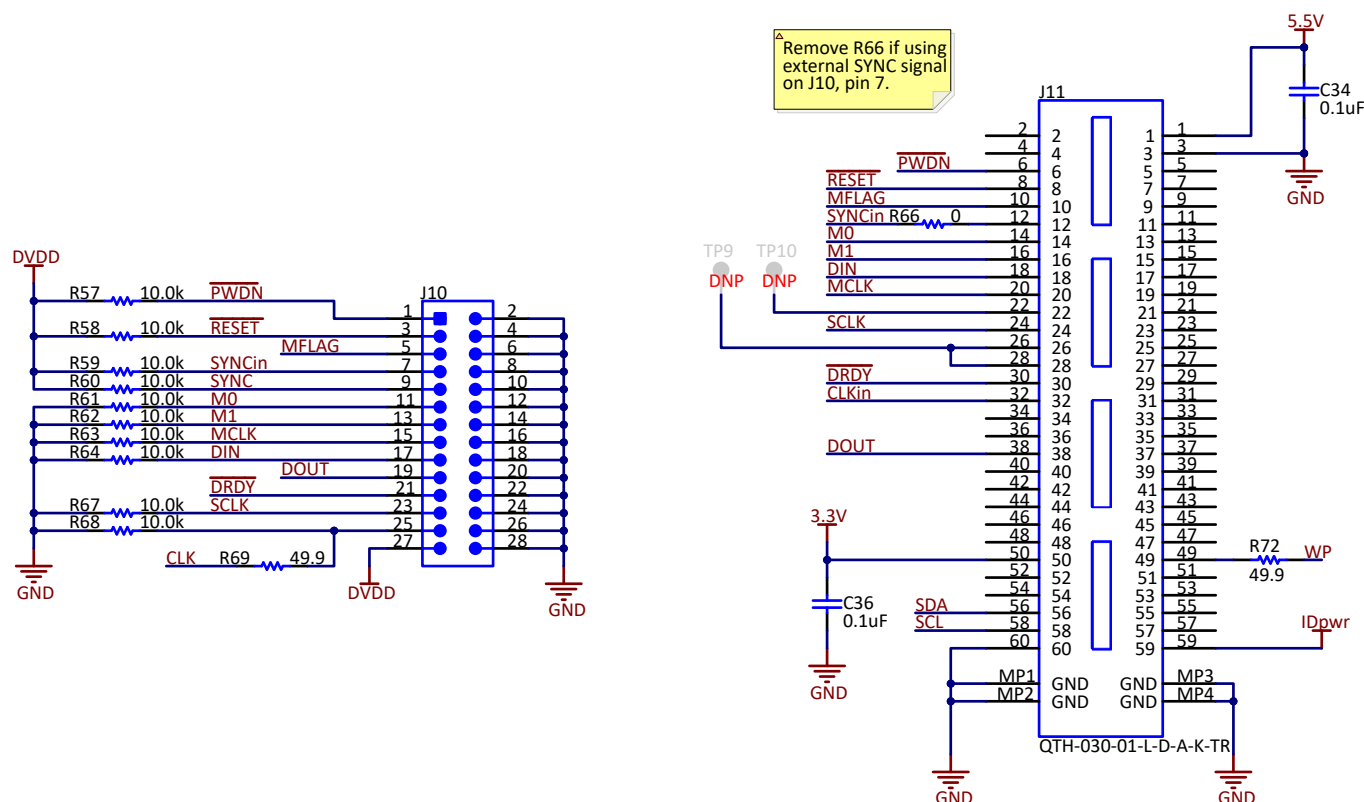


Figure 2-12. Connections to Signals on PHI and Digital Header

2.11 EEPROM

Figure 2-13 shows the EEPROM circuit the PHI uses to identify the EVM at power up. The EEPROM communicates with the PHI over an I2C bus that is not shared with the ADS1282. This circuit is not required by the ADS1282 for operation and is powered down when not used by the PHI.

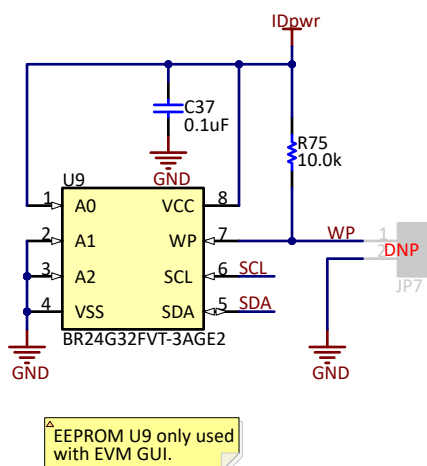


Figure 2-13. EEPROM for EVM ID

2.12 Using the ADS1282EVM With an External Controller

The ADS1282EVM is designed for easy connection to an external controller. This design enables the user to test application code and firmware on the ADS1282 without having to develop a custom PCB. This section describes the specific connections required to use the ADS1282EVM with an external controller. [Figure 2-14](#) shows the location of various headers, connectors and terminal blocks described in this section.

Complete the following steps to prepare the ADS1282 EVM for use with an external controller:

1. Remove the PHI board if still connected to the EVM
2. Verify or move shunt positions:
 - a. JP3, +DVIN position
 - b. JP4, UNIPOLAR or BIPOLAR
 - c. JP5, +AVIN position
 - d. JP6, Oscillator Enable
3. Connect an external bench supply to +AVIN, -VIN (Optional) and +DVIN:
 - a. Connect +6V to +AVIN, terminal block J8
 - b. Connect -3V to -VIN, terminal block J9 (Optional BIPOLAR connection)
 - c. Connect +1.65V to +3.6V to +DVIN, terminal block J7 (Voltage must be equal to the controller voltage)
4. Connect external controller ground to header J10 on one or more GND pins (even pin numbers 2 through 28) and connect power supply grounds to GND pins of terminal blocks J7, J8 and J9.
5. Apply digital communication signals to header J10 on the EVM:
 - a. Connect POCI (peripheral out, controller in) from the controller to DOUT (pin 19)
 - b. Connect PICO (peripheral in, controller out) from the controller to DIN (pin 17)
 - c. Connect SCLK from the controller to SCLK (pin 23)
 - d. Connect an I/O pin from the controller to $\overline{\text{DRDY}}$ (pin 21). $\overline{\text{DRDY}}$ is an output from the ADC that indicates when new data are ready to be clocked out of the ADC. Write a user-defined data collection routine that monitors this pin (polling or interrupt) and only transfer data after a falling edge
 - e. (Optional) Connect I/O pins from the controller to $\overline{\text{PWDN}}$ (pin 1), SYNCin (pin 7) and $\overline{\text{RESET}}$ (pin 3) to power down, control conversions and reset the device, respectively
6. Connect signal source to the input terminal blocks J1 or J3
7. (Optional) Connect one or two RTDs to terminal block J6

Verify that the external power supply voltages, communication signal levels, and applied input signals meet the specifications listed in [Table 1-1](#).

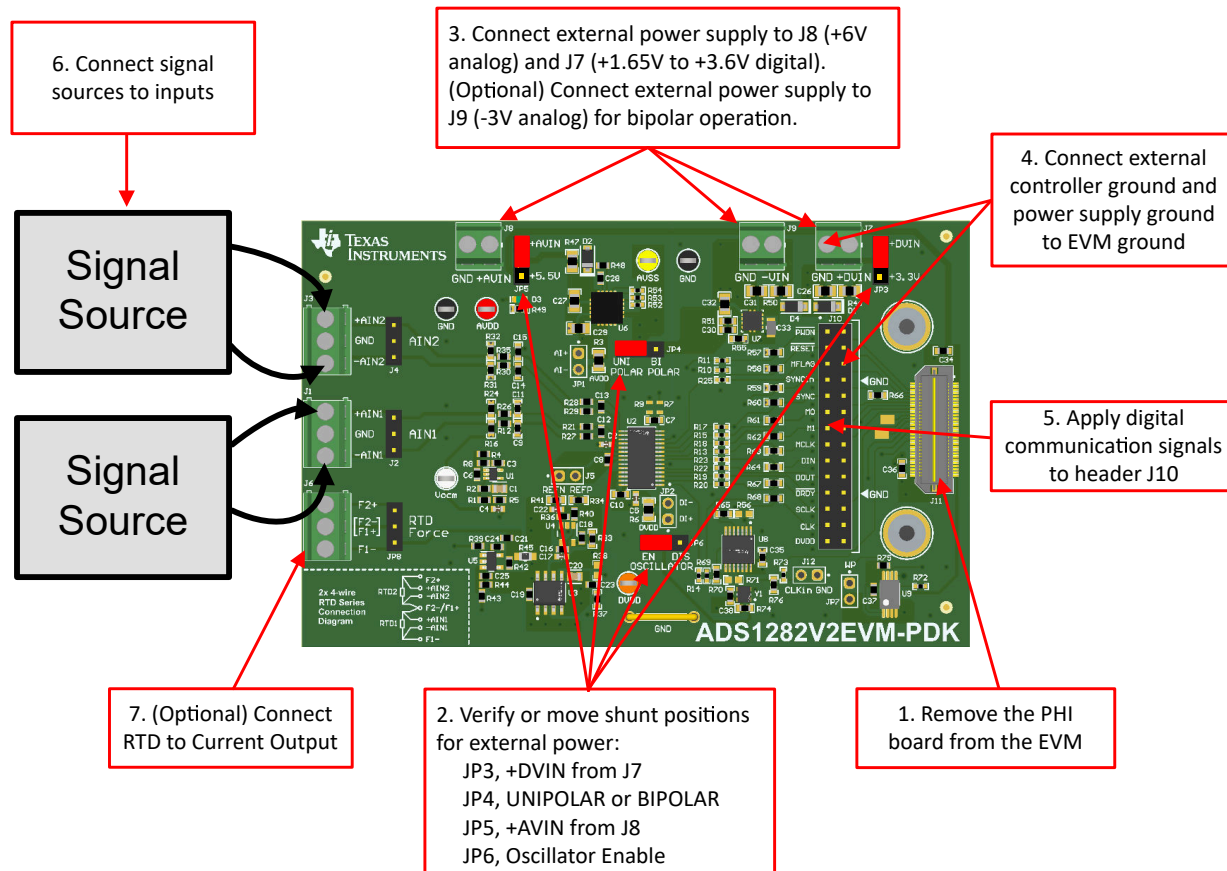


Figure 2-14. External Controller Connections to the ADS1282EVM

3 Software

3.1 Software Description

The ADS1282EVM-PDK-GUI software suite includes graphical tools for data capture, register configuration, time domain analysis, spectral analysis and histogram analysis. This suite also has a provision for exporting data to a text file for post-processing.

3.2 ADS1282 EVM Software Installation

Download the latest version of the EVM graphical user interface (GUI) installer from the [ADS1282EVM Tools and Software](#) folder and run the GUI installer to install the EVM GUI software on your computer.

As shown in [Figure 3-1](#), accept the license agreement and follow the on-screen instructions to complete the installation. If the LabVIEW™ run-time engine has not already been installed, then a prompt to accept this license agreement appears.

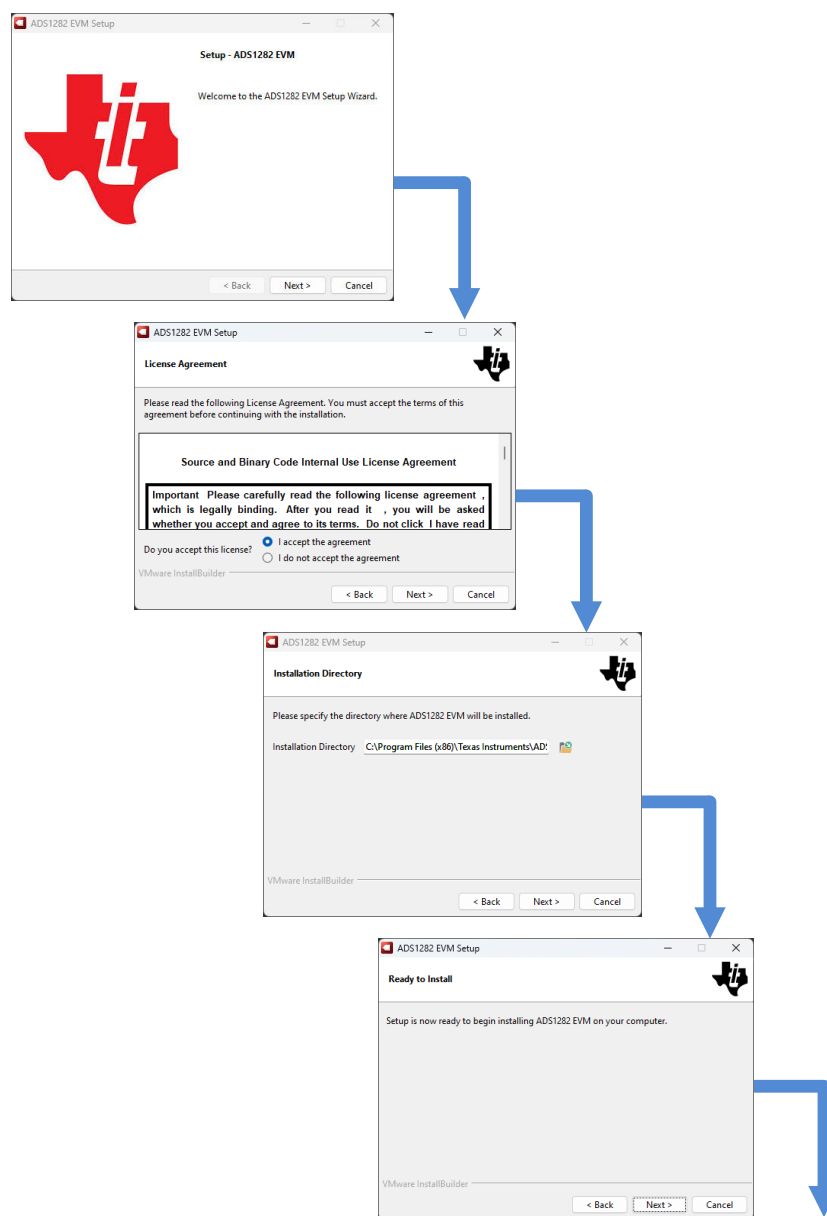


Figure 3-1. Software Installation and Prompts (1)

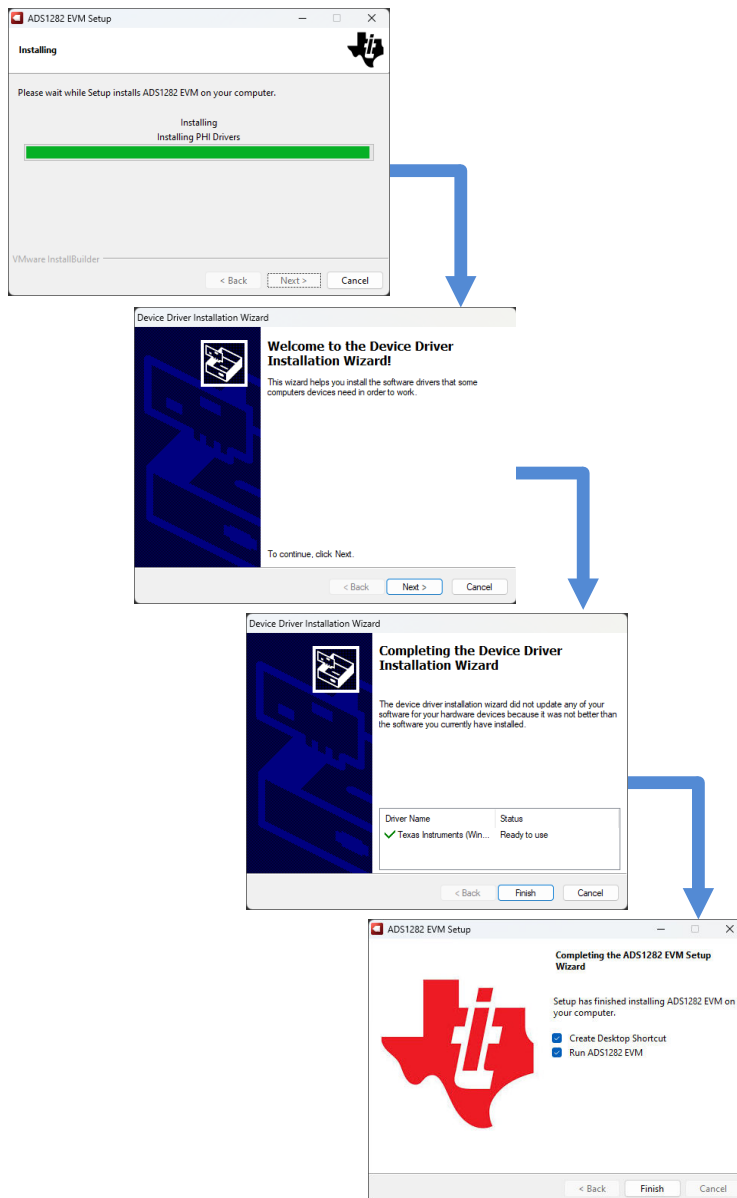


Figure 3-2. Software Installation and Prompts (2)

4 Implementation Results

4.1 EVM Operation

4.1.1 Evaluation Setup

Connect the EVM as shown in [Figure 4-1](#) after installing the software:

1. Physically connect connector P2 of the PHI to connector J11 of the ADS1282EVM. Install the included screws to provide a robust connection.
2. Connect the USB connector on the PHI to the computer.
 - a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
 - b. LED D1 and LED D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; [Figure 4-1](#) shows the resulting LED indicators.
3. Start the software GUI as shown in [Figure 4-2](#). Notice that the LEDs blink slowly when the FPGA firmware is loaded on the PHI. This loading takes a few seconds. LED D3 on the ADS1282EVM illuminates once a connection has been established.
4. Verify the default shunt positions of the ADS1282 EVM. Shunt JP3 is placed in the +3.3V position, shunt JP4 is placed in the UNIPOLAR position, shunt JP5 is placed in the +5.5V position, and shunt JP6 is placed in the OSCILLATOR ENABLE position.
5. Connect the differential signal generator to the ADS1282EVM inputs. The differential full-scale input range is $\pm 2.5V$ and the recommended common mode voltage is 2.5V. A typical input signal is a $4.8V_{PP}$ sinusoidal wave centered at 2.5V. Adjust the input signal just below the $5V_{PP}$ full-scale range to avoid clipping.

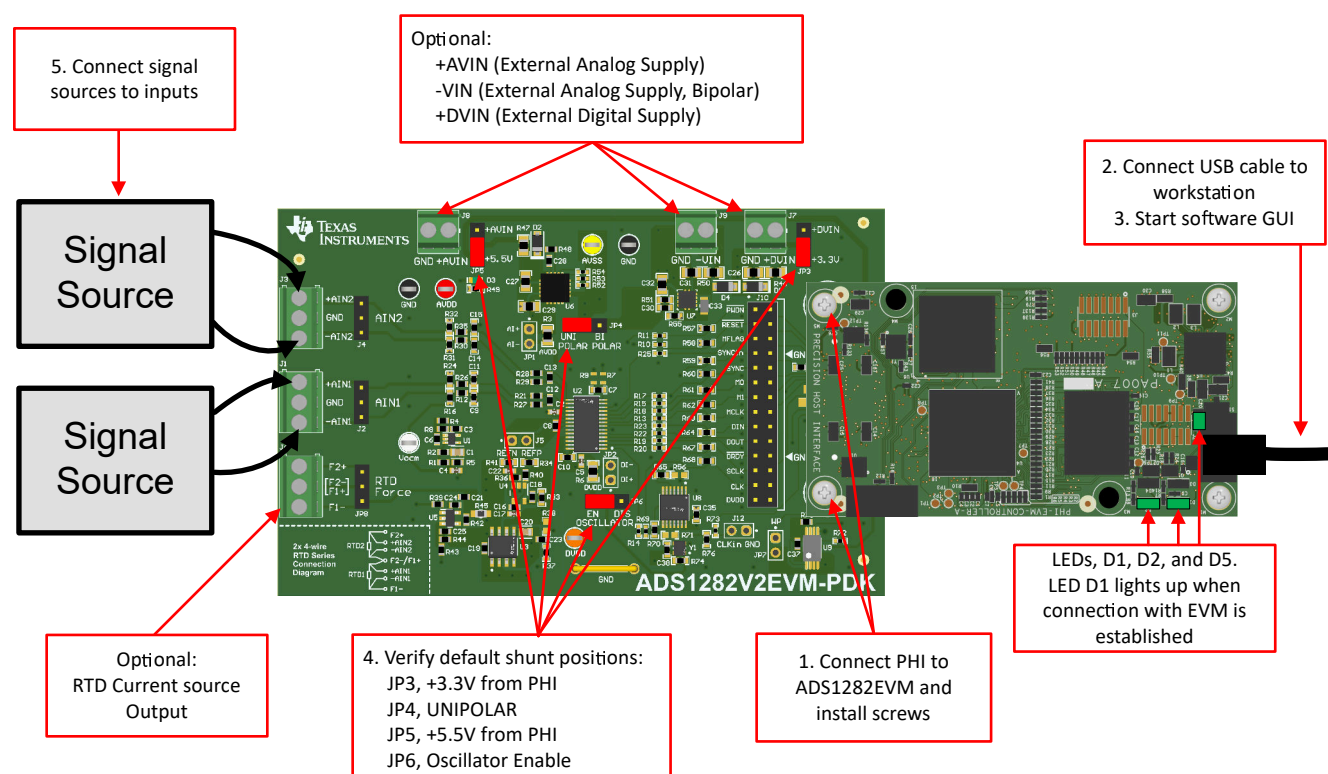


Figure 4-1. Connecting the Hardware to the ADS1282EVM

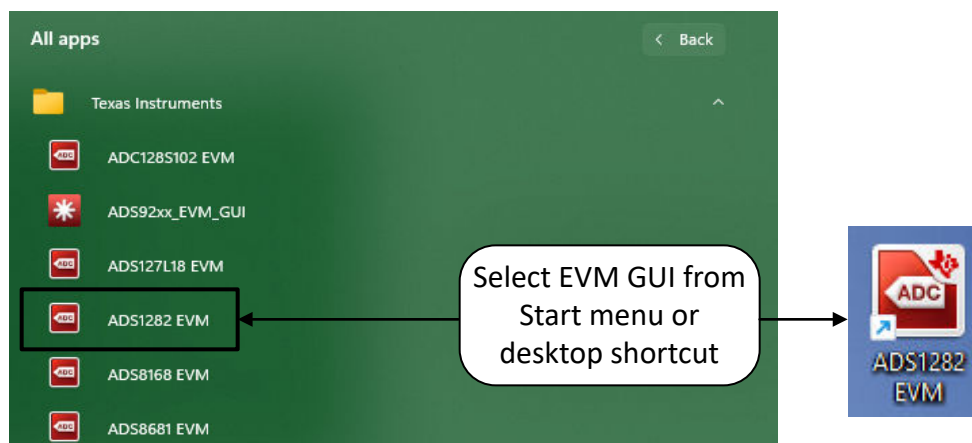


Figure 4-2. Launch the ADS1282EVM GUI Software

4.1.2 EVM Register Settings

Figure 4-3 shows the ADC register settings. Modify the registers to enable different device modes (such as filter settings and synchronization settings). Access this page by selecting *Register Map Config* under *Pages* on the left side of the GUI.

Register Map Configuration

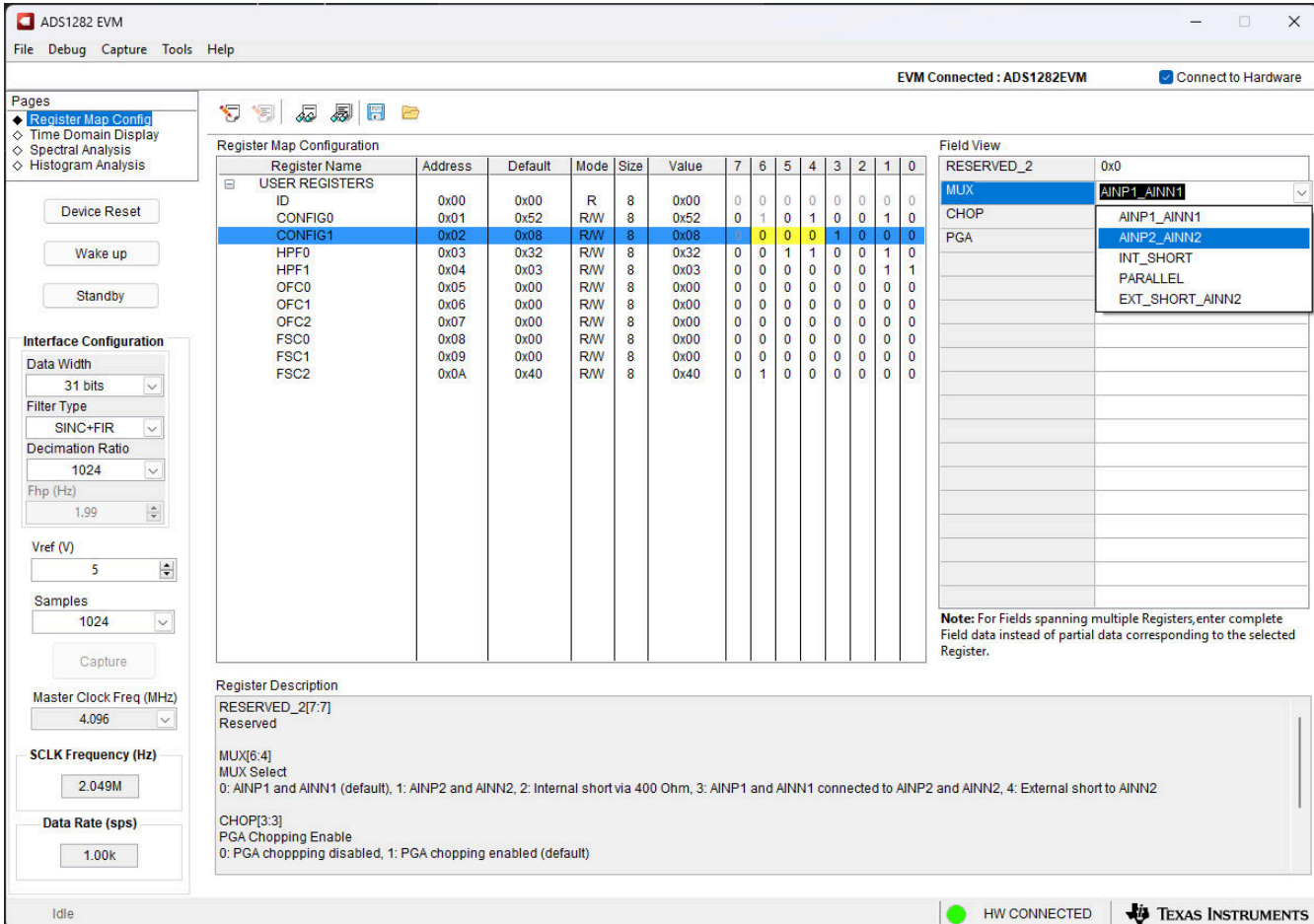
Register Name	Address	Default	Mode	Size	Value	7	6	5	4	3	2	1	0
USER REGISTERS													
ID	0x00	0x00	R	8	0x00	0	0	0	0	0	0	0	0
CONFIG0	0x01	0x52	R/W	8	0x52	0	1	0	1	0	0	1	0
CONFIG1	0x02	0x08	R/W	8	0x08	0	0	0	0	1	0	0	0
HPF0	0x03	0x32	R/W	8	0x32	0	0	1	1	0	0	1	0
HPF1	0x04	0x03	R/W	8	0x03	0	0	0	0	0	0	1	1
OFC0	0x05	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC1	0x06	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC2	0x07	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC0	0x08	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC1	0x09	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC2	0x0A	0x40	R/W	8	0x40	0	1	0	0	0	0	0	0

Note: For Fields spanning multiple Registers, enter complete Field data instead of partial data corresponding to the selected Register.

Figure 4-3. EVM Register Configuration

4.1.2.1 Channel Configuration

Figure 4-4 shows how the MUX field of the CONFIG1 register can be used to switch between channels 1 and 2. Options available for this field are AINP1_AINN1, AINP2_AINN2, INT_SHORT, PARALLEL, and EXT_SHORT_AINN2. The *Register Description* section at the bottom of the *Register Map Config* page describes each option.



The screenshot displays the ADS1282 EVM Register Map Configuration tool. The interface includes a menu bar (File, Debug, Capture, Tools, Help), a status bar (EVM Connected: ADS1282EVM, Connect to Hardware), and a sidebar with navigation options (Register Map Config, Time Domain Display, Spectral Analysis, Histogram Analysis). The main window is divided into several sections:

- Device Control:** Buttons for Device Reset, Wake up, and Standby.
- Interface Configuration:** Settings for Data Width (31 bits), Filter Type (SINC+FIR), Decimation Ratio (1024), Fhp (Hz) (1.99), Vref (V) (5), Samples (1024), Master Clock Freq (MHz) (4.096), SCLK Frequency (Hz) (2.049M), and Data Rate (sps) (1.00k).
- Register Map Configuration:** A table listing registers and their bit fields. The CONFIG1 register is highlighted, showing its address (0x02), default value (0x08), mode (R/W), size (8), and value (0x08). The bit fields are: 7 (0), 6 (0), 5 (0), 4 (0), 3 (1), 2 (0), 1 (0), 0 (0).
- Field View:** A dropdown menu for the MUX field, showing options: AINP1_AINN1, AINP2_AINN2, INT_SHORT, PARALLEL, and EXT_SHORT_AINN2. AINP2_AINN2 is selected.
- Register Description:** A section providing detailed information about the registers. It includes:
 - RESERVED_2[7:7]:** Reserved.
 - MUX[6:4]:** MUX Select. 0: AINP1 and AINN1 (default), 1: AINP2 and AINN2, 2: Internal short via 400 Ohm, 3: AINP1 and AINN1 connected to AINP2 and AINN2, 4: External short to AINN2.
 - CHOP[3:3]:** PGA Chopping Enable. 0: PGA chopping disabled, 1: PGA chopping enabled (default).

The status bar at the bottom indicates "Idle" and "HW CONNECTED" with the Texas Instruments logo.

Figure 4-4. Channel Selection

4.1.2.2 PGA Gain Selection

Figure 4-5 shows how the ADS1282 internal PGA gain can be configured by the PGA field of the CONFIG1 register. Gain options available are 1, 2, 4, 8, 16, 32 and 64. Use this setting to optimize the dynamic range of the ADC to small input signals.

The screenshot shows the ADS1282 EVM software interface. The 'Register Map Configuration' window is open, displaying a table of registers. The 'CONFIG1' register is selected, and the 'PGA' field is being configured to 'GAIN_1'.

Register Name	Address	Default	Mode	Size	Value	7	6	5	4	3	2	1	0
USER REGISTERS													
ID	0x00	0x00	R	8	0x00	0	0	0	0	0	0	0	0
CONFIG0	0x01	0x52	R/W	8	0x52	0	1	0	1	0	0	1	0
CONFIG1	0x02	0x08	R/W	8	0x08	0	0	0	0	1	0	0	0
HPF0	0x03	0x32	R/W	8	0x32	0	0	1	1	0	0	1	0
HPF1	0x04	0x03	R/W	8	0x03	0	0	0	0	0	0	1	1
OFC0	0x05	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC1	0x06	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC2	0x07	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC0	0x08	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC1	0x09	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC2	0x0A	0x40	R/W	8	0x40	0	1	0	0	0	0	0	0

The 'Field View' section shows the 'PGA' field selected, with a dropdown menu displaying gain options: GAIN_1, GAIN_2, GAIN_4, GAIN_8, GAIN_16, GAIN_32, and GAIN_64. GAIN_1 is currently selected.

Note: For Fields spanning multiple Registers, enter complete Field data instead of partial data corresponding to the selected Register.

The 'Register Description' section shows the following details:

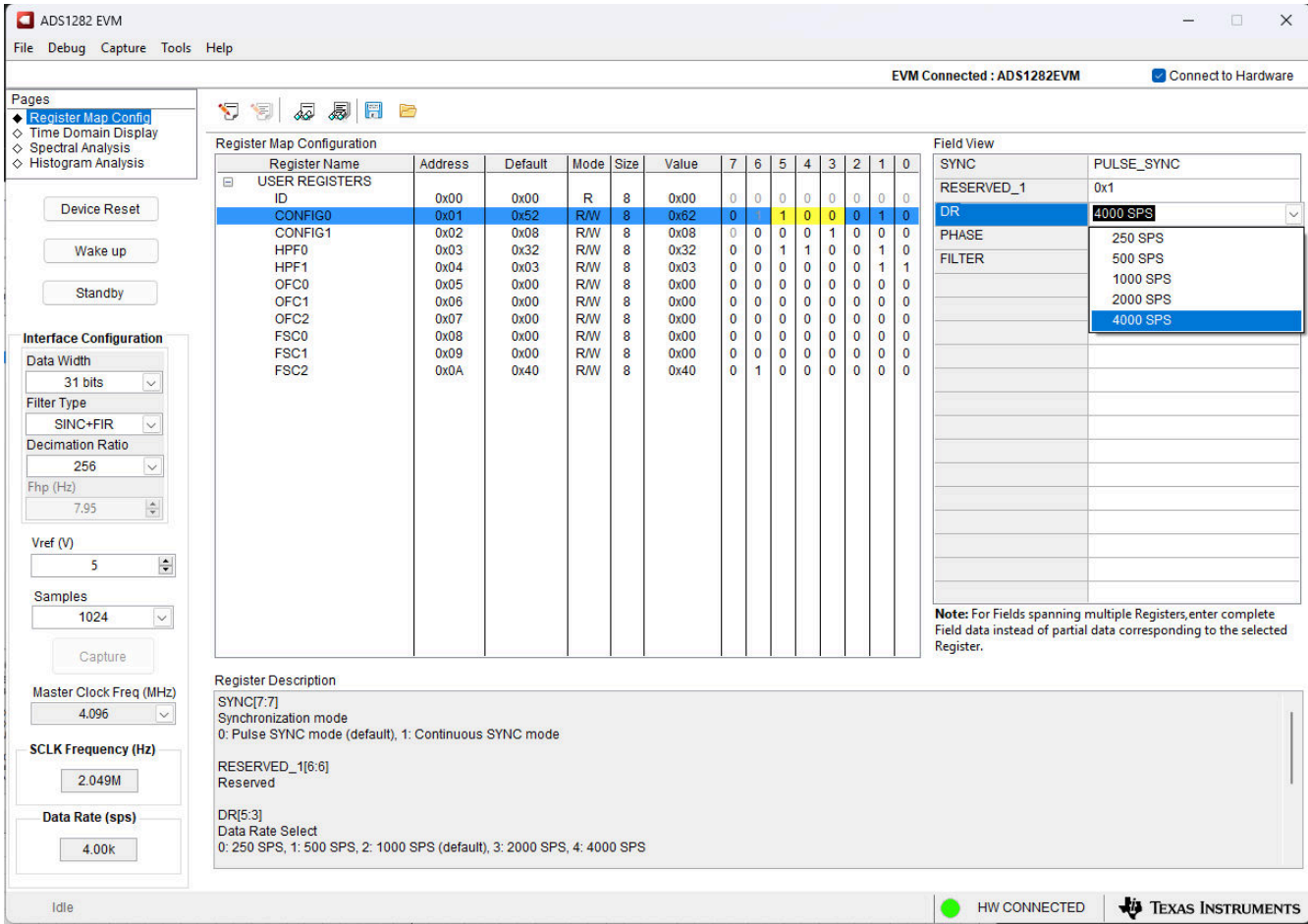
- RESERVED_2[7:7] Reserved
- MUX[6:4] MUX Select
0: AINP1 and AINN1 (default), 1: AINP2 and AINN2, 2: Internal short via 400 Ohm, 3: AINP1 and AINN1 connected to AINP2 and AINN2, 4: External short to AINN2
- CHOP[3:3] PGA Chopping Enable
0: PGA chopping disabled, 1: PGA chopping enabled (default)

Figure 4-5. PGA Gain Selection

4.1.2.3 Data Rate Configuration

Figure 4-6 shows how to select the data output rate of the ADS1282. These data rates are only correct when using the default SINC+FIR filter option with an ADC clock frequency (f_{clk}) of 4.096MHz. Refer to the [ADS1282 datasheet](#) for more information when using a different filter type or clock frequency.

The ADS1282 supports data output speeds of up to 4000 samples per second (SPS). Other options available are 250SPS, 500SPS, 1000SPS and 2000SPS.



The screenshot displays the ADS1282 EVM software interface. On the left, the 'Pages' menu includes 'Register Map Configuration', 'Time Domain Display', 'Spectral Analysis', and 'Histogram Analysis'. Below this, there are buttons for 'Device Reset', 'Wake up', and 'Standby'. The 'Interface Configuration' section on the left includes settings for 'Data Width' (31 bits), 'Filter Type' (SINC+FIR), 'Decimation Ratio' (256), 'Fhp (Hz)' (7.95), 'Vref (V)' (5), 'Samples' (1024), 'Master Clock Freq (MHz)' (4.096), 'SCLK Frequency (Hz)' (2.049M), and 'Data Rate (sps)' (4.00k). The 'Register Map Configuration' table shows the following registers:

Register Name	Address	Default	Mode	Size	Value	7	6	5	4	3	2	1	0
USER REGISTERS													
ID	0x00	0x00	R	8	0x00	0	0	0	0	0	0	0	0
CONFIG0	0x01	0x52	R/W	8	0x52	0	1	0	0	0	1	0	0
CONFIG1	0x02	0x08	R/W	8	0x08	0	0	0	0	1	0	0	0
HPF0	0x03	0x32	R/W	8	0x32	0	0	1	1	0	0	1	0
HPF1	0x04	0x03	R/W	8	0x03	0	0	0	0	0	0	1	1
OFC0	0x05	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC1	0x06	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
OFC2	0x07	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC0	0x08	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC1	0x09	0x00	R/W	8	0x00	0	0	0	0	0	0	0	0
FSC2	0x0A	0x40	R/W	8	0x40	0	1	0	0	0	0	0	0

The 'Field View' section on the right shows the 'DR' register selected, with a dropdown menu for 'Data Rate' showing options: 250 SPS, 500 SPS, 1000 SPS, 2000 SPS, and 4000 SPS. The '4000 SPS' option is selected. A note at the bottom right states: 'Note: For Fields spanning multiple Registers, enter complete Field data instead of partial data corresponding to the selected Register.'

The 'Register Description' section at the bottom provides details for the selected register: SYNC[7:7] Synchronization mode (0: Pulse SYNC mode (default), 1: Continuous SYNC mode), RESERVED_1[6:6] Reserved, and DR[5:3] Data Rate Select (0: 250 SPS, 1: 500 SPS, 2: 1000 SPS (default), 3: 2000 SPS, 4: 4000 SPS).

Figure 4-6. Data Rate Configuration

4.1.3 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. Use this tool to study the behavior and debug any gross problems with the ADC or drive circuits. Access this page by selecting *Time Domain Display* under *Pages* on the left side of the GUI.

Trigger a capture of the data of the selected number of samples from the ADS1282 EVM, as per the current interface mode settings indicated in [Figure 4-7](#) by using the *Capture* button. The sample indices on the x-axis and the y-axis show the corresponding equivalent analog codes or voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

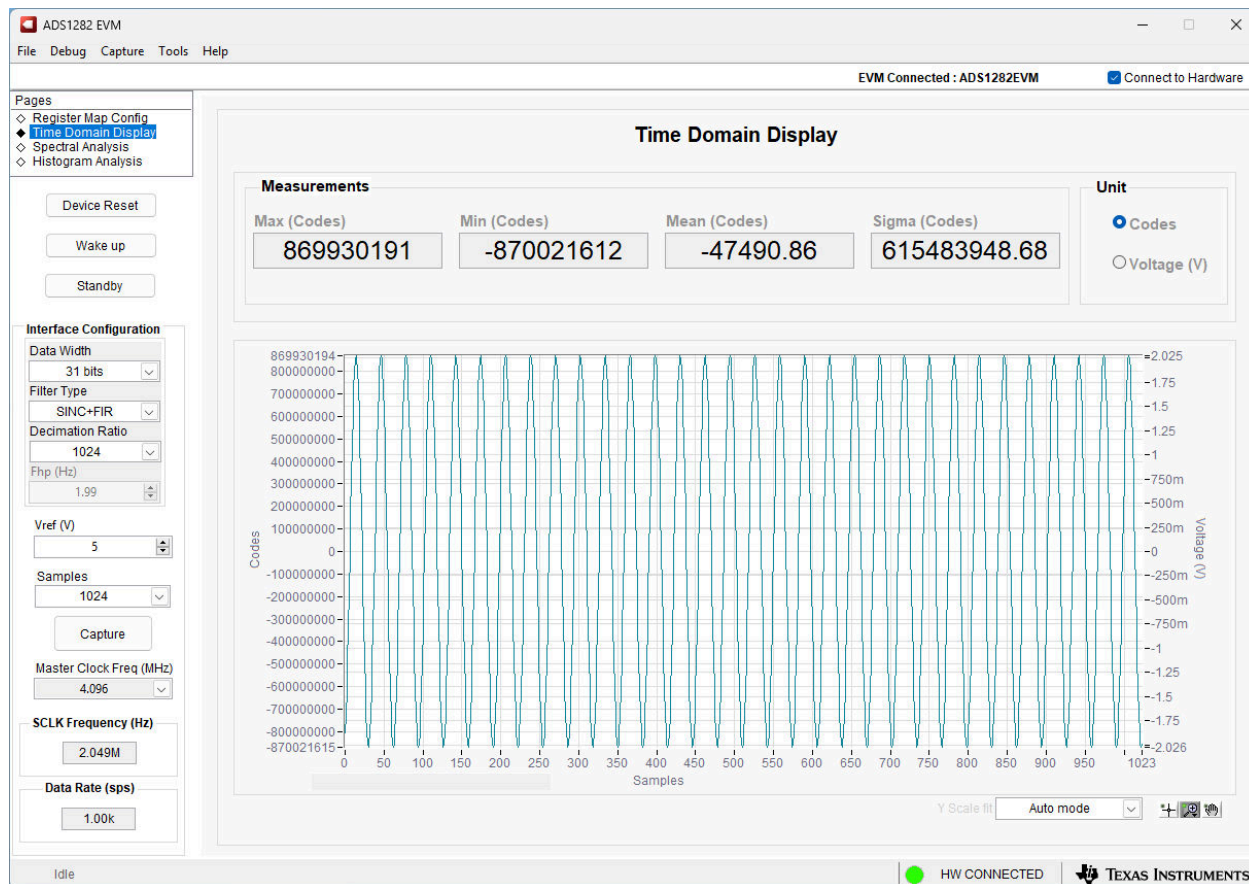


Figure 4-7. Time Domain Display

4.1.4 Spectral Analysis Display

The spectral analysis tool, shown in [Figure 4-8](#), is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS1282 through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. Access this page by selecting *Spectral Analysis* under *Pages* on the left side of the GUI.

The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The option to use no window is not recommended in evaluating the performance of the ADS1282.

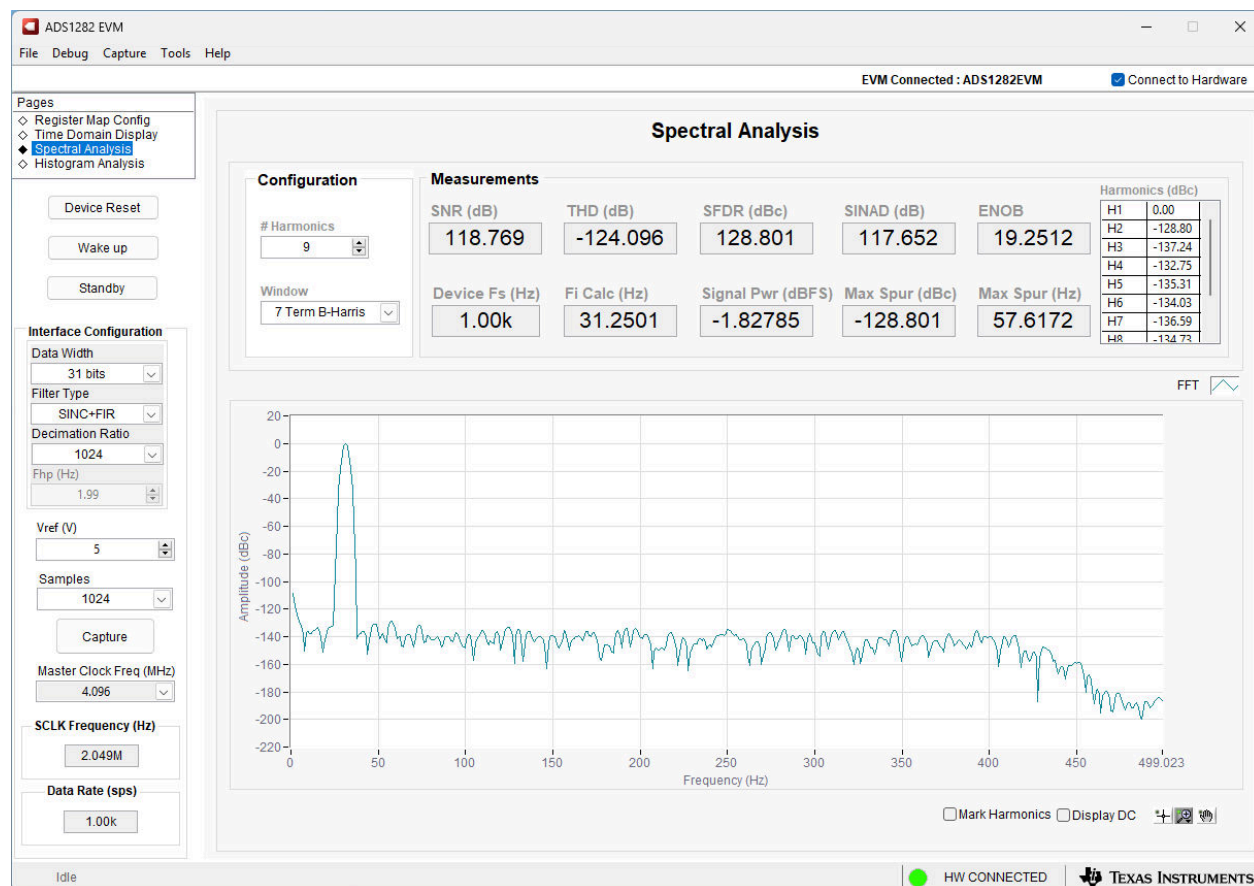


Figure 4-8. Frequency Domain Display

4.1.5 Histogram Analysis Display

The histogram analysis tool, shown in [Figure 4-9](#), calculates the maximum, minimum, peak-to-peak, mean and sigma (standard deviation) on a DC input data set. Access this page by selecting the *Histogram Analysis* under *Pages* on the left side of the GUI.

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution. The cumulative effect of noise coupled to the ADC output comes from sources such as the input drive circuit, reference drive circuit, ADC power supply and the ADC. Cumulative noise is reflected in the standard deviation of the ADC output code histogram obtained by performing multiple conversions of a DC input applied to a given channel. [Figure 4-9](#) shows the histogram corresponding to a DC input displayed by clicking the *Capture* button.

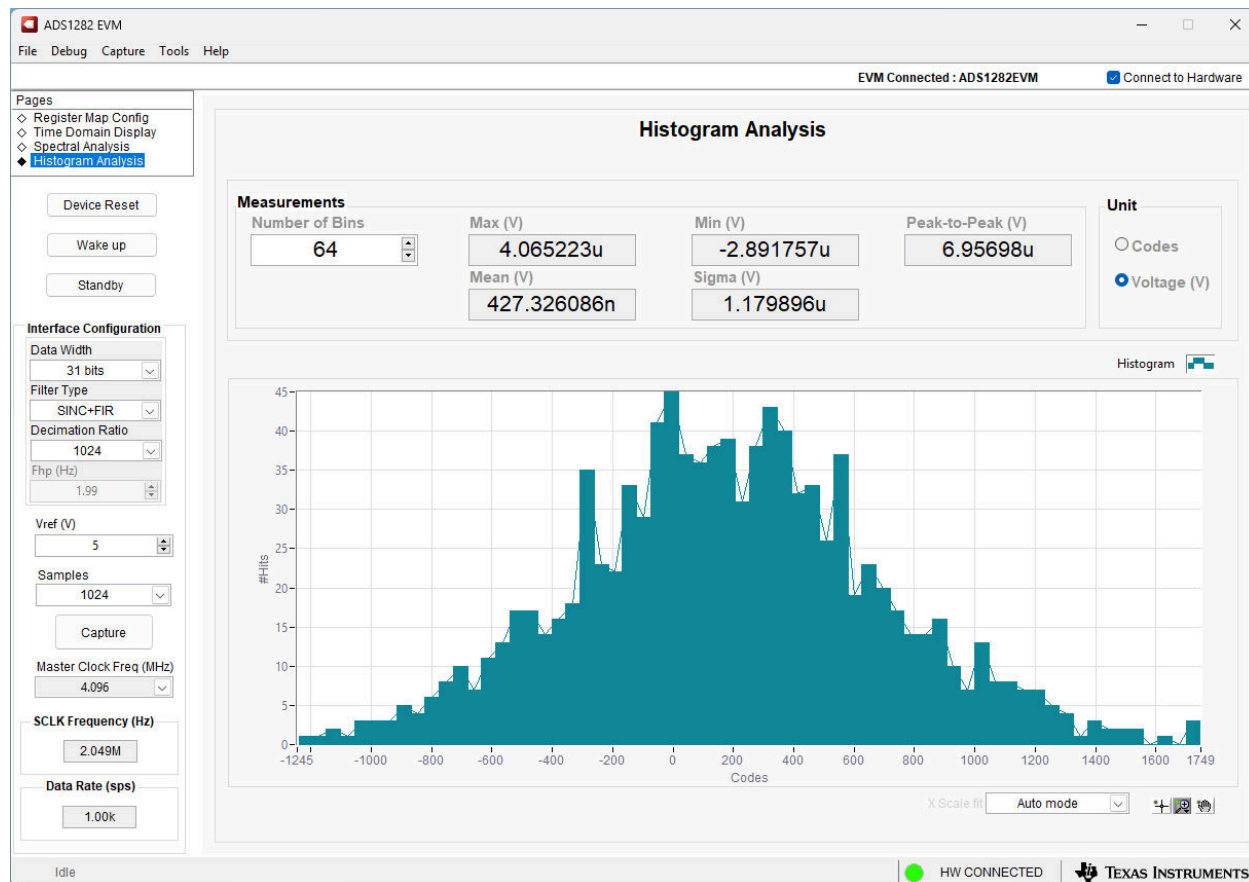


Figure 4-9. Histogram Display

4.1.6 GUI Data Export

Data can be exported from the Time Domain Display, Spectral Analysis and Histogram Analysis pages by right-clicking in the data display window and selecting *Export -> Export Data To Clipboard* or *Export -> Export Data To Excel*. Refer to [Figure 4-10](#) for a Time Domain data export example.

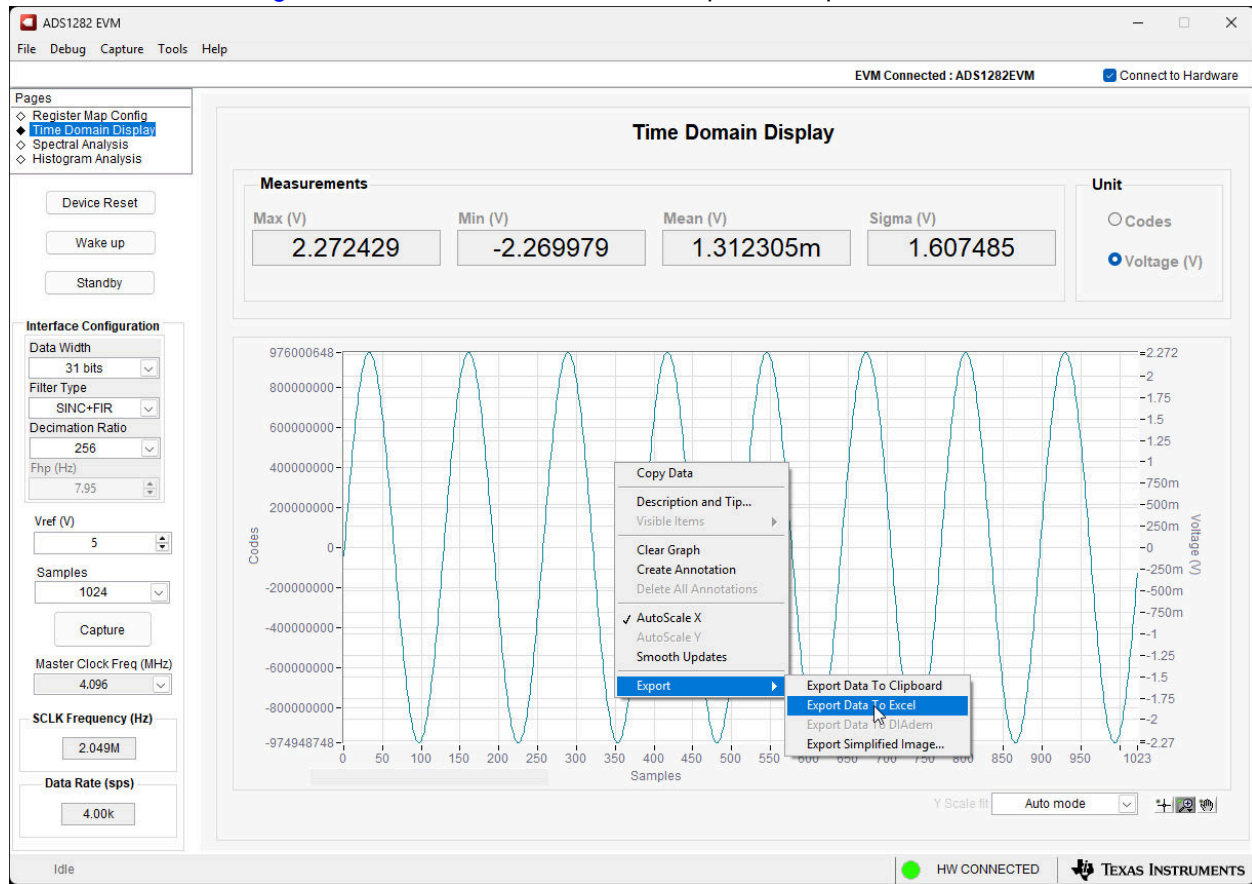


Figure 4-10. ADS1282 EVM GUI Data Export

[Figure 4-11](#) shows an export data example from the Time Domain Display to Microsoft Excel®. The data is exported as ADC codes but can be converted to voltage using [Equation 1](#).

$$V_{\text{adc}} = \frac{V_{\text{ref}}}{\text{PGA}} \times \frac{\text{CODE}}{2^{31}} \quad (1)$$

- V_{ref} is set to 5V on the EVM
- PGA is the gain value and can be set to values of 1 (default), 2, 4, 8, 16, 32 and 64
- CODE is the signed output integer exported to the clipboard or Excel

	A	B	C
1	Samples - Analog Channel 0	Codes - Analog Channel 0	
2	0	-38502698	
3	1	9322787	
4	2	57134571	
5	3	104804130	
6	4	152227117	
7	5	199285058	

Figure 4-11. ADS1282 EVM GUI Data Export to Excel

5 Hardware Design Files

This section contains the ADS1282 EVM schematics, PCB layout, and bill of materials (BOM).

5.1 Schematics

Figure 5-1 to Figure 5-4 show the complete ADS1282EVM schematic.

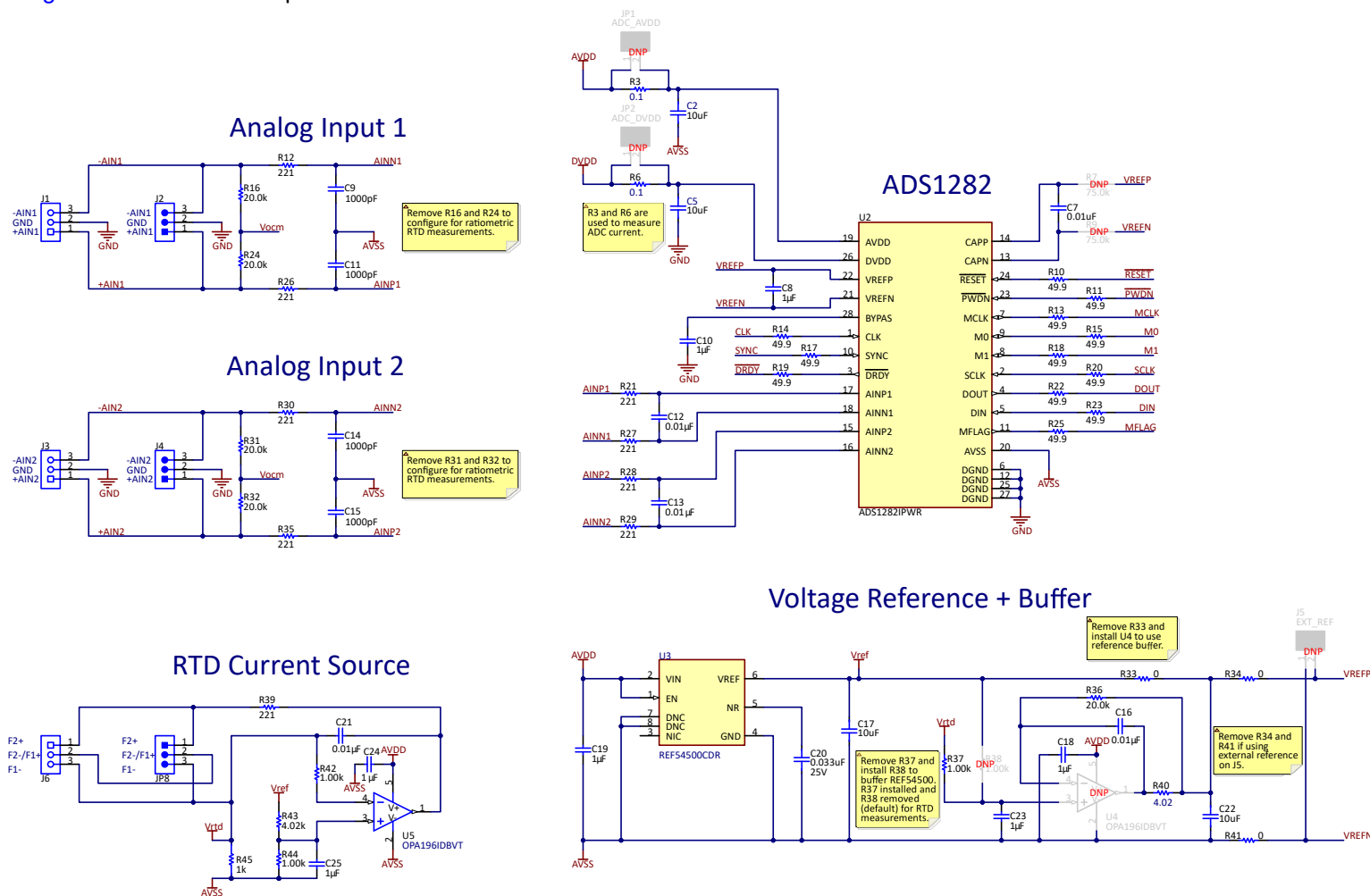
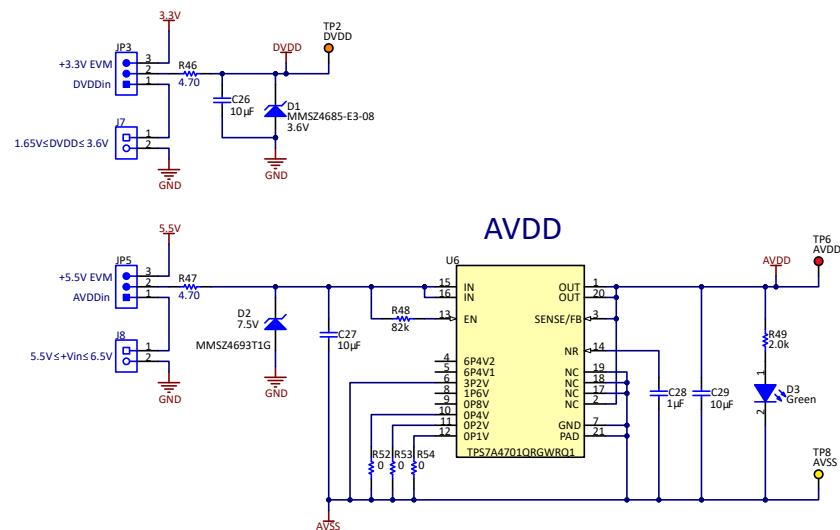
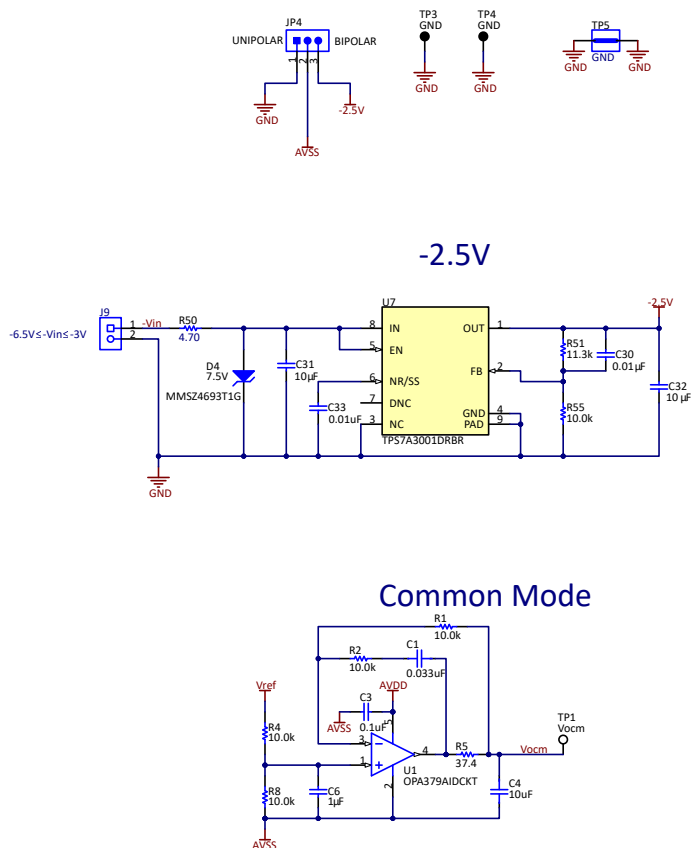


Figure 5-1. ADS1282EVM Analog Inputs and Reference Schematic

AVSS Select and Testpoints



Programmable LDO Configurations			
Vout (V)	QP4V	QP2V	QP1V
4.8	-	R53 INSTALLED	-
4.9	-	R53 INSTALLED	R54 INSTALLED
5.0	R52 INSTALLED	-	-
5.1	R52 INSTALLED	-	R54 INSTALLED
5.2	R52 INSTALLED	R53 INSTALLED	-
5.3	R52 INSTALLED	R53 INSTALLED	R54 INSTALLED

INSTALLED = Solder 0-Ohm jumper to GND/AVSS
 VOUT = 1.4V + $\sum$ (all grounded pins)

Figure 5-2. ADS1282EVM Power Schematic

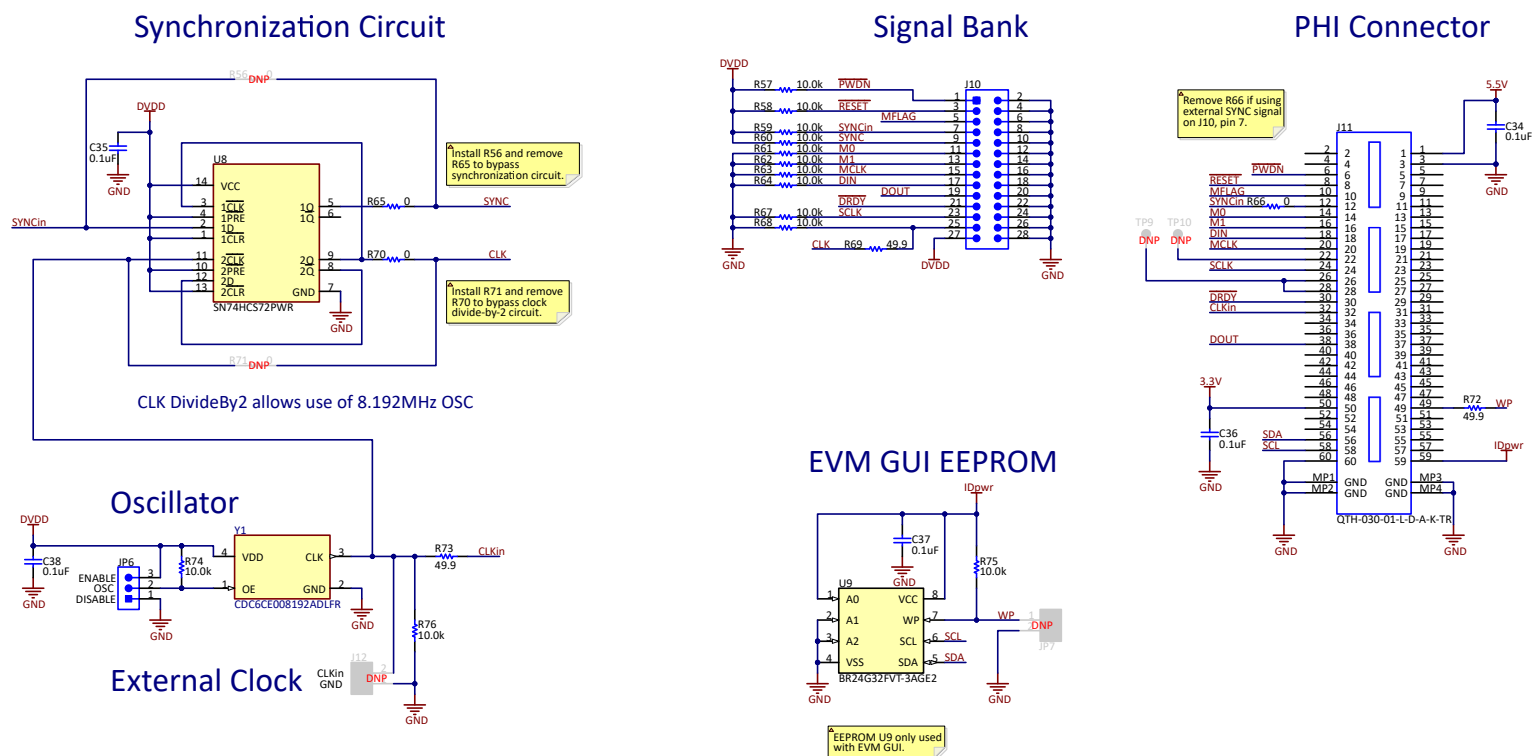


Figure 5-3. ADS1282EVM Digital Interface and Clocking Schematic

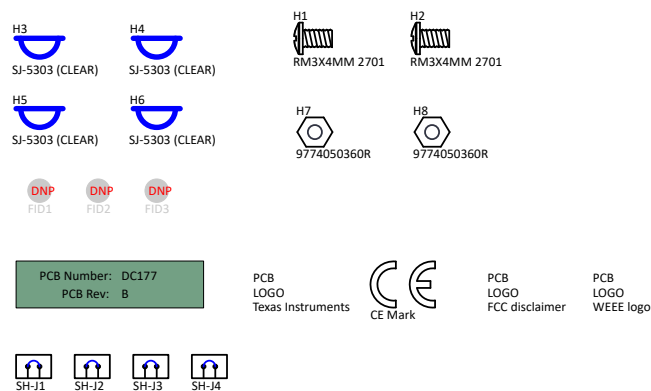


Figure 5-4. ADS1282EVM Hardware

5.2 PCB Layouts

Figure 5-5 to Figure 5-10 show the layout drawings for all ADS1282EVM PCB layers.

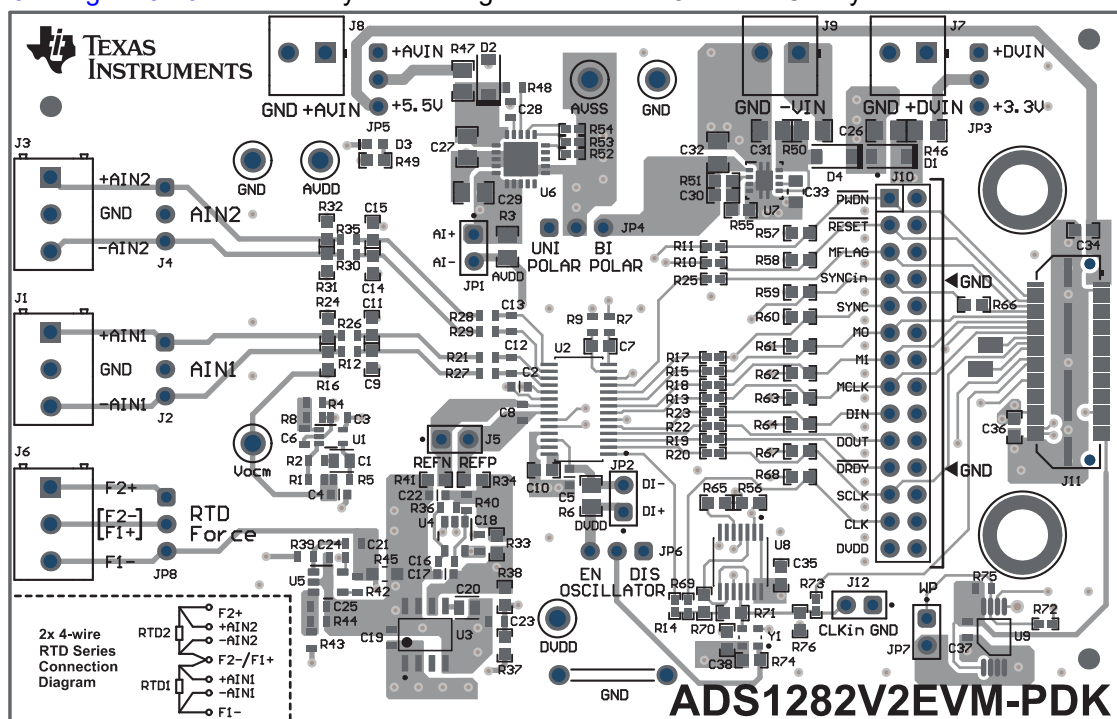


Figure 5-5. PCB Layout for the ADS1282EVM (Top Composite - Top View)

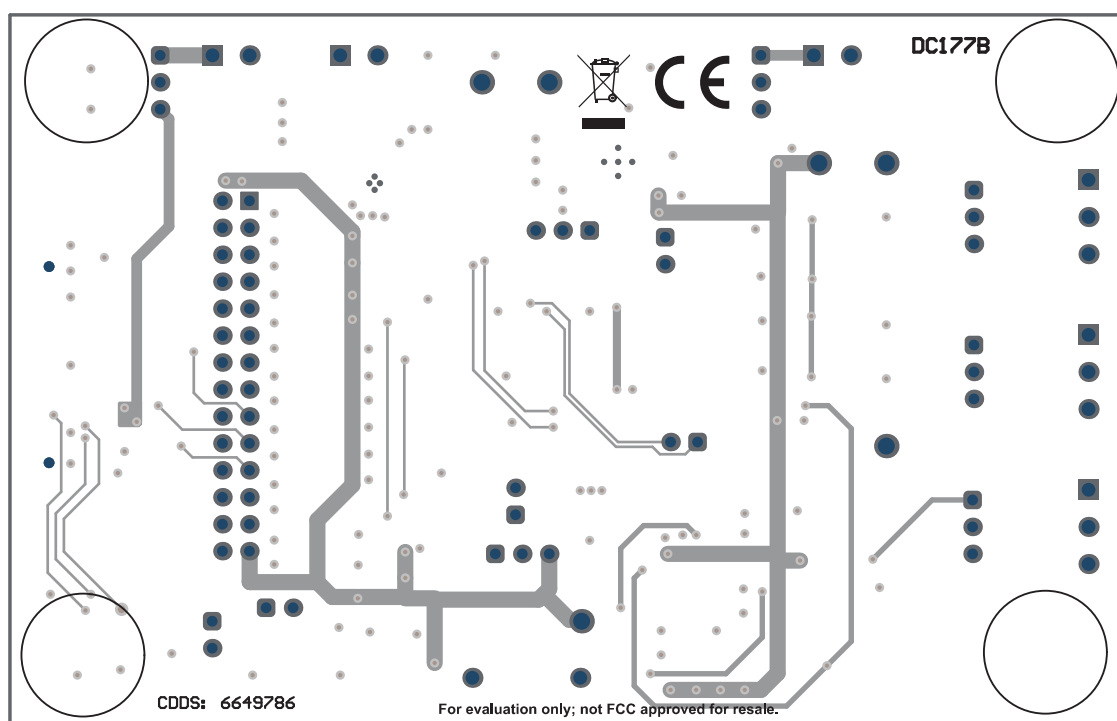


Figure 5-6. PCB Layout for the ADS1282EVM (Bottom Composite - Bottom View)

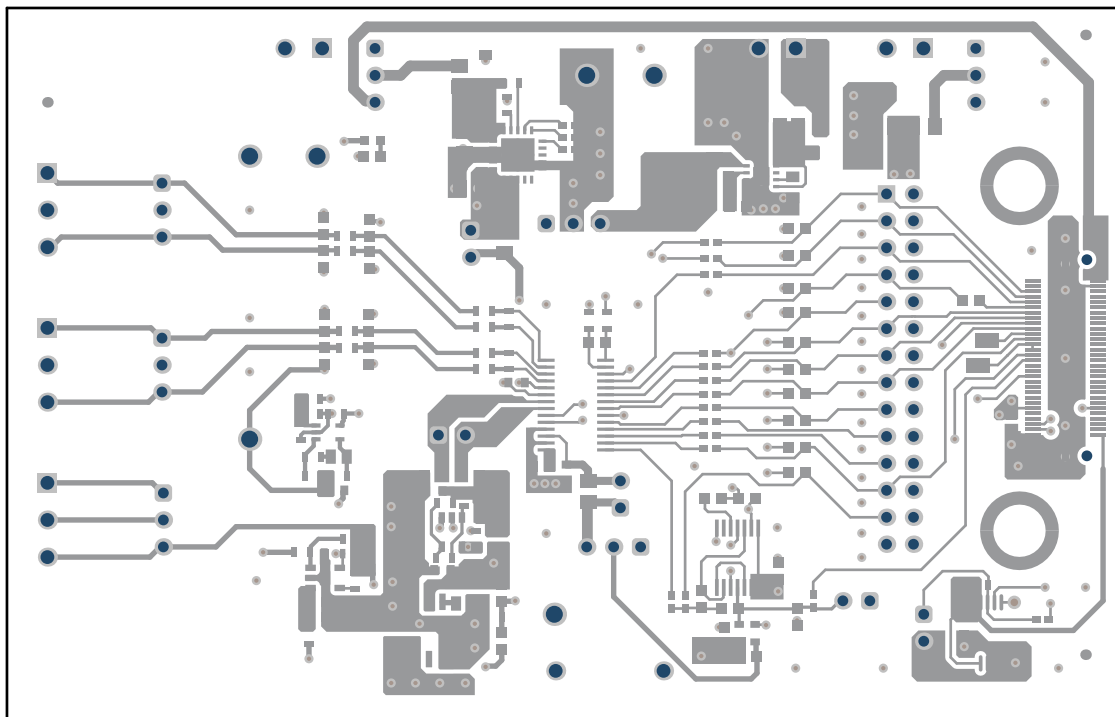


Figure 5-7. PCB Layout for the ADS1282EVM (Top Layer - Top View)

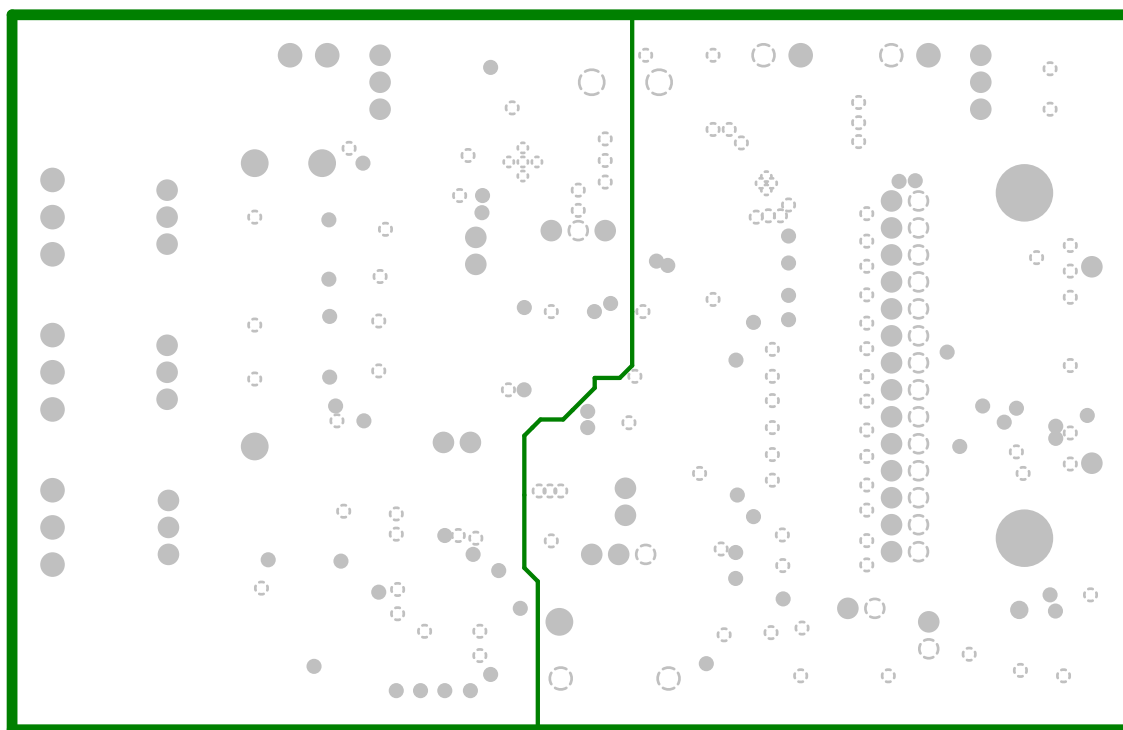


Figure 5-8. PCB Layout for the ADS1282EVM (Internal GND AVSS Plane 1 - Top View)

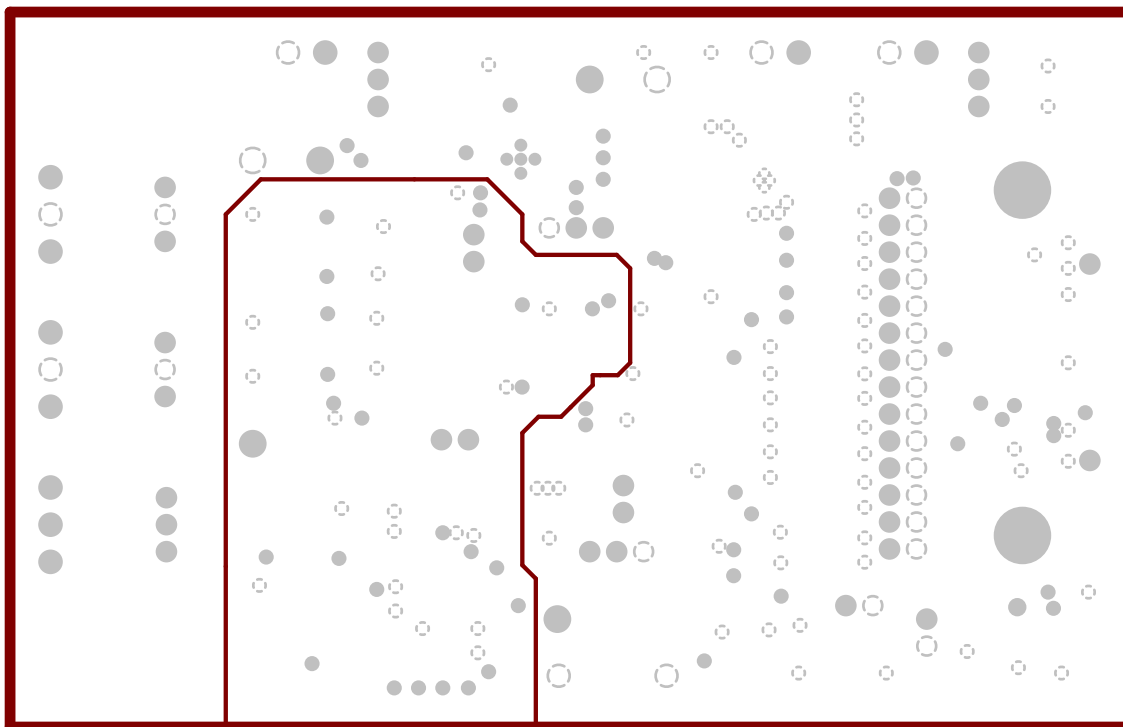


Figure 5-9. PCB Layout for the ADS1282EVM (Internal GND AVSS Plane 2 - Top View)

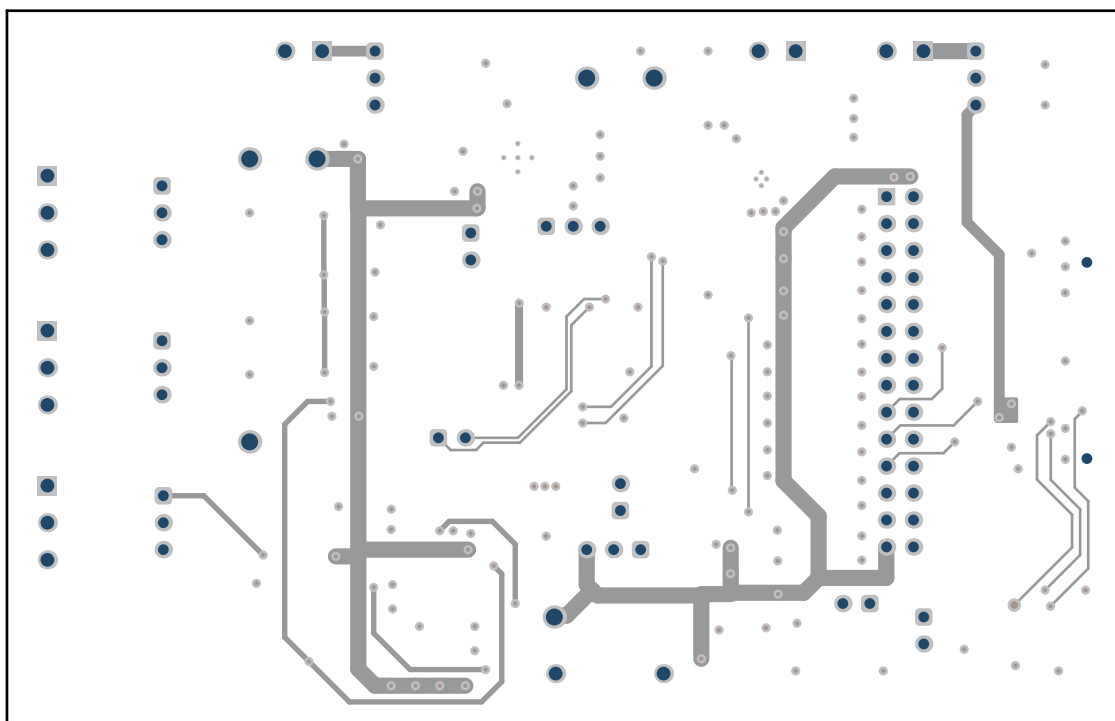


Figure 5-10. PCB Layout for the ADS1282EVM (Bottom Layer - Top View)

5.3 Bill of Materials (BOM)

Table 5-1 lists the ADS1282EVM bill of materials.

Table 5-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC177	Any
C1, C20	2	33nF	0.033 μ F $\pm$ 1% 25V Ceramic Capacitor C0G, NP0 0805 (2012 Metric)	0805	C0805C333F3GEC7210	KEMET
C2, C4, C5, C17, C22	5	10 μ F	10 μ F $\pm$ 20% 25V Ceramic Capacitor X5R 0603 (1608 Metric)	0603	ZRB18AR61E106ME01L	Murata Electronics
C3, C34, C35, C36, C37, C38	6	0.1 μ F	CAP, CERM, 0.1 μ F, 25 V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C6, C8, C18, C19, C23, C24, C25, C28	8	1 μ F	CAP, CERM, 1 μ F, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C7	1	0.01 μ F	CAP, CERM, 0.01 μ F, 25 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	0603	C0603C103J3GECAUTO	Kemet
C9, C11, C14, C15	4	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C102J5GACTU	Kemet
C10	1		CAP, 1 μ F, 25V, $\pm$ 10%, X7R, 0603	0603	CL10B105KA8NNNC	Samsung
C12, C13, C16, C21, C30	5	0.01 μ F	CAP, CERM, 0.01 μ F, 25 V, +/- 1%, C0G/NP0, 0603	0603	C0603C103F3GACTU	Kemet
C26, C27, C29, C31, C32	5	10 μ F	CAP, CERM, 10 μ F, 25 V, +/- 10%, X5R, 0805	0805	CC0805KKX5R8BB106	Yageo
C33	1	0.01 μ F	CAP, CERM, 0.01 μ F, 50 V, +/- 5%, C0G/NP0, 0805	0805	GRM2195C1H103JA01D	MuRata
D1	1	3.6V	Diode, Zener, 3.6 V, 500 mW, SOD-123	SOD-123	MMSZ4685-E3-08	Vishay-Semiconductor
D2, D4	2	7.5V	Diode, Zener, 7.5 V, 500 mW, SOD-123	SOD-123	MMSZ4693T1G	ON Semiconductor
D3	1	Green	LED, Green, SMD	0603 LED	SM0603GCL	Bivar
H1, H2	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H3, H4, H5, H6	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
H7, H8	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Würth Elektronik
J1, J3, J6	3		Terminal Block, 3.5mm, 3x1, Tin, TH	Terminal Block, 3.5mm, 3x1, Tin, TH	691214110003	Würth Elektronik
J2, J4, JP3, JP4, JP5, JP6, JP8	7		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J7, J8, J9	3		Terminal Block, 3.5mm, 2x1, Tin, TH	Receptacle, 3.5mm, 2x1, TH	691214110002	Würth Elektronik
J10	1		Header, 100mil, 14x2, Gold, TH	14x2 Header	TSW-114-07-G-D	Samtec
J11	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A-K-TR	Samtec
R1, R2, R4, R8, R55, R57, R58, R59, R60, R61, R62, R63, R64, R67, R68, R74, R75, R76	18	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R3, R6	2	0.1	RES, 0.1, 1%, 0.125 W, AEC-Q200 Grade 1, 0805	0805	RL0805FR-070R1L	Yageo America
R5	1	37.4	RES, 37.4, 1%, 0.1 W, 0603	0603	RC0603FR-0737R4L	Yageo
R10, R11, R13, R14, R15, R17, R18, R19, R20, R22, R23, R25, R69, R72, R73	15	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	RC0402FR-0749R9L	Yageo America
R12, R21, R26, R27, R28, R29, R30, R35, R39	9	221	RES, 221, 0.1%, 0.1 W, 0603	0603	RT0603BRD07221RL	Yageo America
R16, R24, R31, R32, R36	5	20.0k	RES, 20.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060320K0FKEA	Vishay-Dale
R33, R34, R41, R65, R66, R70	6	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R37, R42, R44	3	1.00k	RES, 1.00 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERA3AEB102V	Panasonic
R40	1	4.02	RES, 4.02, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034R02FKEA	Vishay-Dale
R43	1	4.02k	RES, 4.02 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD074K02L	Yageo America
R45	1	1k	1 kOhms $\pm$ 0.1% 0.125W, 1/8W Chip Resistor 0805 (2012 Metric) Automotive AEC-Q200 Thin Film	0805	ERA-6ARB102V	Panasonic
R46, R47, R50	3	4.70	RES, 4.70, 1%, 0.5 W, AEC-Q200 Grade 0, 0805	0805	CRCW08054R70FKEAHP	Vishay-Dale
R48	1	82k	RES, 82 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060382K0JNEA	Vishay-Dale
R49	1	2.0k	RES, 2.0 k, 5%, 0.1 W, 0603	0603	RC0603JR-072KL	Yageo
R51	1	11.3k	RES, 11.3 k, 1%, 0.1 W, 0603	0603	RC0603FR-0711K3L	Yageo
R52, R53, R54	3	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RK73Z1ETTP	KOA Speer
SH-J1, SH-J2, SH-J3, SH-J4	4	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1	1		Test Point, Compact, White, TH	White Compact Testpoint	5007	Keystone Electronics
TP2	1		Test Point, Compact, Orange, TH	Orange Compact Testpoint	5008	Keystone Electronics
TP3, TP4	2		Test Point, Compact, Black, TH	Black Compact Testpoint	5006	Keystone Electronics
TP5	1		1mm Uninsulated Shorting Plug, 10.16mm spacing, TH	Shorting Plug, 10.16mm spacing, TH	D3082-05	Harwin
TP6	1		Test Point, Compact, Red, TH	Red Compact Testpoint	5005	Keystone Electronics
TP8	1		Test Point, Compact, Yellow, TH	Yellow Compact Testpoint	5009	Keystone Electronics
U1	1		2.9 uA, 90 kHz Rail-to-Rail I/O Operational Amplifier, 1.8 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DCK5), Green (RoHS & no Sb/Br)	DCK0005A	OPA379AIDCKT	Texas Instruments

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U2	1		Ultra-High-Resolution, 4kSPS, 2-Ch Delta-Sigma ADC With PGA for Seismic and Energy Exploration	TSSOP-28	ADS1282IPWR	Texas Instruments
U3	1		0.8ppm/°C Maximum Drift, 0.11ppmp-p 1/f Noise, 380µA Current, Precision Voltage Reference	SOIC8	REF54500CDR	Texas Instruments
U5	1		36V, Low Power, All-Purpose Amplifier with MUX-Friendly Input, DBV0005A (SOT-23-5)	DBV0005A	OPA196IDBVT	Texas Instruments
U6	1		Automotive 35V, 1A, 4.2µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4701QRGWRQ1	Texas Instruments
U7	1		Vin -3V to -36V, -200mA, Ultra-Low-Noise, High-PSRR, Low-Dropout (LDO) Linear Regulator, DRB0008A (VSON-8)	DRB0008A	TPS7A3001DRBR	Texas Instruments
U8	1		Flip Flop 2 Element D-Type 2 Bit Negative Edge 14-TSSOP (0.173", 4.40mm Width)	TSSOP14	SN74HCS72PWR	Texas Instruments
U9	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
Y1	1		Low Power LVCMOS Output BAW Oscillator, 8.192MHz, DLF0004A	VSON4	CDC6CE008192ADLFR	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J5, J12, JP1, JP2, JP7	0		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
R7, R9	0	75.0k	RES, 75.0 k, 0.1%, 0.1 W, 0603	0603	RG1608P-753-B-T5	Susumu Co Ltd
R38	0	1.00k	RES, 1.00 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERA3AEB102V	Panasonic
R56, R71	0	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
TP9, TP10	0		Test Point, SMT	Test Point, SMT	S2751-46R	Harwin
U4	0		36V, Low Power, All-Purpose Amplifier with MUX-Friendly Input, DBV0005A (SOT-23-5)	DBV0005A	OPA196IDBVT	Texas Instruments

6 Additional Information

6.1 Trademarks

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7 Related Documentation

7.1 Supplemental Content

Table 7-1 shows the related documentation from Texas Instruments.

Table 7-1. Related Documentation

Document	Literature Number
ADS1282 product datasheet	SBAS418
OPA196 product datasheet	SBOS869
REF54500 product datasheet	SNVSCN7
TPS7A3001 product datasheet	SBVS125
OPA379 product datasheet	SBOS347
TPS7A4701 product datasheet	SBVS204
SN74HCS72 product datasheet	SCLS801
CDC6C product datasheet	SNAS843

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2024) to Revision A (October 2026)	Page
• Updated document title from "ADS1282EVM-PDK Evaluation Module" to "ADS1282 Performance Demonstration Kit Evaluation Module".....	1
• Updated <i>Description</i> section.....	1
• Updated <i>Features</i> section.....	1
• Updated hardware image with updated board design to improve noise performance.....	1
• Updated Figure 1-1	2
• Updated Table 1-1	3
• Added Figure 1-2	3
• Updated <i>Hardware</i> section.....	4
• Updated Figure 2-1	4
• Updated text in <i>EVM Analog Input Options</i> section.....	4
• Updated Figure 2-2	5
• Updated title from <i>Analog Input 1 Circuit</i> to <i>Analog Input Circuit</i>	6
• Updated text in <i>Analog Input Circuit</i> section.....	6
• Deleted <i>Analog Input 2 Amplifier</i> section.....	7
• Added <i>RTD Current Source</i> section.....	7
• Updated Figure 2-6	8
• Updated text in <i>Voltage Reference</i> section.....	8
• Updated Figure 2-7	9
• Updated text in <i>ADC Connections and Decoupling</i> section.....	9
• Updated text in <i>Power Supplies</i> section.....	10
• Added Figure 2-8	10
• Updated Figure 2-9	10
• Deleted <i>Low Dropout Regulators (LDO)</i> section.....	12
• Changed title from <i>Flip-Flop/SYNC Circuit</i> to <i>SYNC / Clock Divide Circuit</i>	12

• Updated Figure 2-10	12
• Updated text in <i>SYNC / Clock Divide Circuit</i>	12
• Updated Figure 2-11	12
• Updated text in <i>Clocking</i> section.....	12
• Updated Figure 2-12	13
• Updated Figure 2-13	13
• Added <i>Using the ADS1282EVM With an External Controller</i> section.....	14
• Updated Figure 4-1	18
• Updated text in <i>Evaluation Setup</i> section.....	18
• Updated "AINP1_AIN22" to "AINP2_AINN2" in <i>Channel Configuration</i> section.....	20
• Updated text in <i>Data Rate Configuration</i> section.....	22
• Updated text describing measurements of spectral analysis "SNR, THD, THD+N, SFDR, and Dynamic Range" to "SNR, THD, SFDR, SINAD, and ENOB").....	24
• Updated Figure 4-8	24
• Updated Figure 4-9	25
• Added <i>GUI Data Export</i> section.....	26
• Updated Figure 5-1 , Figure 5-2 , and Figure 5-3	27
• Added Figure 5-4	27
• Updated Figure 5-5 through Figure 5-10	31
• Updated Table 5-1	34
• Updated Table 7-1 in <i>Supplemental Content</i> section.....	38

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