

# High Voltage Amplifier with Improved Howland Current Pump and Discrete Output Current Boost

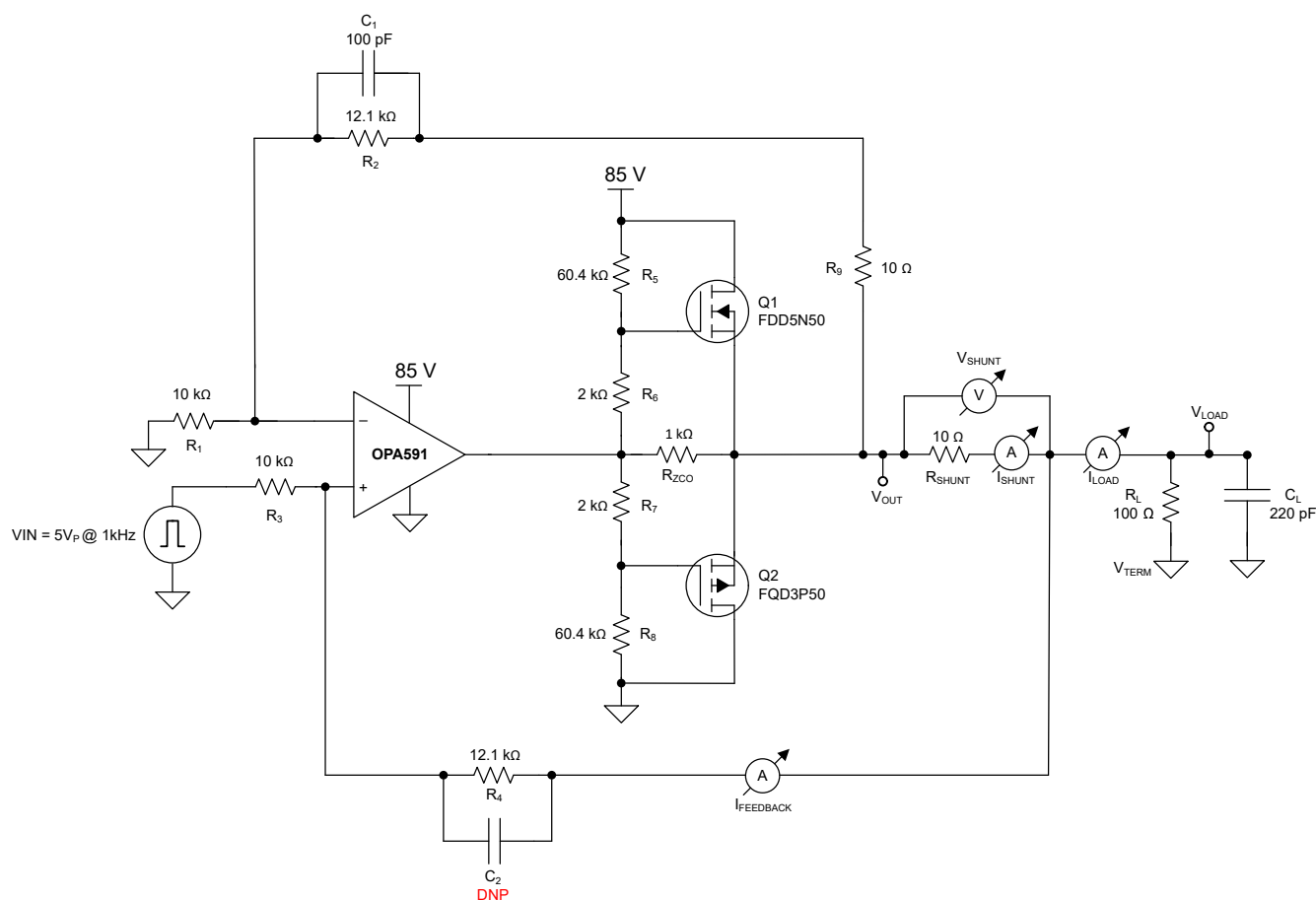


## Design Goals

| Input                         |      |        | Output          |            |
|-------------------------------|------|--------|-----------------|------------|
| $V_{IN}$                      | BW   | Gain   | $V_{LOAD}$      | $I_{LOAD}$ |
| $0\text{ V}_P - 5\text{ V}_P$ | 1kHz | 1.2V/V | $60\text{ V}_P$ | 600mA      |

## Design Description

This circuit implements an improved Howland current pump (IHCP) to drive a NMOS type transistor. This is a voltage controlled high current source, capable of delivering 600mA at 1kHz with negligible distortion. A digital to analog converter (DAC) can be used to create the voltage input signal. This circuit is designed to be operated at a single supply of 85V.



Improved Howland Current Pump with Discrete Output Current Boost Circuit

## Design Notes

1. Designing the Howland current pump can be an iterative process. First, determine the desired output current using a known shunt resistor value. Then, choose  $R_1$  and scale  $R_2$ ,  $R_3$ , and  $R_4$  accordingly. For full details and design notes for designing an IHCP, see the ["Improved" Howland current pump circuit](#) Analog Engineer's circuit.
2. This circuit is designed to source current. The polarity of the power supplies can be inverted ( $V_{EE} = -85V$  and  $V_{CC} = 0V$ ) to produce an identical circuit that sinks current. For this reason, complementary FET design is included in the schematic design.
3. Resistor mismatch contributes gain error and degrade CMRR of the circuit.
4. Error in final results can be expected due to  $I_{FEEDBACK}$  current. Placing high-value resistors will limit the effect of this current but will add thermal noise to the circuit. Possible bandwidth limitations and stability issues caused by large resistances and parasitic capacitances in the circuit also become more prevalent.
5. In an ideal "Improved" Howland current pump, resistor  $R_4$  is usually set equal to  $R_2 - R_9$ , which slightly alters the feedback network but results in the expected  $I_{LOAD}$  value. Accuracy of these resistors will limit the effectiveness of the technique at reducing errors.
6. A voltage divider network ( $R_5$ ,  $R_6$ ,  $R_7$ ,  $R_8$ ) provides nominal voltage to bias  $V_{GS}$ .
7. A capacitive load can be added to the output of the circuit. If using a capacitive load  $>200pF$ , further compensation may be needed to stabilize the circuit. See [Operational Amplifier Stability Theory and Compensation Methods](#) for information on stabilizing op amps.
8. Including a footprint for compensation capacitors  $C_1$  and  $C_2$  is recommended to provide flexibility for stability optimization. Instability can result from capacitive loading at the output node, large feedback resistors, or capacitance on the inverting input. During the bench measurements for this circuit design, ringing was seen on the input. The simulation and design was updated to include a feedback resistor in parallel with  $R_2$  ( $C_1$ ). Refer to the [Operational Amplifier Stability Theory and Compensation Methods](#) technical paper for a detailed discussion of op amp stability and compensation methods.
9. Choose a high voltage op amp to maximize the output swing of the circuit.
10. Verify input voltage is within the full power bandwidth and output voltage specifications for the given op amp. For an 85 V supply, slew induced distortion will become significant above 20 kHz (see Figure 6-3 and Figure 6-4 from [OPA591 datasheet](#)). This can also be calculated using the equation:

$$V_{pk} = \frac{SlewRate}{2\pi f} \quad (1)$$

Distortion becomes more significant the closer the output voltage is to the power supply rails. However, distortion in the output crossover region, resulting from the switching characteristics of the discrete transistors, differs from slew-rate-induced distortion. This crossover distortion is also dependent on the input and output capacitance of the transistors, and difficult to calculate empirically. Therefore, the best approach to determine if the desired input frequency is feasible is to simulate the circuit.

11. When designing the voltage divider that biases the MOSFET transistors, be aware of the trade-off in the size of the resistors. Smaller resistor values increase the current consumption through the bias path, but higher resistor values introduce higher thermal noise. In this example design,  $R_5$  and  $R_8$  were chosen to be 60.4k $\Omega$  for best results.
12. Careful consideration of the characteristics and tradeoffs between bipolar junction transistors (BJTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) is essential when choosing a discrete complementary output stage (see Table 3-1 from the application note [Optimizing Dual Feedback Compensation in the OPA593 With a Current Booster](#) for further detail).
13. Ensure the circuit is operating within the safe operating area (SOA) of the MOSFET. Consider reducing the power supply to limit the power dissipation within the circuit. This is particularly important when using a DC input source rather than an AC source, as the overall power of the circuit is inherently higher in DC configurations. If the operating range of the circuit exceeds the SOA of the MOSFET, thermal runaway can occur and damage the MOSFET.
14. Components in output path of the transistors, such as the load resistor,  $R_L$ , must have adequate power ratings. High voltage and high-power PCB layout guidelines should also be followed ([see the TIPL training on Power and Temperature](#)). Consider using a fan to help reduce the heat that the circuit can generate.

## Design Steps

1. Calculate gain (G) for a given  $I_{LOAD}$  and shunt resistor.

$$G = \frac{I_{LOAD} \times R_{SHUNT}}{V_{IN}} = \frac{600mA \times 10\Omega}{5V} = 1.2V/V \quad (2)$$

2. Ensure  $V_{OUT}$  is within the voltage output swing from rails ( $V_{OUT\_MIN}$ ,  $V_{OUT\_MAX}$ ) of the op amp.

$$V_{OUT\_MIN} < V_{OUT} < V_{OUT\_MAX} \quad (3)$$

$$V_{OUT} = (I_{LOAD} \times R_L) + V_{SHUNT} \quad (4)$$

$$V_{OUT} = 0 + (600mA \times 100\Omega) + 6V \quad (5)$$

$$V_{OUT} = 66V \quad (6)$$

3. Calculate the output power of the circuit and select the MOSFET with appropriate power dissipation capabilities. The output FET power will be a function of the load, output voltage and supply voltage. For a square wave output with resistive loads, with the load ground-referenced, the average power can be found using the equation:

The TINA-TI simulation results showing a maximum output power of approximately 22 W. Note that the output of the amplifier is significantly lower, consuming approximately 400mW of power, demonstrating the benefits of this circuit configuration. Select MOSFETs that have greater than 30W of power dissipation capability, such as FDD5N50, which has a power dissipation of at least 50 W. The maximum power dissipation at the output stage with a resistive load can be calculated using the following equation. Note that power consumption will vary with the load type (resistive vs. current). Refer to the [TIPL on Power and Temperature](#) for further details.

$$P_{AVG} = \frac{V_{OUT}^2}{R_L} \times DUTY\_CYCLE \quad (7)$$

$$P_{AVG} = \frac{(66V)^2}{100\Omega} \times 0.5 \quad (8)$$

$$P_{AVG} = 21.78W \quad (9)$$

4. Select a zero-crossover resistor ( $R_{ZCO}$ ) that provides sufficient current to drive the circuit while the MOSFET is off. Consider the trade-offs when selecting the  $R_{ZCO}$ .  $R_{ZCO}$  must be high enough to avoid current limit of the amplifier, but low enough to minimize noise and crossover distortion. A large  $R_{ZCO}$ , when paired with a capacitive load, can result in slower transients. However, a larger  $R_{ZCO}$  results in lower power dissipation.

The value of  $R_{ZCO}$  can be iteratively determined through simulation. The results shown below demonstrate that resistor values below 100 $\Omega$  cannot fully drive the loop. The 499  $\Omega$  resistor value drives 10.29mA of current, while the 1 k $\Omega$  drives 5.14 mA of current. The 1k $\Omega$  resistor has a thermal noise of approximately 4nV/ $\sqrt{Hz}$ , which is smaller than the op amp voltage noise of 13 nV/ $\sqrt{Hz}$ . Therefore, 1k $\Omega$  is a good choice for the  $R_{ZCO}$ , optimizing for both voltage noise and low power dissipation.

5. Calculate the voltage divider resistor values based on the  $V_{TH}$  of the selected MOSFET or BJT. To minimize power dissipation from VCC and VEE, use relatively large resistance for  $R_5$ .

Given:  $R_5 = 60.4 \text{ k}\Omega$ .

From the FDD5N50 datasheet,  $3 \text{ V} < V_{GS(th)} < 5 \text{ V}$ .

Optimize the resistor divider network by selecting  $R_6$  such that  $V_{GS(th)} = 3 \text{ V}$ .

Set  $V_{GS}$  to nominal value 3 V to optimize for crossover distortion without cross conduction.

$$V_{GS} = \frac{R_6}{R_5 + R_6} \times VCC \quad (10)$$

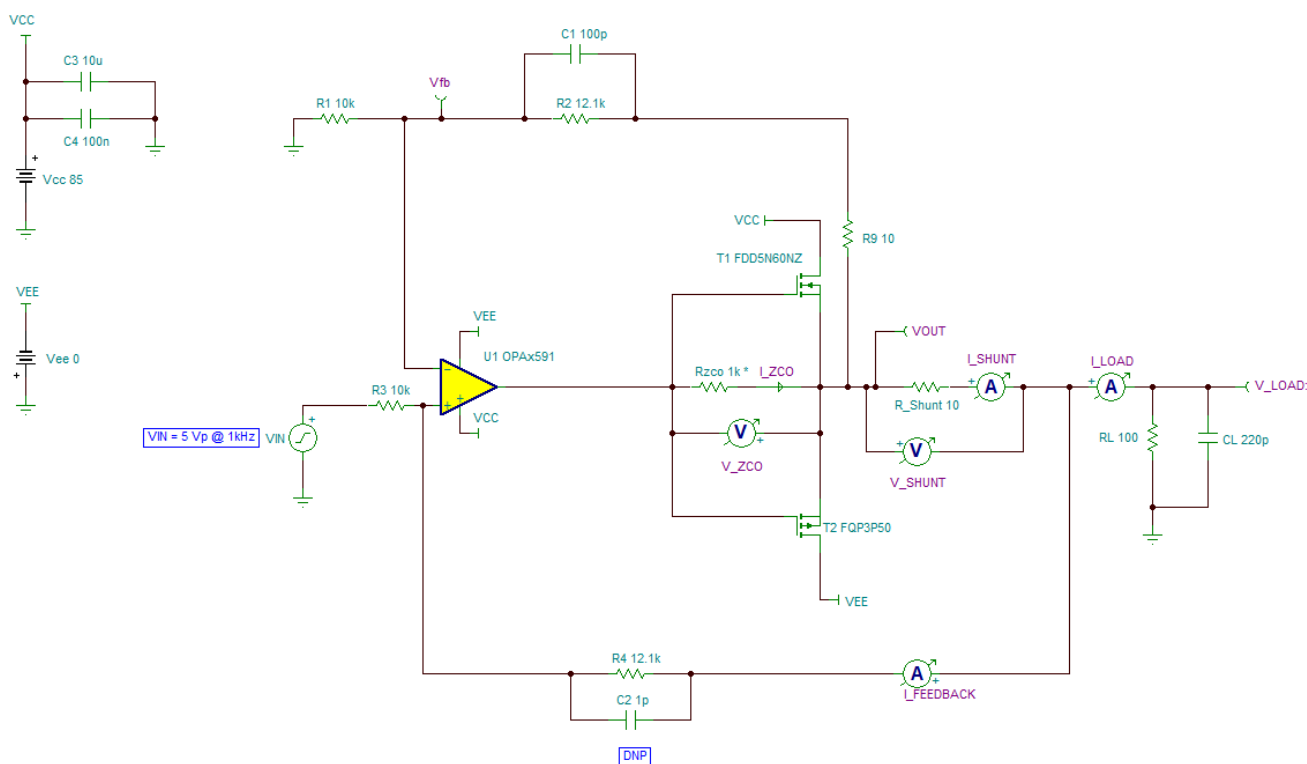
$$3V = \frac{R_6}{60.4k\Omega + R_6} \times 85V \quad (11)$$

$$R_6 = 2209.76\Omega \quad (12)$$

Choose conservative standard resistor value such that  $R_6 = R_7 = 2k\Omega$ .

$R_6$  and  $R_7$  can be further optimized for crossover distortion empirically, as individual  $V_{GS(th)}$  values for the chosen MOSFET varies due to process variation.

## Design Simulation Results

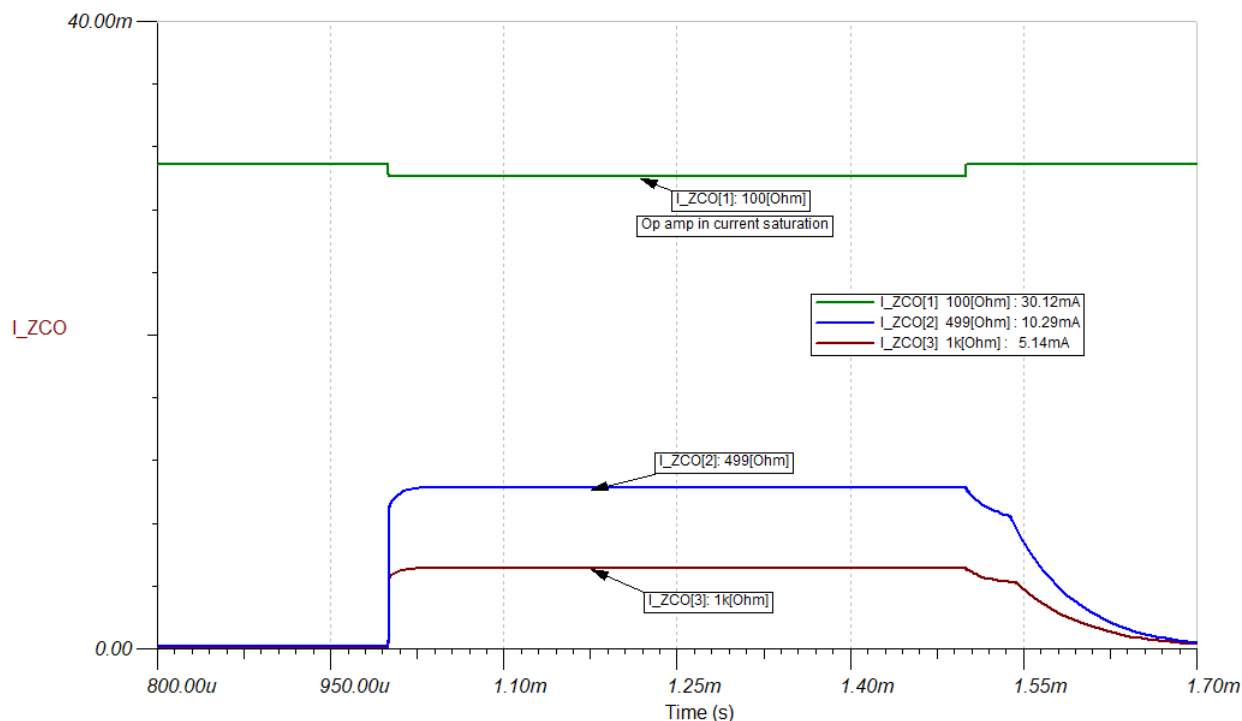


### OPA591 IHCP + Discrete Output Current Boost $R_{ZCO}$ TINA Circuit

#### Note

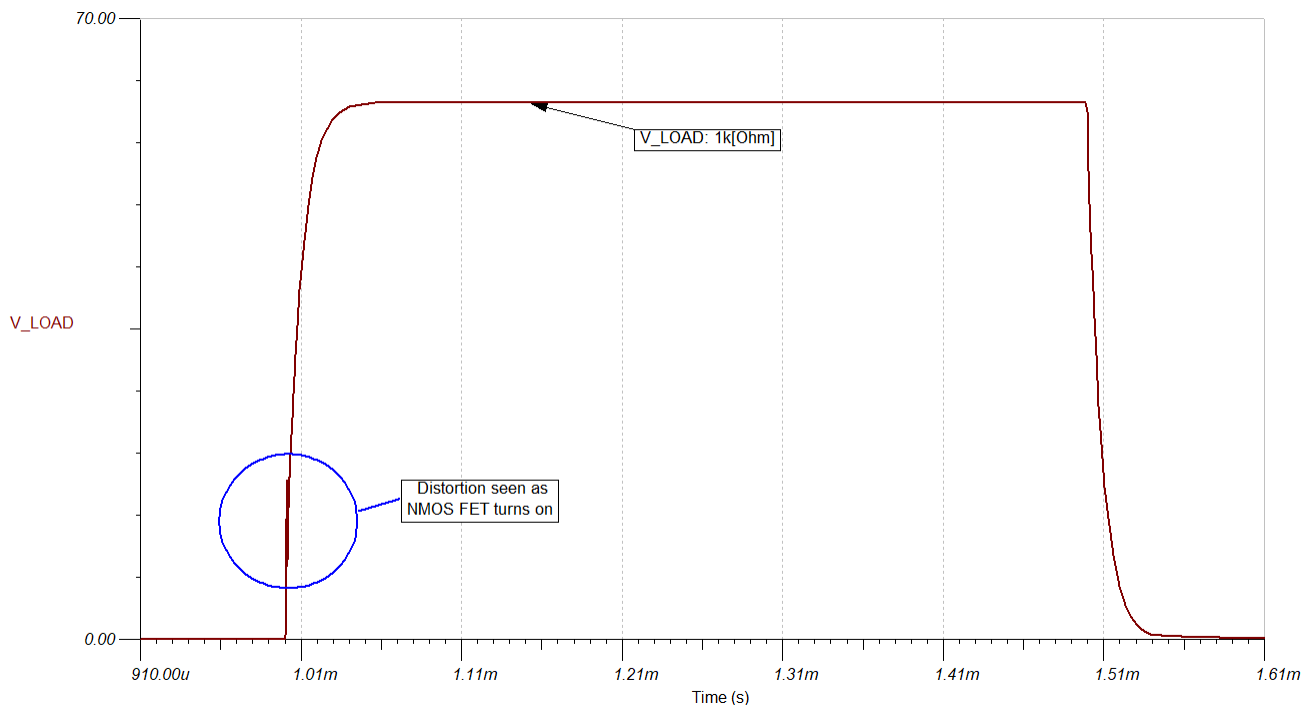
The SPICE model FDD5N60NZ was used for modeling since there is no model available for the 500 V version of the NMOS.

TINA simulations are run originally without the voltage divider as part of the circuit. This allows for insight into the optimized value of  $R_{ZCO}$ . Later, a voltage divider is added to the circuit to further optimize crossover distortion.



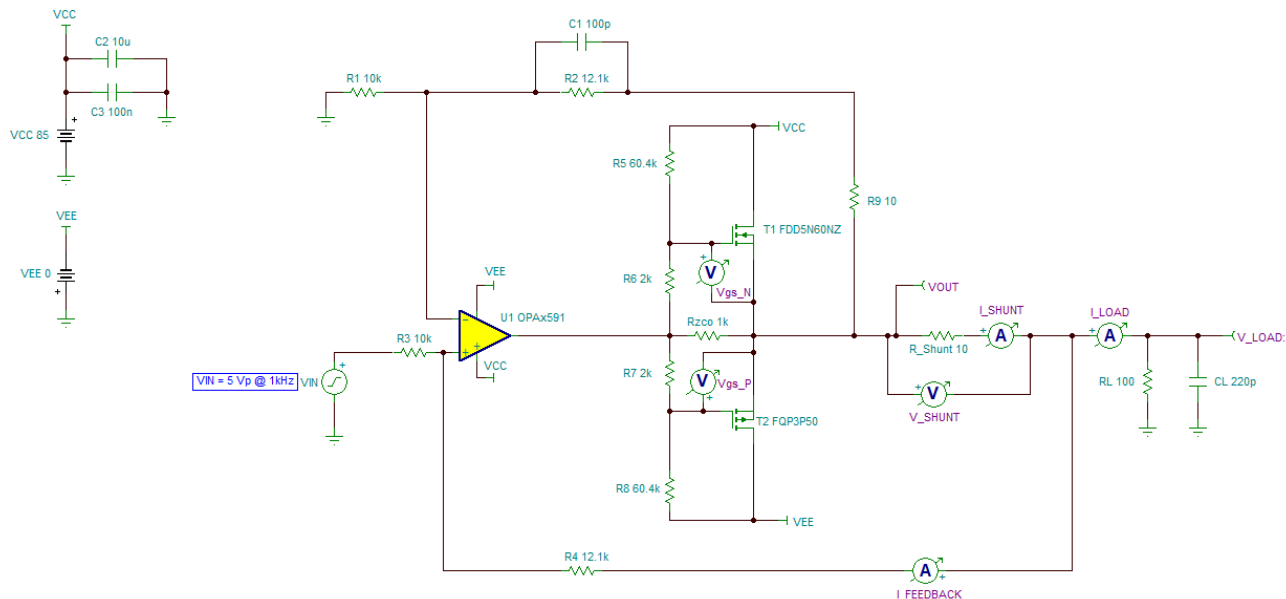
### OPA591 Discrete Output Current Boost $R_{ZCO}$ TINA Circuit

A 5V<sub>P</sub> square wave is applied to the input of the circuit. The output response provides insight into the current driving the load when the MOSFETs are turned off. Selecting  $R_{ZCO}$  resistors that are too low (100  $\Omega$ , 499  $\Omega$ ) result in excessive current flow (labelled  $I_{ZCO}$ ) from the output of the amplifier. Here, 1 k $\Omega$  was chosen for  $R_{ZCO}$  as it adds 5.14mA of current to the circuit, as opposed to the 10.29mA of current consumption with the 499  $\Omega$  resistor (see the figure above). Furthermore, the noise difference between the 499 $\Omega$  resistor and the 1kohm resistor is minimal, making 1 k $\Omega$  a suitable choice for  $R_{ZCO}$ . A larger resistor can be used but will add additional noise to the circuit.



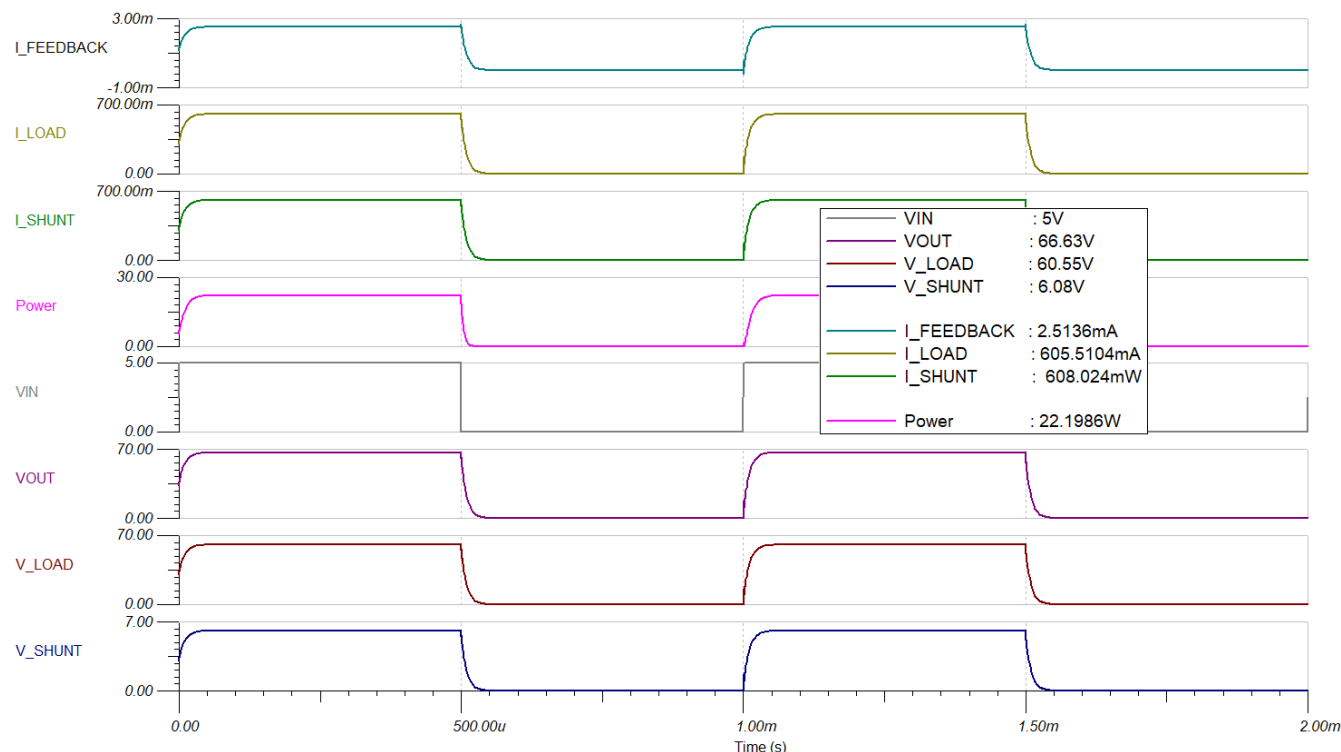
### Simulation Results for $R_{ZCO}$ and Corresponding $I_{ZCO}$ Values

Looking at  $V_{LOAD}$  when  $R_{ZCO} = 1k\Omega$ , there is still distortion. This distortion is due to the NMOS FET turning on. Adding a voltage divider to the circuit allows for a controlled  $V_{GS}$  that is continuously applied to the gate of the MOSFET.



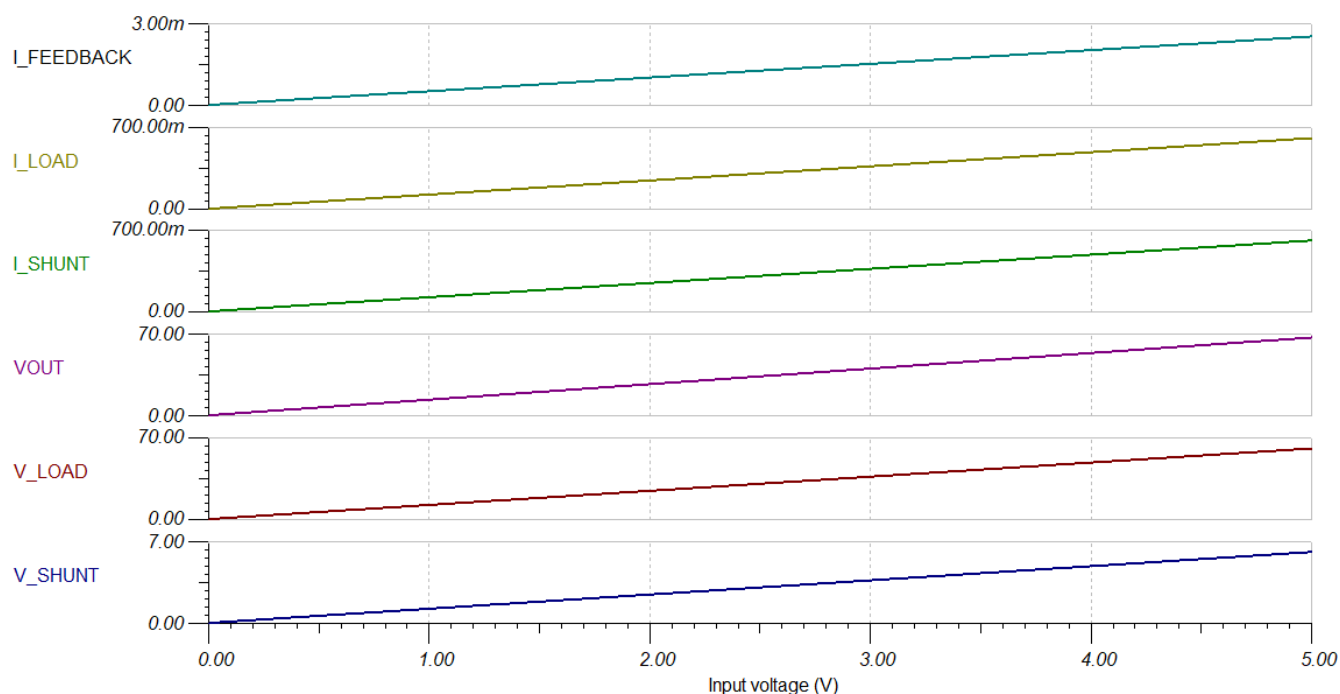
**OPA591 IHCP + Discrete Output Current Boost Circuit TINA Circuit**

OPA591 Discrete Output Current Boost Circuit Transient Simulation Results and OPA591 Discrete Output Current Boost Circuit DC Sweep Simulation Results show the simulated design results for the completed circuit. The distortion on the output has been minimized after adding a voltage divider to the gate of the MOSFET.



**OPA591 Discrete Output Current Boost Circuit Transient Simulation Results**

The post processor in TINA is used to calculate the average output power of the circuit (seen at node VOUT), using the same calculation as seen above in [Equation 8](#).



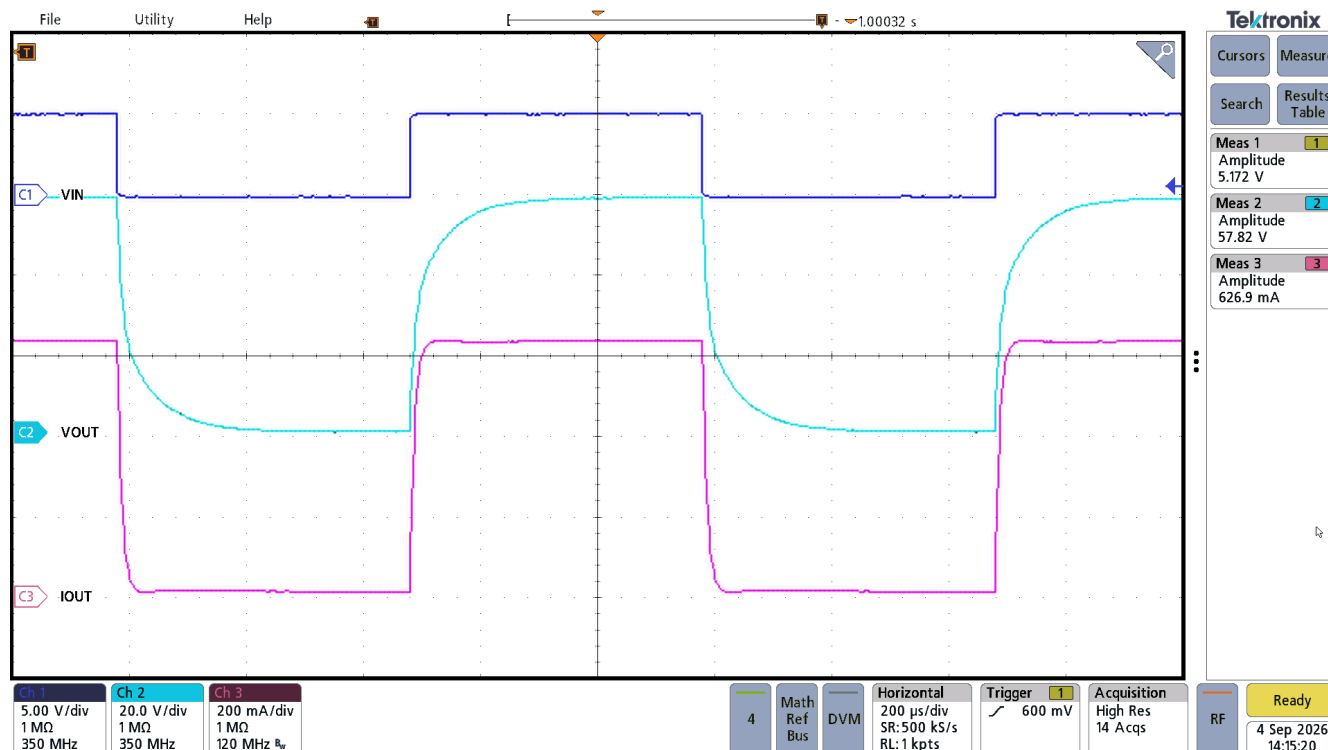
### OPA591 Discrete Output Current Boost Circuit DC Sweep Simulation Results

The DC sweep analysis in TINA shows the linear relationship between the input voltage and the output current.

## Design Measured Results

See below for oscilloscope results for the circuit.

| Input         |      |        | Output     |            |
|---------------|------|--------|------------|------------|
| $V_{IN}$      | BW   | Gain   | $V_{LOAD}$ | $I_{LOAD}$ |
| $0V_P - 5V_P$ | 1kHz | 1.2V/V | $60V_P$    | 600mA      |



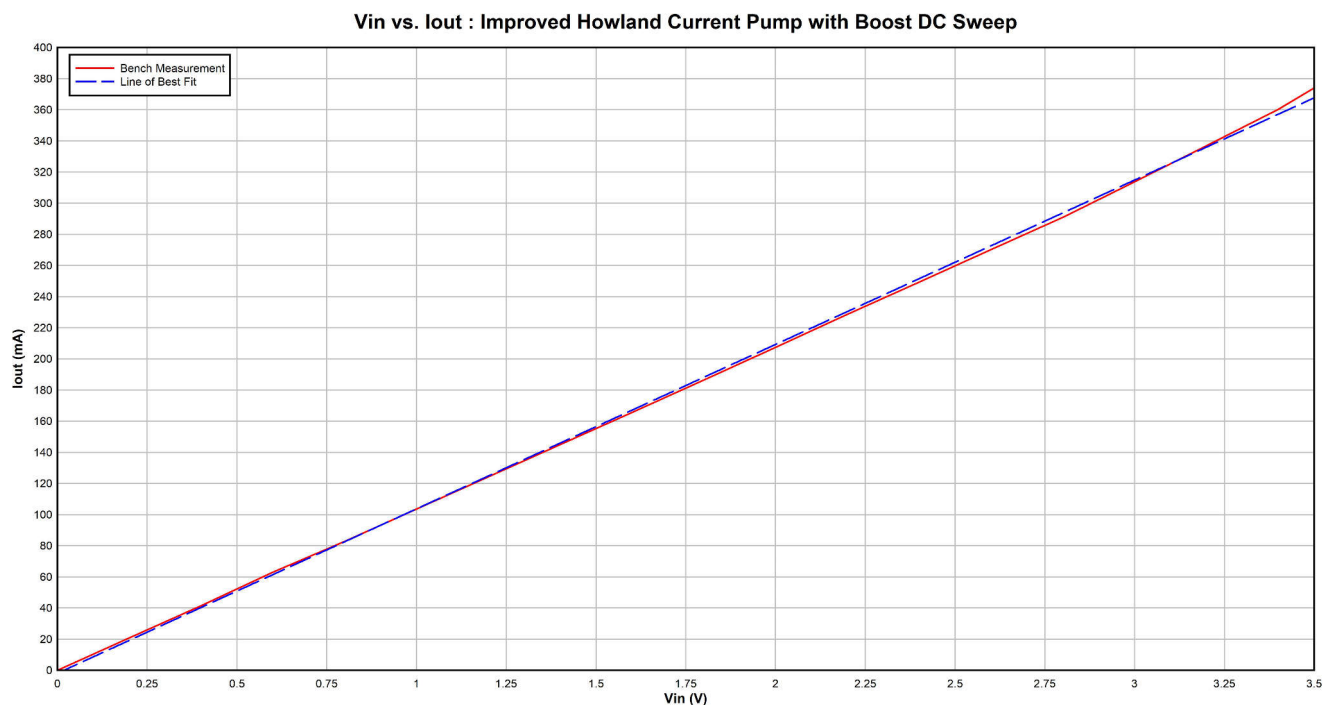
### OPA591 DC Sweep Measured Results ( $V_{in} = 5V_P @ 1\text{ kHz}$ )

A square waveform from  $0-5V_P$  is applied to the circuit. The OPA591 DC Sweep Measured Results above shows the relationship between  $V_{IN}$ ,  $V_{OUT}$ , and  $I_{OUT}$ , verifying the Improved Howland Current Pump and Discrete Output Boost circuit is behaving as expected.

| Input           |       | Output     |             |
|-----------------|-------|------------|-------------|
| $V_{IN}$        | $V_S$ | $V_{LOAD}$ | $I_{LOAD}$  |
| $0V_P - 3.5V_P$ | 60V   | $37.4V_P$  | 0mA - 384mA |

Since a DC signal has a higher power equivalence for the same input voltage, the voltage supply of the circuit is decreased to 60V. A DC sweep from  $0 - 3.5V_P$  is applied to the circuit. The figure below shows the linear behavior between  $V_{IN}$  and  $I_{OUT}$ , verifying the Improved Howland Current Pump and Discrete Output Boost circuit is behaving as expected. The line of best fit is included, showing small deviation from the expected

values. At  $3.5V_P$ , the output current deviates from the expected value. This is due to the high power dissipation of the circuit. As the MOSFET temperature increases, the output becomes less linear.



**V<sub>IN</sub> vs. I<sub>OUT</sub> : DC Sweep Measured Results**

## Target Applications

- High Voltage / High Signal Generator
- Parametric Measurement Unit
- Source Measurement Unit

## Design Featured Device

| OPA591           |                                                                                 |
|------------------|---------------------------------------------------------------------------------|
| V <sub>SS</sub>  | 8V to 85V                                                                       |
| V <sub>OUT</sub> | (V <sub>-</sub> ) + 0.5 to (V <sub>+</sub> ) – 0.5 (with R <sub>L</sub> = 10kΩ) |
| V <sub>OS</sub>  | 200μV                                                                           |
| I <sub>Q</sub>   | 500μA                                                                           |
| UGBW             | 3MHz (G = 10)                                                                   |
| Slew Rate        | 100V/μs                                                                         |
| OPA591           |                                                                                 |

## Design Alternative Device

| OPA596    |                                                    |
|-----------|----------------------------------------------------|
| $V_{SS}$  | 8V to 85V                                          |
| $V_{OUT}$ | (V-) + 0.5 to (V+) – 0.5 (with $R_L = 10k\Omega$ ) |
| $V_{OS}$  | 1mV                                                |
| $I_Q$     | 500 $\mu$ A                                        |
| UGBW      | 3MHz (G = 10)                                      |
| Slew Rate | 100V/ $\mu$ s                                      |
| OPA596    |                                                    |

## Design References

1. Texas Instruments, OPA591 Discrete Output Current Boost Circuit, TINA-TI simulation files [SBOMCV6](#)
2. Texas Instruments, [OPA591 TINA-TI Spice Model](#)

## 1 Additional Resources

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Last updated 10/2025