

XTR11x 4-20mA Current-Loop Transmitters

1 Features

- Low quiescent current: 200µA
- 5V regulator for external circuits
- V_{REF} for sensor excitation:
 - XTR115: 2.5V
 - XTR116: 4.096V
- Low span error: 0.05%
- Low nonlinearity error: 0.003%
- Wide loop supply range: 7.5V to 36V
- SOIC-8 package

2 Applications

- [Field transmitter & sensor](#)
- [Flow transmitter](#)
- [Temperature transmitter](#)
- [PLC, DCS, & PAC](#)
- Two-wire, 4-20mA current loop transmitter
- Voltage-to-current amplifier
- Compatible with HART modem

3 Description

The XTR115 and XTR116 (XTR11x) are precision current output converters designed to transmit analog 4mA to 20mA signals over an industry standard current loop. These devices provide accurate current scaling and output current limit functions.

The on-chip voltage regulator (5V) can be used to power external circuitry. A precision on-chip V_{REF} (2.5V for the XTR115 and 4.096V for the XTR116) can be used for offsetting or to excite transducers. A current return pin (I_{RET}) senses any current used in external circuitry to provide an accurate control of the output current.

The XTR11x are a fundamental building block of smart sensors using 4mA to 20mA current transmission.

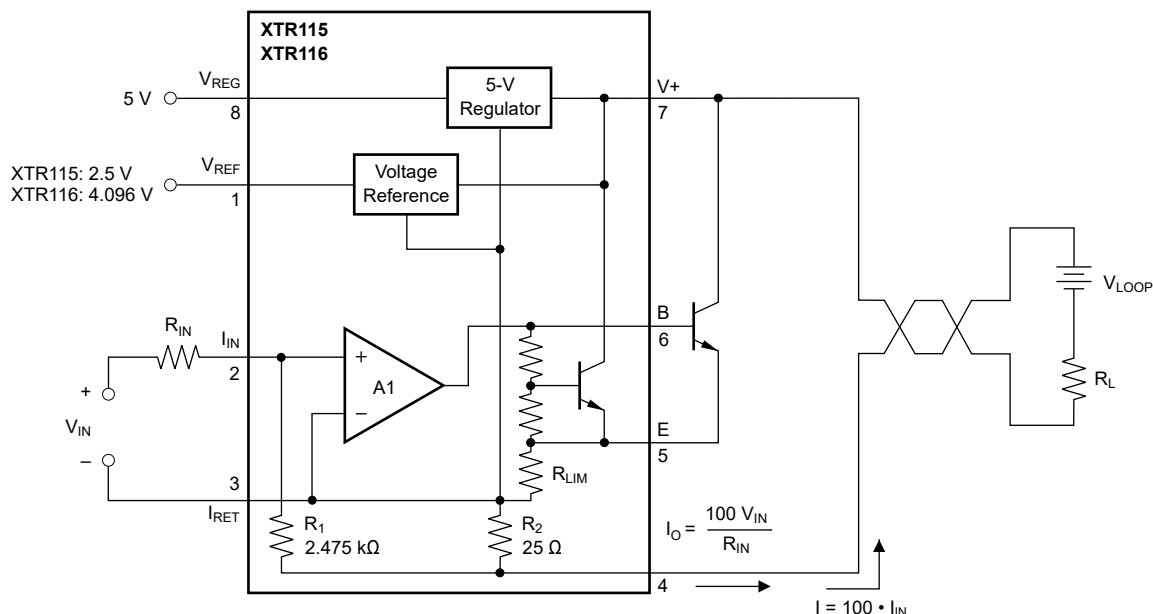
The XTR11x are specified for operation over the extended industrial temperature range, -40°C to $+85^{\circ}\text{C}$.

Package Information

PRODUCT	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
XTR115	D (SOIC, 8)	4.90mm × 3.90mm
XTR116	D (SOIC, 8)	4.90mm × 3.90mm

(1) For more information, see [Section 13](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application



Table of Contents

1 Features	1	8 Application and Implementation	11
2 Applications	1	8.1 Application Information.....	11
3 Description	1	9 Power Supply Recommendations	15
4 Device Comparison	3	10 Layout	15
5 Pin Configuration and Functions	4	10.1 Layout Guidelines.....	15
6 Specifications	5	11 Device and Documentation Support	16
6.1 Absolute Maximum Ratings.....	5	11.1 Device Support.....	16
6.2 Recommended Operating Conditions.....	5	11.2 Documentation Support.....	16
6.3 Thermal Information.....	5	11.3 Receiving Notification of Documentation Updates..	16
6.4 Electrical Characteristics.....	6	11.4 Support Resources.....	16
6.5 Typical Characteristics.....	8	11.5 Trademarks.....	16
7 Detailed Description	9	11.6 Electrostatic Discharge Caution.....	16
7.1 Overview.....	9	11.7 Glossary.....	16
7.2 Functional Block Diagram.....	9	12 Revision History	17
7.3 Feature Description.....	10	13 Mechanical, Packaging, and Orderable Information	17
7.4 Device Functional Modes.....	10		

4 Device Comparison

Related 4-20mA devices

DEVICE	DESCRIPTION ⁽¹⁾
XTR115	5V regulator output and 2.5V reference output
XTR116	5V regulator output and 4.096V reference output
XTR117	5V regulator output

(1) For complete 4-20mA bridge and RTO conditioner options, see the XTR product family at www.ti.com.

5 Pin Configuration and Functions

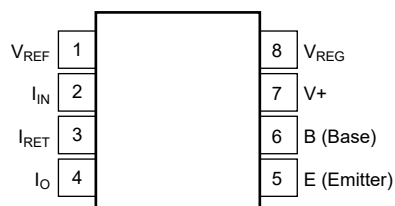


Figure 5-1. D Package, SOIC-8 (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V _{REF}	Output	Reference voltage output (2.5V for XTR115, 4.096V for XTR116)
2	I _{IN}	Input	Current input pin
3	I _{RET}	Input	Local ground return pin for V _{REG} and V _{REF}
4	I _O	Output	Regulated 4mA to 20mA current-loop output
5	E (Emitter)	Input	Emitter connection for external transistor
6	B (Base)	Output	Base connection for external transistor
7	V ₊	Power	Loop power supply
8	V _{REG}	Output	5V regulator voltage output

6 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see [Section 11.1](#).

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V+	Power supply (referenced to I _O pin)		40	V
	Input voltage (referenced to I _{RET} pin)	0	V+	V
	Output current limit	Continuous		
	V _{REG} short-circuit	Continuous		
	V _{REF} short-circuit	Continuous		
T _A	Operating temperature	–40	125	°C
T _{stg}	Storage temperature	–55	125	°C
	Lead temperature (soldering, 10s)		300	°C
T _J	Junction temperature		165	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Power supply voltage	7.5	24	36	V
T _A	Specified temperature	–40		85	°C

6.3 Thermal Information

THERMAL METRIC ⁽¹⁾		XTR115/6	UNIT
		8 PINS	
		D (SOIC)	
R _{θJA}	Junction-to-ambient thermal resistance	128.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	68.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	75.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	15.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	74.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application note.

6.4 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_+ = 24\text{V}$, $R_{IN} = 20\text{k}\Omega$ and TIP29C external transistor, all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
OUTPUT								
I _O	Output current equation				I _O = I _{IN} * 100			
	Output current, linear range				0.25		25	mA
I _{LIM}	Over-scale limit					32		mA
I _{MIN}	Under-scale limit	I _{REG} = 0, I _{REF} = 0				0.2	0.25	mA
SPAN								
S	Span (current gain)				100			A/A
	Error ⁽¹⁾	I _{OUT} = 250µA to 25mA	U variant		±0.05		±0.2	%
			UA variant		±0.05		±0.4	
			T _A = −40°C to +85°C		±3		±20	ppm/°C
	Nonlinearity	I _{OUT} = 250µA to 25mA	U variant		±0.003		±0.01	%
			UA variant		±0.003		±0.02	
INPUT								
V _{OS}	Offset voltage (op amp)	I _{IN} = 40µA	U variant		±100		±250	µV
			UA variant		±100		±500	
			T _A = −40°C to +85°C	U variant	±0.7		±3	µV/°C
		UA variant		±0.7		±6		
		V+ = 7.5V to 36V			±0.1		±2	µV/V
I _B	Bias current	CSO: SHE			−35			nA
		CSO: TID			−60			
	Bias current vs temperature	T _A = −40°C to +85°C	CSO: SHE		150			pA/°C
			CSO: TID		300			
e _n	Noise	0.1Hz to 10Hz			0.6			µVpp
DYNAMIC RESPONSE								
	Small signal bandwidth	C _{LOOP} = 0, R _L = 0			380			kHz
	Slew rate	CSO: SHE			3.2			mA/µs
		CSO: TID			5			
VOLTAGE REFERENCE (V _{REF})								
V _{REF}	Reference voltage ⁽²⁾	XTR115			2.5			V
		XTR116			4.096			
	Voltage accuracy	I _{REF} = 0	CSO: SHE	U variant	±0.05		±0.25	%
				UA variant	±0.05		±0.5	
			CSO: TID	U variant	±0.1		±0.25	
				UA variant	±0.1		±0.5	
	Voltage accuracy vs temperature	T _A = −40°C to +85°C	U variant		±20		±35	ppm/°C
			UA variant		±20		±75	
	Voltage accuracy	V+ = 7.5V to 36V			±1		±10	ppm/V
	Voltage accuracy vs load	I _{REF} = 0mA to 2.5mA	CSO: SHE		±100			ppm/mA
			CSO: TID		±200			
	Noise	0.1Hz to 10Hz			10			µVpp
	Short-circuit current				16			mA
VOLTAGE REGULATOR (V _{REG})								
V _{REG}	Regulator voltage ⁽²⁾				5			V
	Voltage accuracy	I _{REG} = 0	CSO: SHE		±0.05		±0.1	V
			CSO: TID		±0.003		±0.02	
	Voltage accuracy vs temperature	T _A = −40°C to +85°C			±0.1			mV/°C

at $T_A = 25^\circ\text{C}$, $V_+ = 24\text{V}$, $R_{IN} = 20\text{k}\Omega$ and TIP29C external transistor, all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Voltage accuracy vs supply voltage, V+	V+ = 7.5V to 36V	CSO: SHE		1		mV/V
			CSO: TID		0.5		mV/V
	Voltage accuracy vs output current			See Section 6.5			
	Short circuit current			12			mA
POWER SUPPLY							
I _Q	Quiescent current	I _O = 0	CSO: SHE		200	250	μA
				T _A = −40°C to 85°C	240	300	
			CSO: TID		165	250	
				T _A = −40°C to 85°C	190	300	

- (1) Does not include initial error or TCR of R_{IN} .
- (2) Voltage measured with respect to I_{RET} pin.

6.5 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_+ = 24\text{V}$, $R_{IN} = 20\text{k}\Omega$, TIP29C external transistor, and all chip site origin (CSO) (unless otherwise noted)

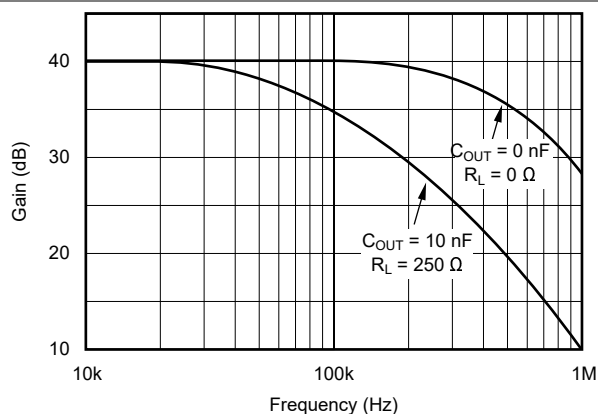


Figure 6-1. Current Gain vs Frequency

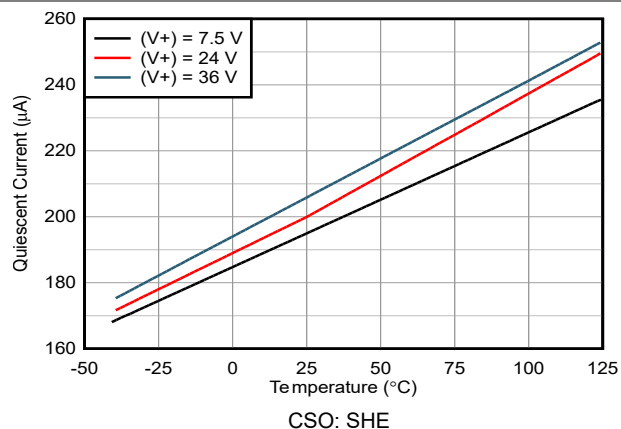


Figure 6-2. Quiescent Current vs Temperature

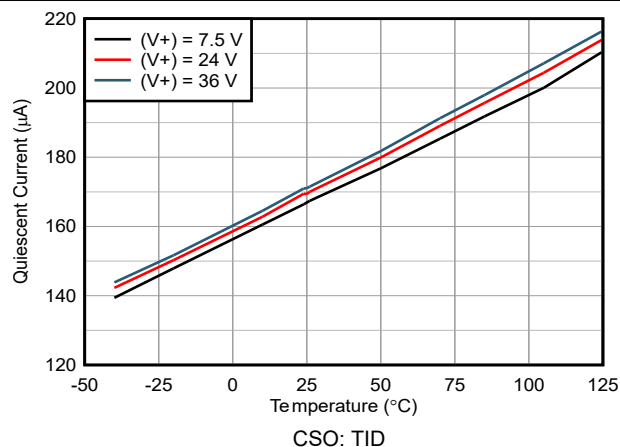


Figure 6-3. Quiescent Current vs Temperature

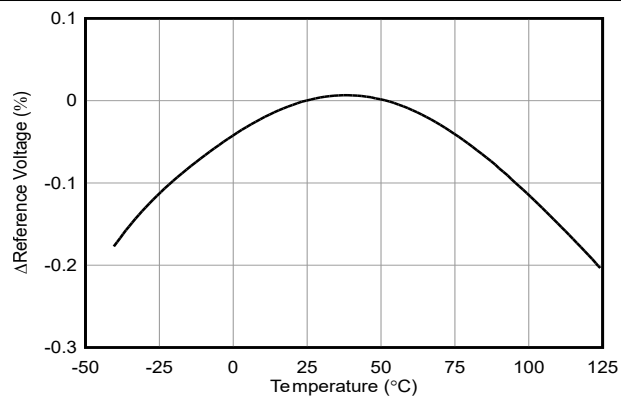


Figure 6-4. Reference Voltage vs Temperature

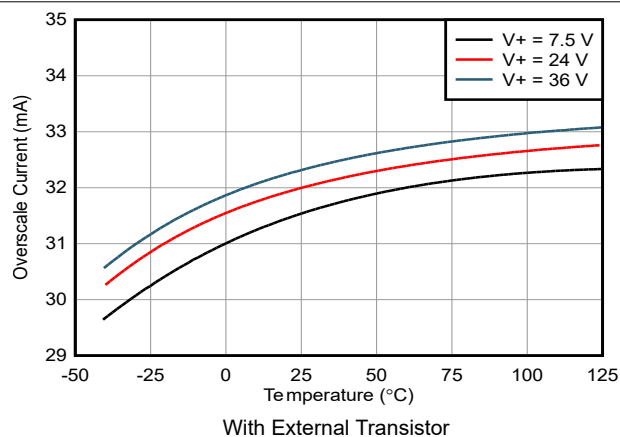


Figure 6-5. Overscale Current vs Temperature

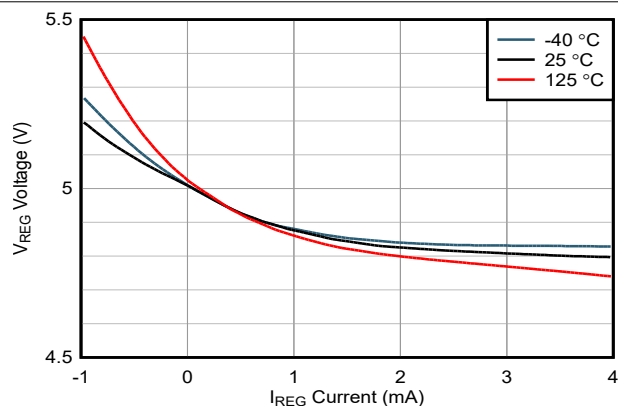
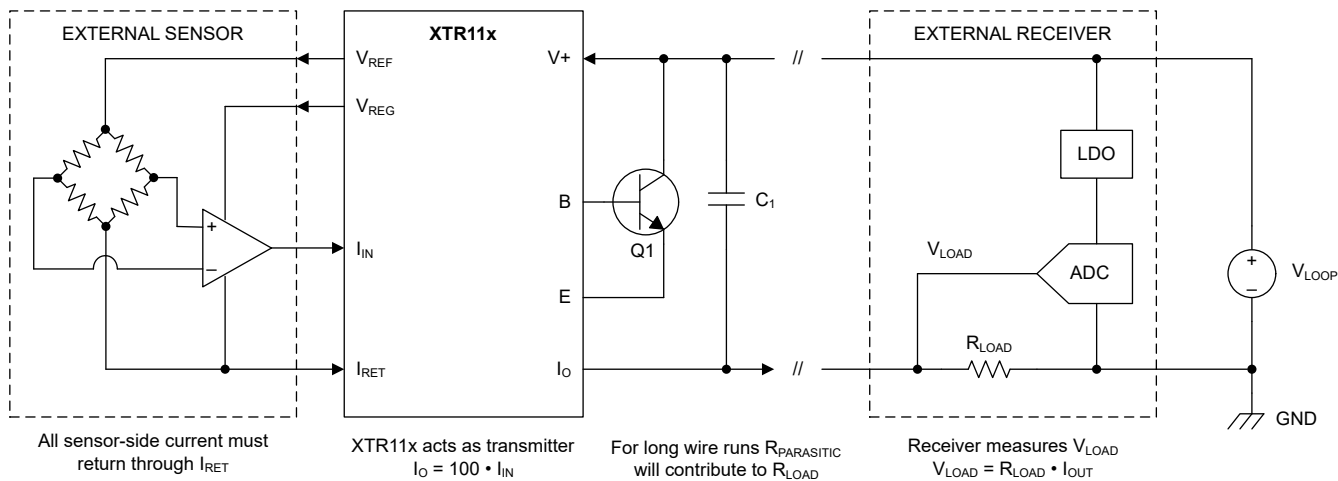


Figure 6-6. V_{REG} Voltage vs V_{REG} Current

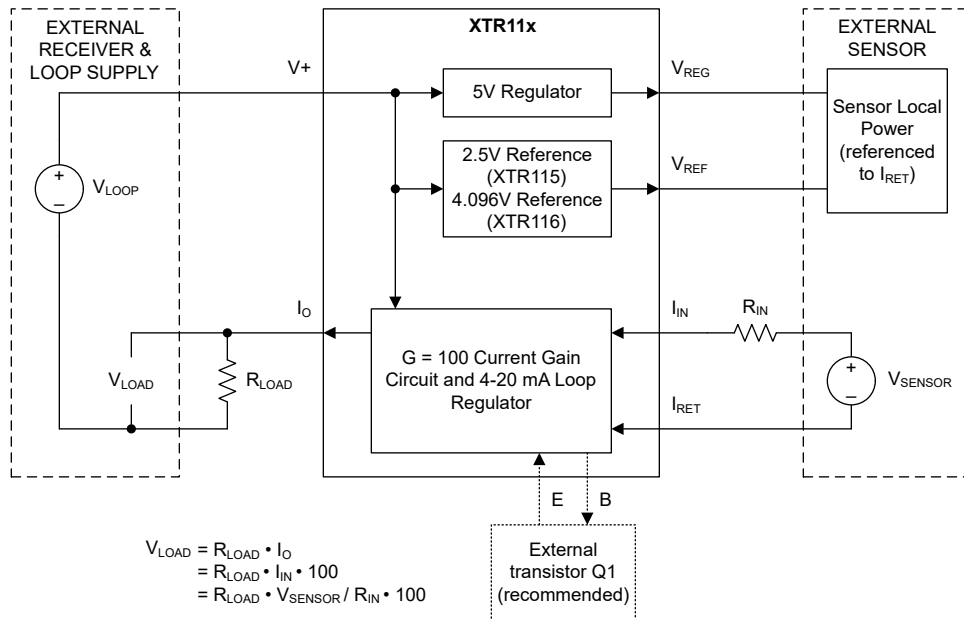
7 Detailed Description

7.1 Overview

The XTR115 and XTR116 are precision current output converters designed to transmit analog 4mA-to-20mA signals over an industry standard current loop. The regulator and reference voltages power a sensor, such as a bridge as shown in Figure 7-1. The sensor output, as a current signal I_{IN} , is gained up and transmitted over the loop to be read by a receiver.



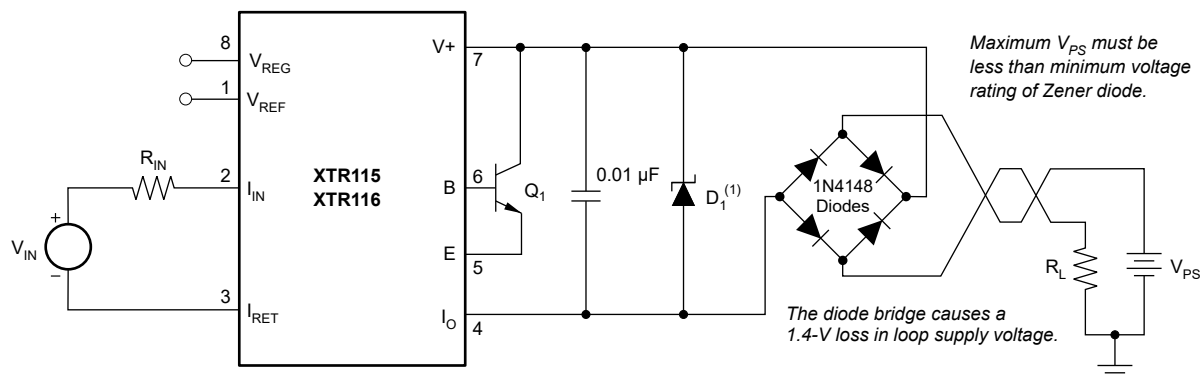
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reverse-Voltage Protection

The XTR11x low compliance voltage rating (7.5V) permits the use of various voltage protection methods without compromising the operating range. Figure 7-2 shows a diode bridge circuit that allows normal operation even when the voltage connection lines are reversed. The bridge causes a two-diode drop (approximately 1.4V) loss in loop supply voltage. This loss results in a compliance voltage of approximately 9V—satisfactory for most applications. A diode can be inserted in series with the loop supply voltage and the V+ pin to protect against reverse output connection lines with only a 0.7V loss in loop supply voltage.



(1) Zener Diode 36V: 1N4753A or Motorola P6KE39A. Use lower-voltage Zener diodes with loop power-supply voltages less than 30V for increased protection; see Section 7.3.2.

Figure 7-2. Reverse Voltage Operation and Overvoltage Surge Protection

7.3.2 Overvoltage Surge Protection

Remote connections to current transmitters can sometimes be subjected to voltage surges. Best practice is to limit the maximum surge voltage applied to the XTR11x to as low as practical. Various Zener and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. For example, a 36V protection diode provides proper transmitter operation at normal loop voltages, and also provides an appropriate level of protection against voltage surges. Characterization tests on several production lots showed no damage with loop supply voltages up to 65V.

Most surge protection Zener diodes have a diode characteristic in the forward direction that conducts excessive current, possibly damaging receiving-side circuitry if the loop connections are reversed. If a surge protection diode is used, also use a series diode or diode bridge for protection against reversed connections.

7.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

8 Application and Implementation

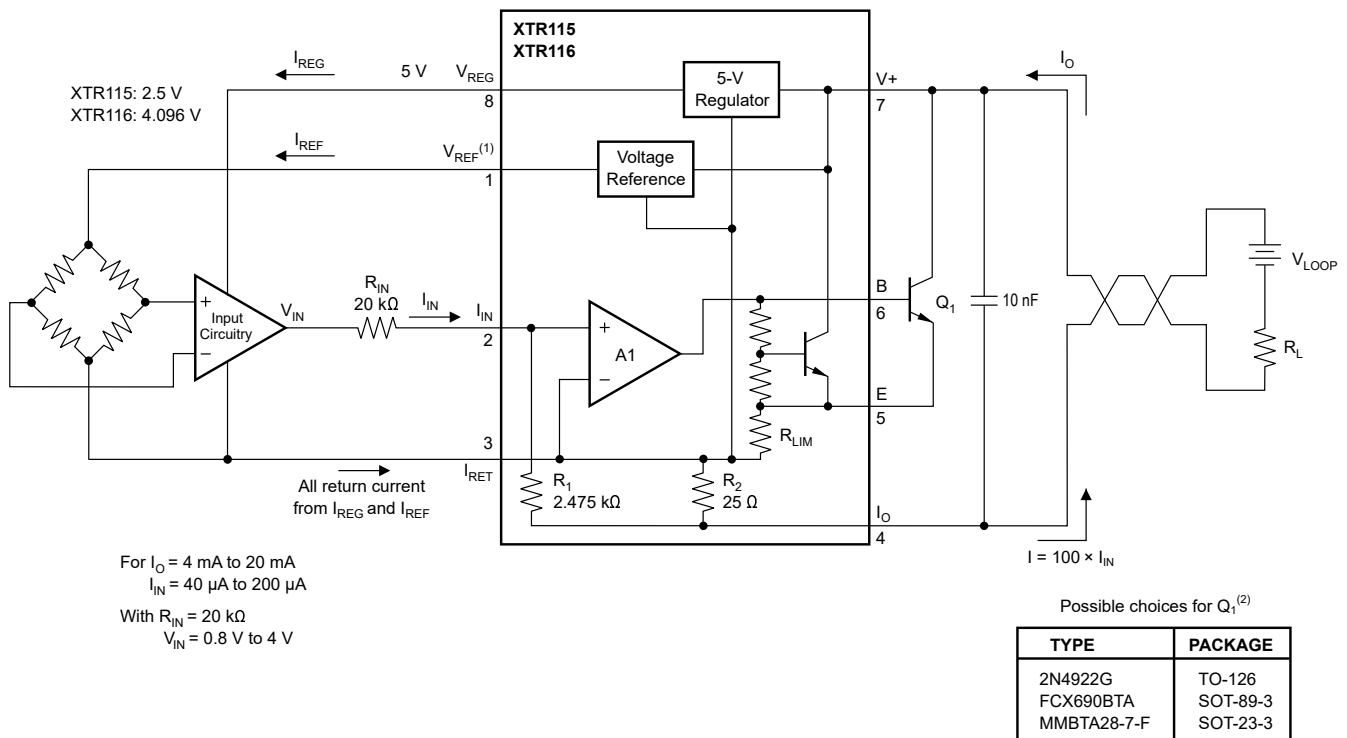
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The XTR115 and XTR116 are identical devices except for the reference voltage output, pin 1. This voltage is available for external circuitry and is not used internally. Further discussions that apply to both devices refer to the XTR11x.

Figure 8-1 shows basic circuit connections with representative simplified input circuitry. The XTR11x is a two-wire current transmitter. The device input signal (pin 2) controls the output current. A portion of this current flows into the V+ power supply, pin 7. The remaining current flows in Q₁. External input circuitry connected to the XTR11x can be powered from VREG or VREF. Current drawn from these terminals must be returned to IRET, pin 3. This IRET pin is a *local ground* for input circuitry driving the XTR11x.



(1) Also see Figure 8-4.

(2) See Section 8.1.1.

Figure 8-1. Basic Circuit Connections

The XTR11x is a current-input device with a gain of 100. A current flowing into pin 2 produces $I_O = 100 \cdot I_{IN}$. The input voltage at the I_{IN} pin is zero (referred to the I_{RET} pin). A voltage input is created with an external input resistor, as shown. Common full-scale input voltages range from 1V and upward. Full-scale inputs greater than 0.5V are recommended to minimize the effect of offset voltage and drift of A1.

8.1.1 External Transistor

The external transistor, Q_1 , conducts the majority of the full-scale output current. Power dissipation in this transistor can approach 0.8W with high loop voltage (40V) and 20mA of output current. The XTR11x is designed to use an external transistor to avoid on-chip, thermal-induced errors. Heat produced by Q_1 still causes ambient temperature changes that can affect the XTR11x. To minimize these effects, locate Q_1 away from sensitive analog circuitry, including the XTR11x. Mount Q_1 so that heat is conducted to the outside of the transducer housing and away from the XTR11x.

The XTR11x is designed to use virtually any NPN transistor with sufficient voltage, current, and power rating. Case style and thermal mounting considerations often influence the choice for any given application. Several possible choices are listed in Figure 8-1. A MOSFET transistor does not improve the accuracy of the XTR11x and is not recommended. Although the XTR11x can be used without an additional external transistor, this configuration is not always practical at higher loop voltages and currents because of self-heating concerns.

8.1.2 Minimum Scale Current

The quiescent current of the XTR11x (typically 200 μ A) is the lower limit of the device output current. Zero input current ($I_{IN} = 0$ A) produces an I_O equal to the quiescent current. Output current does not begin to increase until $I_{IN} > I_Q / 100$. Current drawn from V_{REF} or V_{REG} adds to this minimum output current. This means that more than 3.7mA is available to power external circuitry while still allowing the output current to go below 4mA.

8.1.3 Offsetting the Input

A low scale of 4mA is produced by creating a 40 μ A input current. This low-scale offset can be created with the proper value resistor from V_{REF} (as shown in Figure 8-2, or by generating offset in the input drive circuitry.

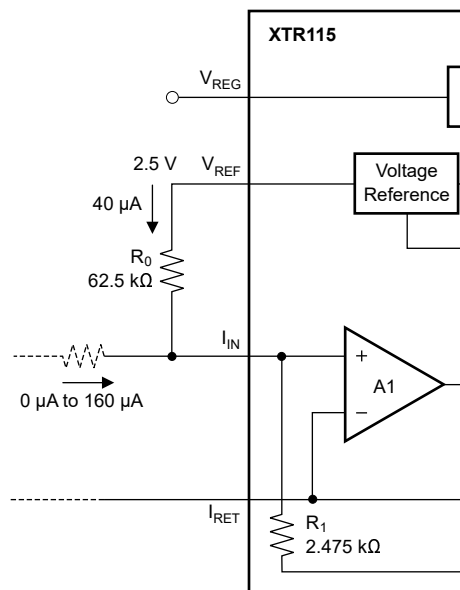


Figure 8-2. Creating Low-Scale Offset

8.1.4 Maximum Output Current

The XTR11x provide accurate, linear output up to 25mA. Internal circuitry limits the output current to approximately 32mA to protect the transmitter and loop power or measurement circuitry.

Extending the output current range of the XTR11x is possible by connecting an external resistor from pin 3 to pin 5 to change the current limit value.

CAUTION

All output current must flow through internal resistors; therefore, damage is possible with excessive current. Output currents greater than 45mA can cause permanent damage.

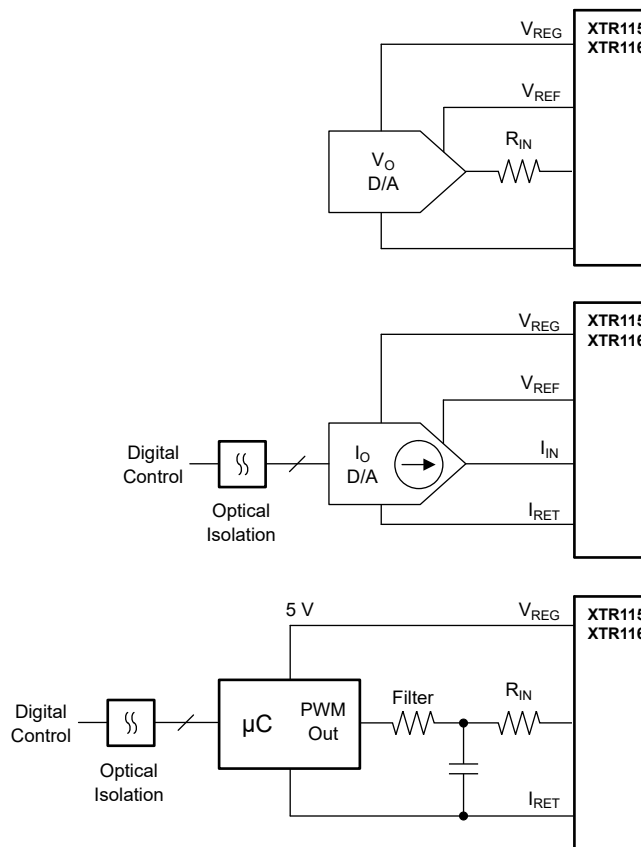


Figure 8-3. Digital Control Methods

8.1.5 Radio Frequency Interference

The long wire lengths of current loops invite radio frequency interference (RF). RF can be rectified by the input circuitry of the XTR11x or preceding circuitry. This RF generally appears as an unstable output current that varies with the position of loop supply or input wiring. Interference can also enter at the input pins. For integrated transmitter assemblies with short connection to the sensor, the interference more likely comes from the current-loop connections.

8.1.6 Circuit Stability

The 4-20mA control-loop stability must be evaluated for any XTR11x design. A 10nF decoupling capacitor between V+ and I_O is recommended for most applications. As this capacitance appears in parallel with the load resistance R_{LOAD} from a stability perspective, the capacitor and resistor form a filter corner that can limit the bandwidth of the system. Therefore, for HART applications, use a bypass capacitance of 2nF to 3nF instead.

For applications with EMI and EMC concerns, use a bypass capacitor with sufficiently low ESR to decouple any ripple voltage from the V_{LOOP} supply. Otherwise, the ripple voltage couples onto the 4mA to 20mA current source, and appears as noise across R_{LOAD} after the current-to-voltage conversion.

Additionally, stability concerns apply to the V_{REF} reference buffer when driving capacitive loads. Figure 8-4 shows that two filtering capacitors are required, one C_{HF} of 10pF to 0.5μF and another C_{LF} of 2.2μF to 22μF. Either a series isolation resistance R_{ISO} or a snubber R_{COMP} is used, depending on application requirements.

If capacitive loading must be placed on the VREF pin, use one of the following compensation schemes to maintain stable operation. Values of capacitance must remain within the given ranges.

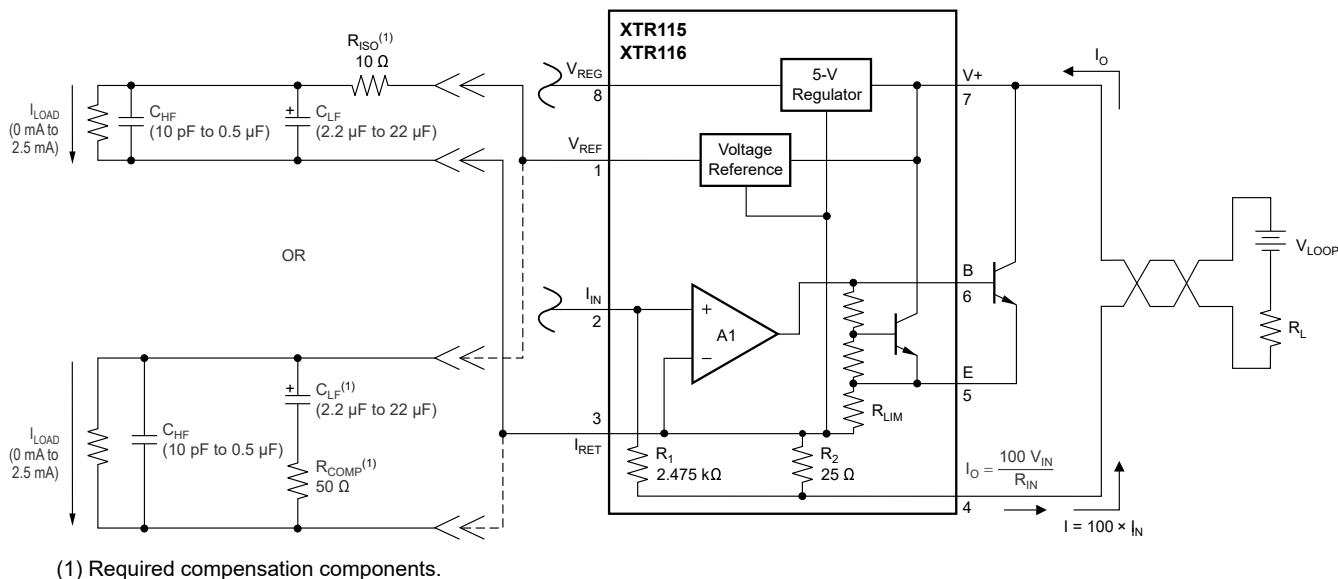


Figure 8-4. Stable Operation With Capacitive Load on V_{REF}

9 Power Supply Recommendations

The XTR11x operates over a supply voltage range of 7.5V to 36V, with a specified temperature of –40°C to 85°C.

CAUTION

Supply voltages larger than 40V can permanently damage the device; see [Section 6.1](#).

10 Layout

10.1 Layout Guidelines

Connect low-ESR, 0.1μF ceramic bypass capacitors between supply pin and ground, placed as close to the device as possible. If the loop power supply is electrically noisy, implement filtering using decoupling capacitors and small resistors or dampening inductors in series with V+.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Device Support

11.1.1 Device Nomenclature

Table 11-1. Device Nomenclature

Part Number	Definition
XTR115U/2K5 XTR115UA/2K5 XTR116U/2K5 XTR116UA/2K5	The die is manufactured in CSO: SHE or CSO: TID.
XTR115U XTR116U XTR116UA	The die is manufactured in CSO: SHE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Special Function Amplifiers: TI Precision Labs introduction video on Current Loop Transmitters](#)
- Texas Instruments, [TIPD190 2-wire, 4-20mA Transmitter, EMC/EMI Tested Reference Design](#) with the XTR116

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2022) to Revision C (January 2026)	Page
• Updated numbering format throughout the document.....	1
• Added standard package information and moved the comparison table to Device Comparison section.....	1
• Added description of device flow information in <i>Specifications</i>	5
• Added all chip site origin (CSO) to typical test conditions in <i>Electrical Characteristics</i>	5
• Added additional fabrication process specification for Bias Current and Bias Current vs Temperature in <i>Electrical Characteristics</i> table.....	6
• Added additional fabrication process specification for Slew Rate in <i>Electrical Characteristics</i> table.....	6
• Added additional fabrication process specification for V_{REF} Voltage Accuracy and Voltage Accuracy vs Load in <i>Electrical Characteristics</i> table.....	6
• Added additional fabrication process specification for V_{REG} Voltage Accuracy in <i>Electrical Characteristics</i> table.....	6
• Added additional fabrication process specification for V_{REG} Voltage Accuracy vs Power Supply in <i>Electrical Characteristics</i> table.....	6
• Added additional fabrication process specification for Quiescent Current in <i>Electrical Characteristics</i> table....	6
• Added all chip site origin (CSO) to typical test conditions in <i>Typical Characteristics</i>	8
• Updated Quiescent Current vs Temperature, Reference Voltage vs Temperature, Overscale Current vs Temperature, and VREG Voltage vs VREG Current to align with absolute maximum temperature rating in <i>Typical Characteristics</i>	8
• Added additional fabrication process curve for Quiescent Current vs Temperature in <i>Typical Characteristics</i> section.....	8
• Added <i>Device Functional Modes</i> section.....	10
• Added Power Supply Recommendations and Layout section.....	15
• Added part number fabrication process information table in <i>Device Support</i>	16

Changes from Revision A (November 2003) to Revision B (March 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added <i>Pin Functions</i> , <i>ESD Ratings</i> , <i>Thermal Information</i> , <i>Recommended Operating Conditions</i> , and <i>Electrical Characteristics</i> tables, and <i>Detailed Description</i> , <i>Overview</i> , <i>Functional Block Diagram</i> , <i>Feature Description</i> , <i>Application and Implementation</i> , <i>Device and Documentation Support</i> , and <i>Mechanical, Packaging, and Orderable Information</i> sections.....	1
• Added <i>Pin Functions</i> table.....	4
• Changed "Operating temperature" absolute minimum from "–55°C" to "–40°C" and moved temperature specifications to <i>Absolute Maximum Ratings</i> table.....	5
• Changed "Span error" specification test condition from " $I_{IN} = 250 \mu A$ to 25 mA", to " $I_{OUT} = 250 \mu A$ to 25 mA", in <i>Electrical Characteristics</i>	6
• Changed V_{REF} "Voltage accuracy vs load" typical specification from ± 100 ppm/mA to ± 200 ppm/mA in <i>Electrical Characteristics</i>	6
• Changed <i>Basic Circuit Connections</i> application diagram.....	11
• Changed <i>External Transistor</i> applications information section to incorporate additional guidance regarding transistor power dissipation and thermal concerns.....	12
• Added <i>Circuit Stability</i> application information section.....	14

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XTR115U	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	XTR 115U
XTR115U/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	XTR 115U
XTR115U/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	XTR 115U
XTR115UA/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 115U A
XTR115UA/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 115U A
XTR116U	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	XTR 116U
XTR116U/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	XTR 116U
XTR116U/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 85	XTR 116U
XTR116UA	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	XTR 116U A
XTR116UA/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 116U A
XTR116UA/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 116U A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR115U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR115UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR116U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR116UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

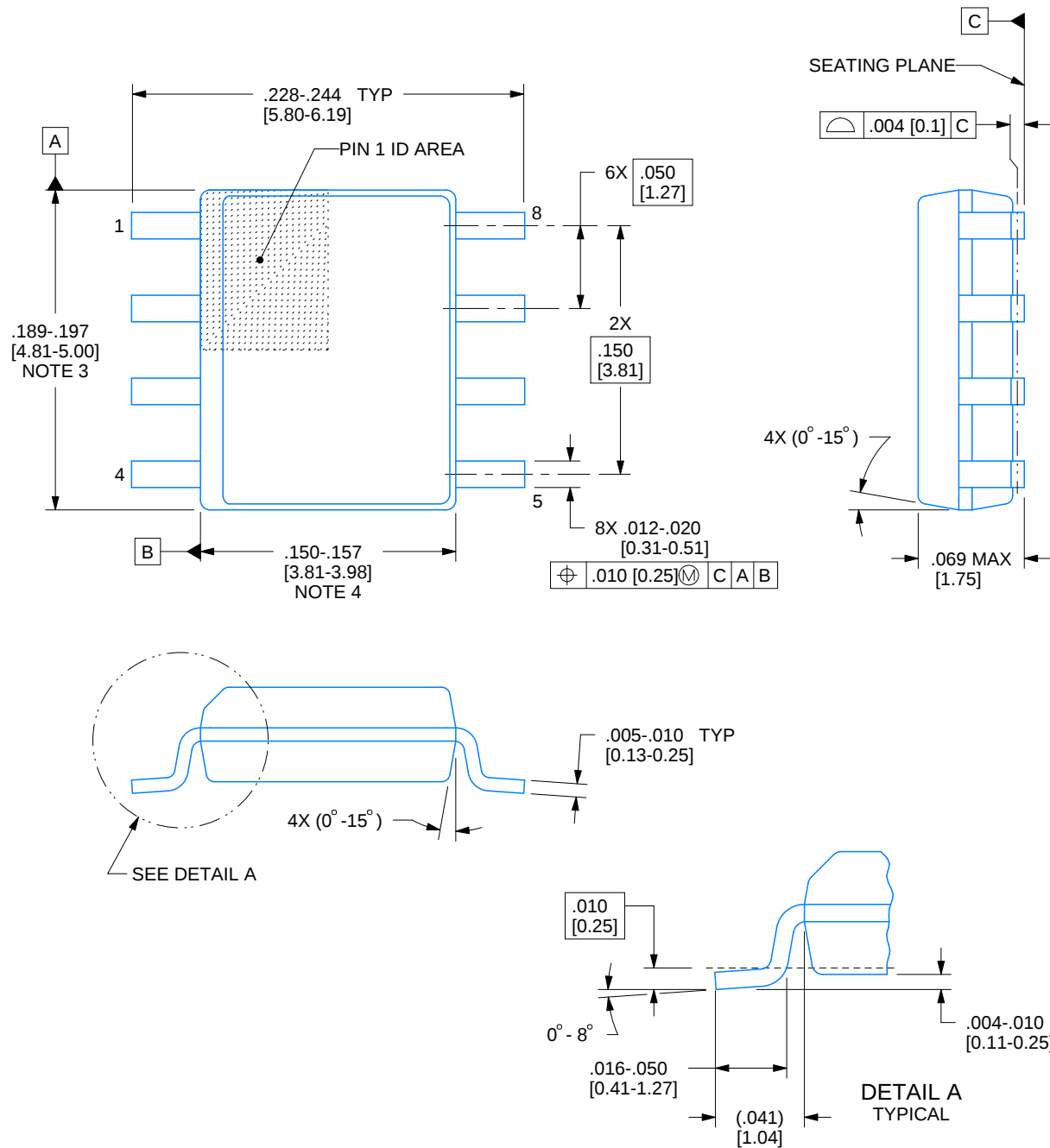
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR115U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
XTR115UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
XTR116U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
XTR116UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

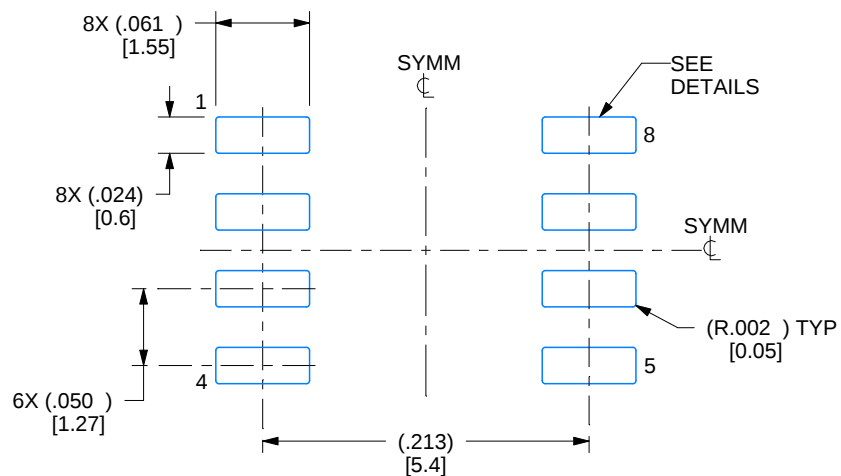
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

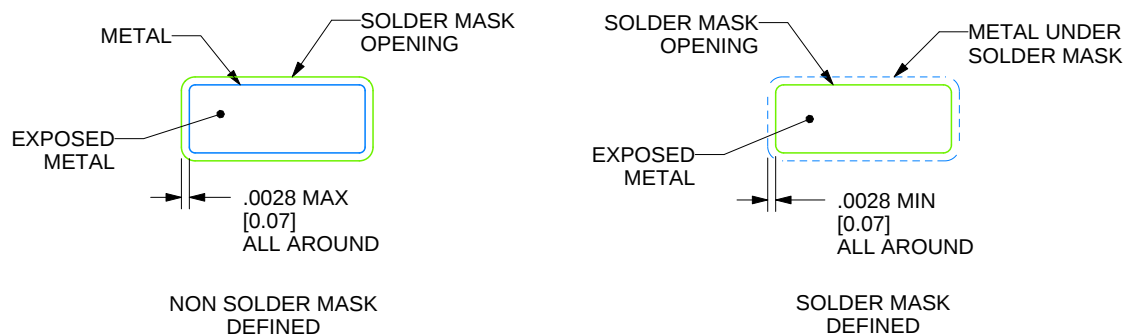
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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