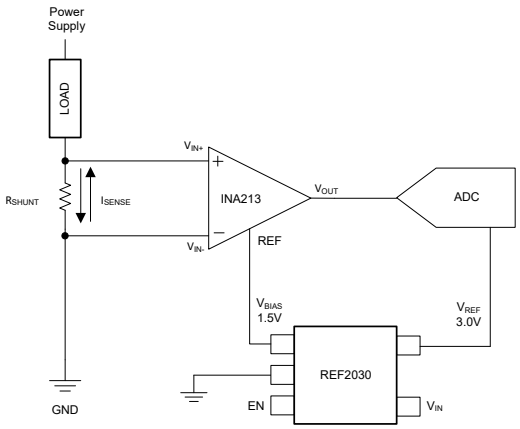
REF20xx Low-Drift, Low-Power, Dual-Output, V_{REF} and V_{REF} / 2 Voltage References

1 Features

- Two outputs, V_{REF} and V_{REF} / 2, for convenient use in single-supply systems
- Excellent temperature drift performance:
  - 8ppm/°C (maximum) from –40°C to 125°C
- High initial accuracy: ±0.05% (maximum)
- V_{REF} and V_{BIAS} tracking overtemperature:
  - 6ppm/°C (maximum) from –40°C to 85°C
  - 7ppm/°C (maximum) from –40°C to 125°C
- Microsize package: SOT23-5
- Low dropout voltage: 10mV
- High output current: ±20mA
- Low quiescent current: 360µA
- Line regulation: 3ppm/V
- Load regulation: 8ppm/mA
- Matte-Sn version (REF2025AISDDCR) for improved corrosion resistance in the Battelle Class III and similar harsh environments

2 Applications

- Electricity meter
- Analog input module
- Analog output module
- Servo drive control module
- Circuit breaker (ACB, MCCB, VCB)
- Clinical digital thermometer
- Lab and field instrumentation
- Battery test



Application Example

3 Description

Applications with only a positive supply voltage often require additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The REF20xx provides a reference voltage (V_{REF}) for the ADC and a second highly-accurate voltage (V_{BIAS}) that can be used to bias the input bipolar signals.

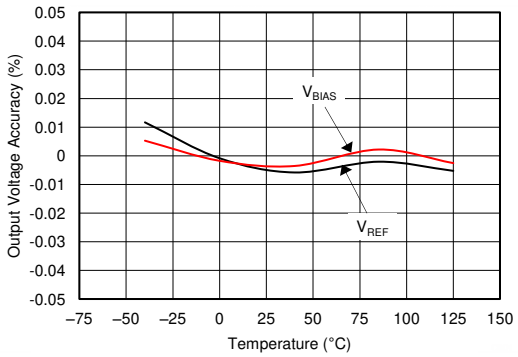
The REF20xx offers excellent temperature drift (8ppm/°C, maximum) and initial accuracy (0.05%) on both the V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430µA. In addition, the V_{REF} and V_{BIAS} outputs track each other with a precision of 6ppm/°C (maximum) across the temperature range of –40°C to 125°C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete solution. Extremely low dropout voltage of only 10mV allows operation from very low input voltages, which can be very useful in battery-operated systems.

Both the V_{REF} and V_{BIAS} voltages have the same excellent specifications and can sink and source current equally well. Very good long-term stability and low noise levels make these devices ideally-designed for high-precision industrial applications.

Package Information

PART NAME	PACKAGE (1)	PACKAGE SIZE(2)
REF20xx	DCC (SOT-23, 5)	2.90mm × 1.60mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



V_{REF} and V_{BIAS} versus Temperature

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4 Device Comparison Table

PRODUCT	V_{REF}	V_{BIAS}
REF2025	2.5V	1.25V
REF2030	3.0V	1.5V
REF2033	3.3V	1.65V
REF2041	4.096V	2.048V

5 Pin Configuration and Functions

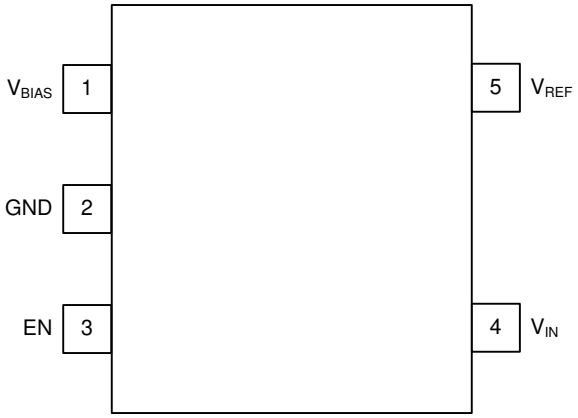


Figure 5-1. DDC Package SOT23-5 (Top View)

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{BIAS}	Output	Bias voltage output (V_{REF} / 2)
2	GND	—	Ground
3	EN	Input	Enable (EN ≥ V_{IN} – 0.7V, device enabled)
4	V_{IN}	Input	Input supply voltage
5	V_{REF}	Output	Reference voltage output (V_{REF})

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	6	V
	EN	–0.3	V_{IN} + 0.3	
Temperature	Operating	–55	150	°C
	Junction, T_j		150	
	Storage, T_{stg}	–65	170	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage range (I_L = 0mA, T_A = 25°C)	V_{REF} + 0.02(1)		5.5	V

(1) See Figure 6-28 in Section 6.6 for minimum input voltage at different load currents and temperature

6.4 Thermal Information

THERMAL METRIC(1)		REF20xx DDC (SOT23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

At T_A = 25°C, I_L = 0mA, and V_{IN} = 5V, unless otherwise noted. Both V_{REF} and V_{BIAS} have the same specifications.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT								
	Output voltage accuracy				–0.05%		0.05%	
	Output voltage temperature coefficient(1)		–40°C ≤ T_A ≤ 125°C			±3	±8	ppm/°C
	V_{REF} and V_{BIAS} tracking over temperature(2)		–40°C ≤ T_A ≤ 85°C			±1.5	±6	ppm/°C
			–40°C ≤ T_A ≤ 125°C			±2	±7	
LINE AND LOAD REGULATION								
$\Delta V_{O(\Delta VI)}$	Line regulation		V_{REF} + 0.02V ≤ V_{IN} ≤ 5.5V			3	35	ppm/V
$\Delta V_{O(\Delta IL)}$	Load regulation	Sourcing	0mA ≤ I_L ≤ 20mA, V_{REF} + 0.6V ≤ V_{IN} ≤ 5.5V			8	20	ppm/mA
		Sinking	0mA ≤ I_L ≤ –20mA, V_{REF} + 0.02V ≤ V_{IN} ≤ 5.5V			8	20	
POWER SUPPLY								
I_{CC}	Supply current	Active mode				360	430	µA
			–40°C ≤ T_A ≤ 125°C				460	
		Shutdown mode				3.3	5	
			–40°C ≤ T_A ≤ 125°C				9	
	Enable voltage		Device in shutdown mode (EN = 0)		0		0.7	V
			Device in active mode (EN = 1)		V_{IN} – 0.7		V_{IN}	
	Dropout voltage					10	20	mV
			I_L = 20mA				600	
I_{SC}	Short-circuit current					50		mA
t_{on}	Turn-on time		0.1% settling, C_L = 1µF			500		µs
NOISE								
	Low-frequency noise(3)		0.1Hz ≤ f ≤ 10Hz			12		ppm_{PP}
	Output voltage noise density		f = 100Hz			0.25		$ppm/\sqrt{Hz}$
CAPACITIVE LOAD								
	Stable output capacitor range				0		10	µF
HYSTERESIS AND LONG TERM STABILITY								
	Long-term stability[4]		0 to 1000 hours			25		ppm
	Output voltage hysteresis[5]		25°C, –40°C, 125°C, 25°C	Cycle 1		60		ppm
				Cycle 2		35		

(1) Temperature drift is specified according to the box method. See Section 8.3 for more details.
(2) The V_{REF} and V_{BIAS} tracking over temperature specification is explained in more detail in Section 8.3.
(3) The peak-to-peak noise measurement procedure is explained in more detail in Section 7.4.
(4) Long-term stability measurement procedure is explained in more in detail in Section 7.2.
(5) The thermal hysteresis measurement procedure is explained in more detail in Section 7.3.

6.6 Typical Characteristics

At T_A = 25°C, I_L = 0mA, V_{IN} = 5V power supply, C_L = 0µF, and 2.5V output, unless otherwise noted.

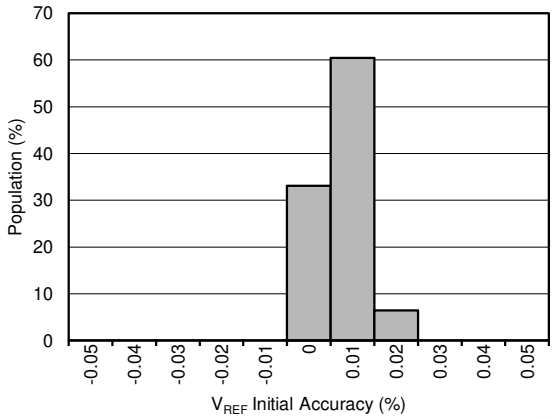
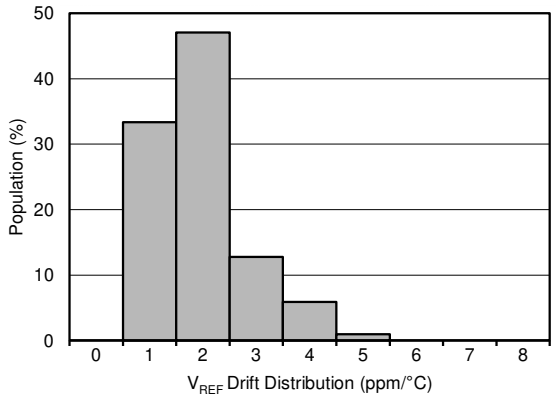


Figure 6-1. Initial Accuracy Distribution (V_{REF})



–40°C ≤ T_A ≤ 125°C

Figure 6-2. Drift Distribution (V_{REF})

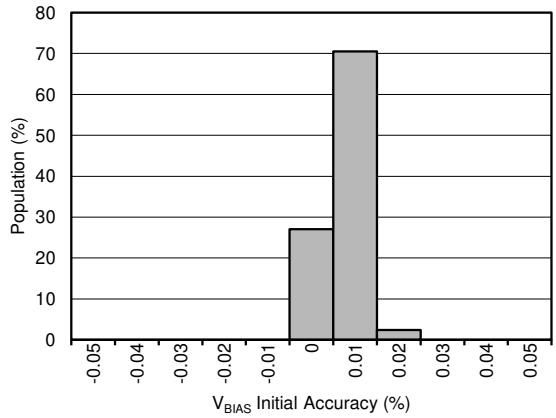
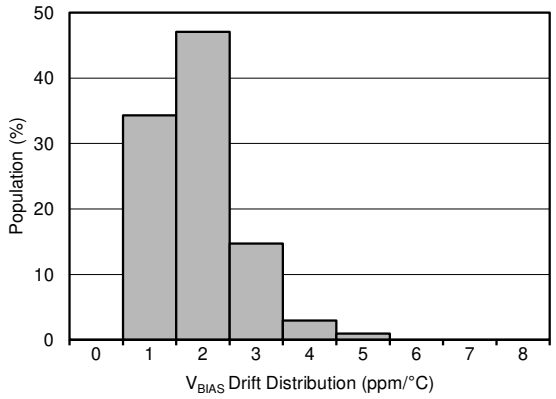


Figure 6-3. Initial Accuracy Distribution (V_{BIAS})



–40°C ≤ T_A ≤ 125°C

Figure 6-4. Drift Distribution (V_{BIAS})

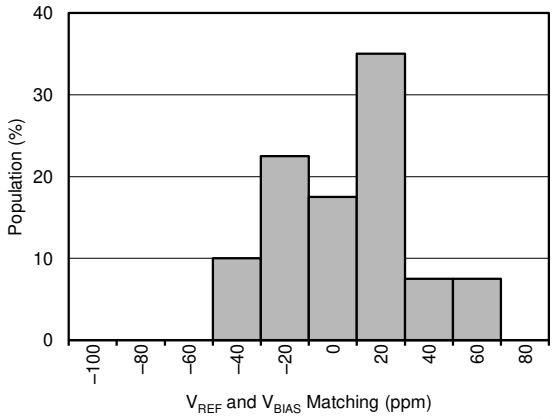
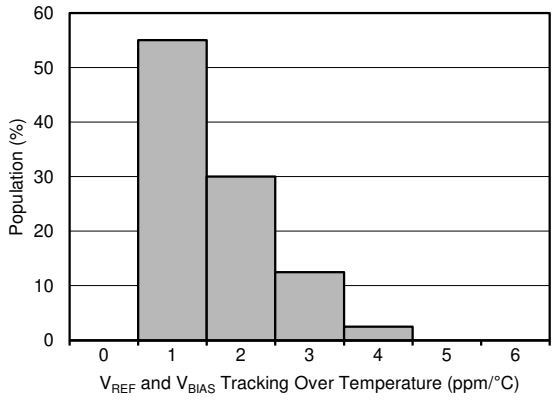


Figure 6-5. V_{REF} – 2 × V_{BIAS} Distribution

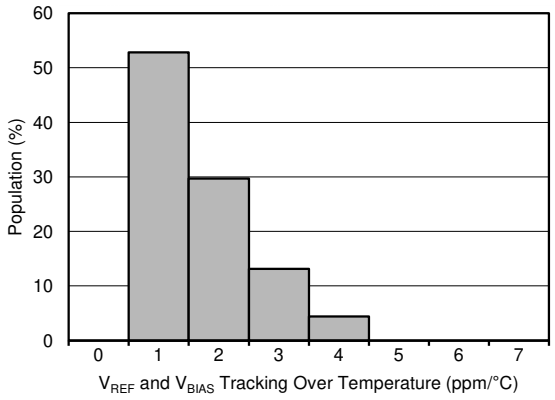


–40°C ≤ T_A ≤ 85°C

Figure 6-6. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature

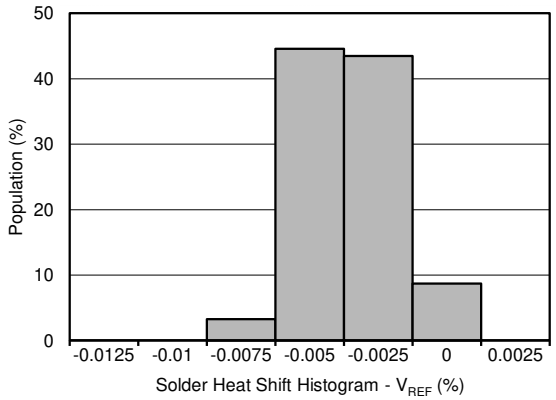
6.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0mA, V_{IN} = 5V power supply, C_L = 0µF, and 2.5V output, unless otherwise noted.



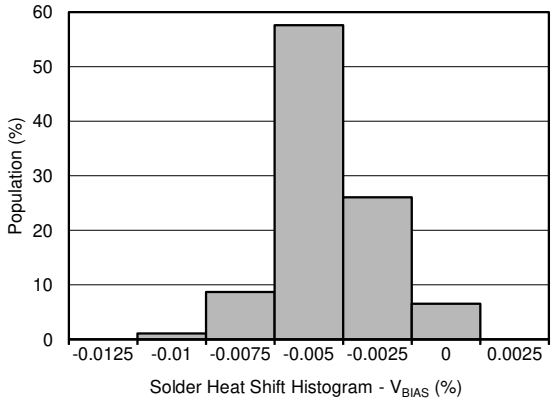
–40°C ≤ T_A ≤ 125°C

Figure 6-7. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature



Refer to the *Section 7.1* section for more information.

Figure 6-8. Solder Heat Shift Distribution (V_{REF})



Refer to the *Section 7.1* section for more information.

Figure 6-9. Solder Heat Shift Distribution (V_{BIAS})

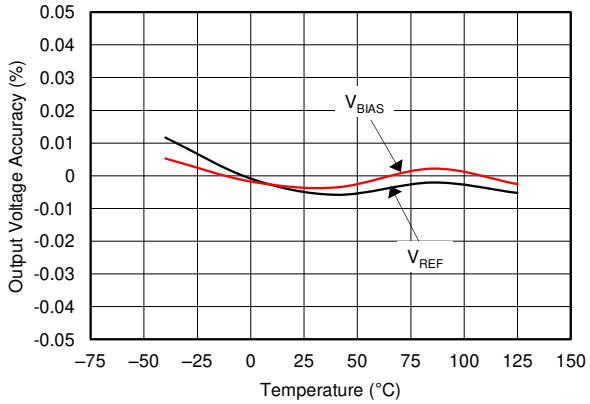


Figure 6-10. Output Voltage Accuracy (V_{REF}) vs Temperature

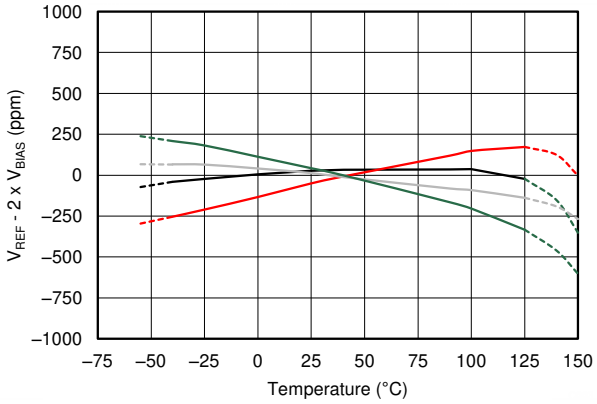
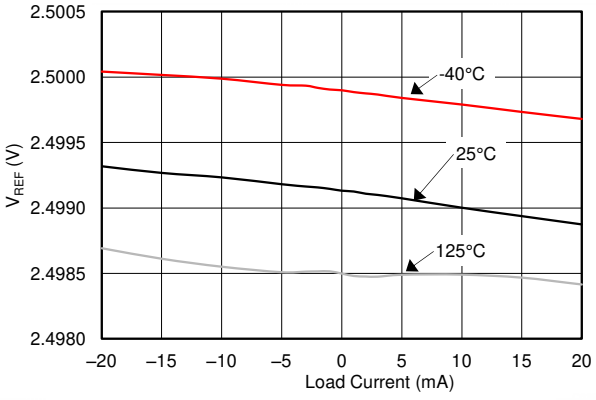


Figure 6-11. V_{REF} – 2 × V_{BIAS} Tracking vs Temperature



V_{REF} output

Figure 6-12. Output Voltage Change vs Load Current (V_{REF})

6.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0mA, V_{IN} = 5V power supply, C_L = 0µF, and 2.5V output, unless otherwise noted.

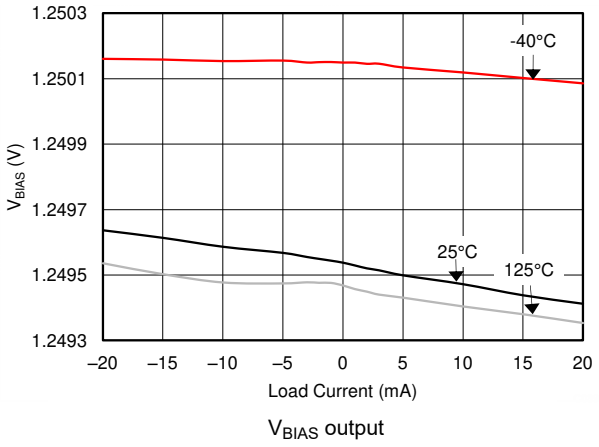


Figure 6-13. Output Voltage Change vs Load Current (V_{BIAS})

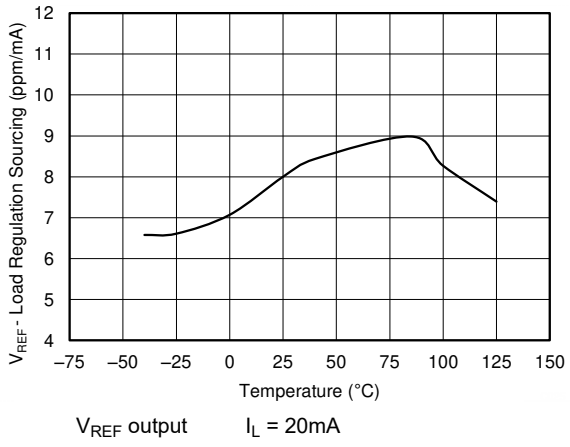


Figure 6-14. Load Regulation Sourcing vs Temperature (V_{REF})

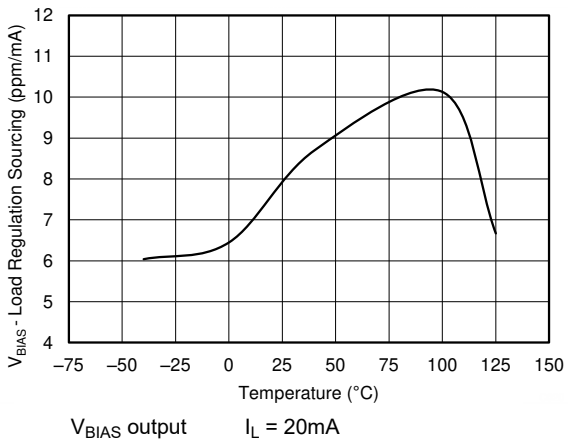


Figure 6-15. Load Regulation Sourcing vs Temperature (V_{BIAS})

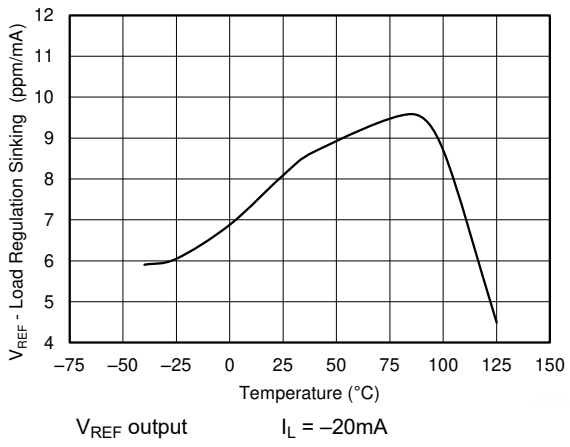


Figure 6-16. Load Regulation Sinking vs Temperature (V_{REF})

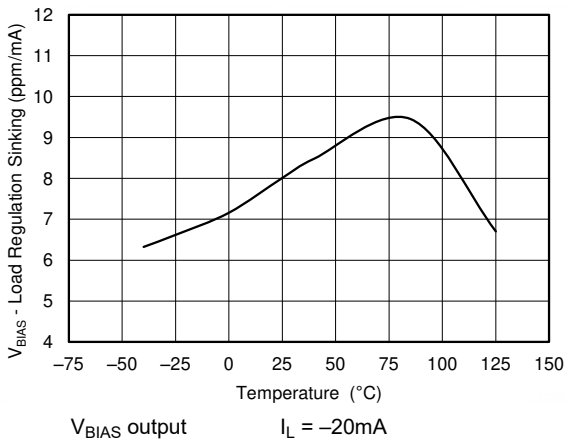


Figure 6-17. Load Regulation Sinking vs Temperature (V_{BIAS})

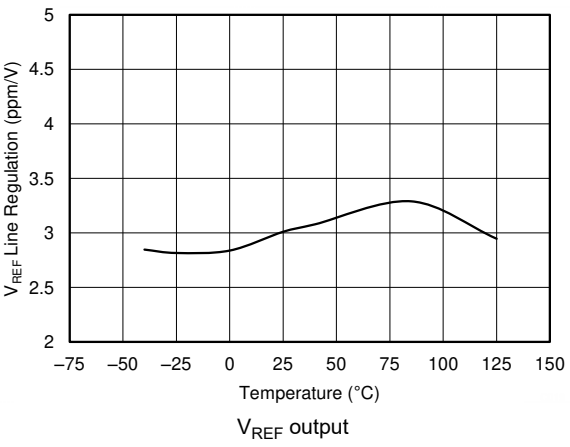
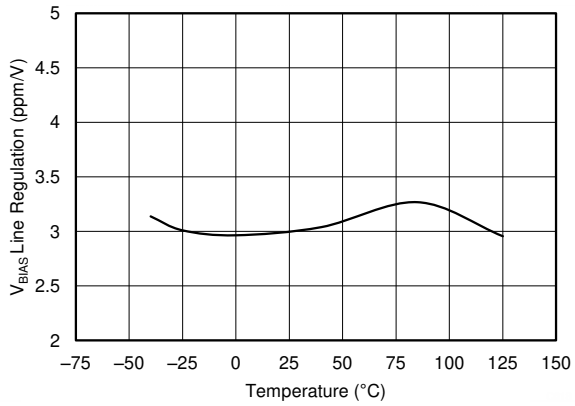


Figure 6-18. Line Regulation vs Temperature (V_{REF})

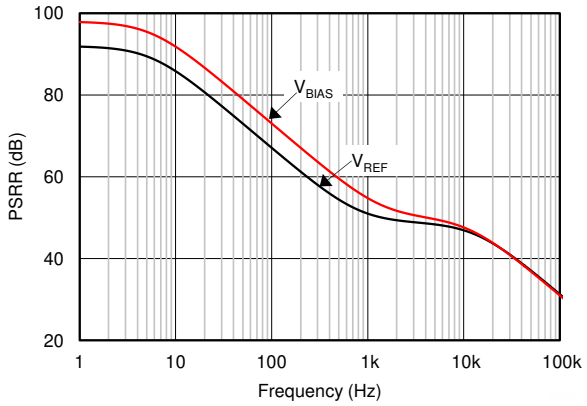
6.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0mA, V_{IN} = 5V power supply, C_L = 0µF, and 2.5V output, unless otherwise noted.



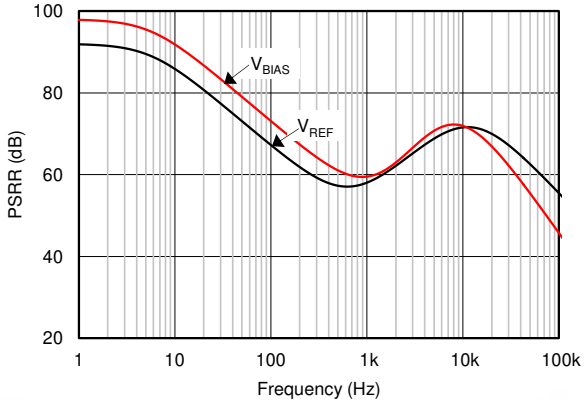
V_{BIAS} output

Figure 6-19. Line Regulation vs Temperature (V_{BIAS})



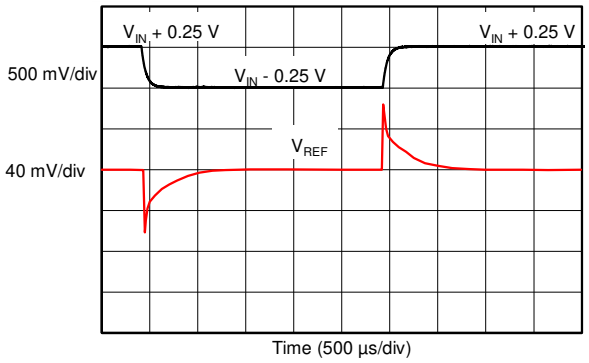
C_L = 0µF

Figure 6-20. Power-Supply Rejection Ratio vs Frequency



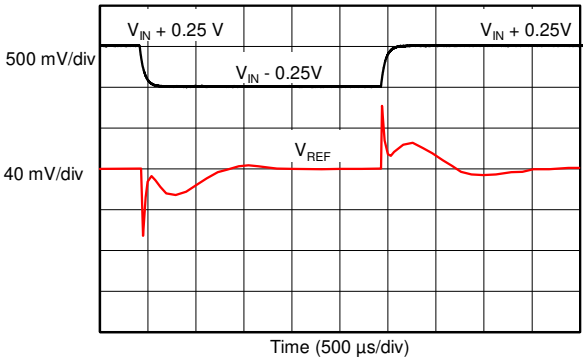
C_L = 10µF

Figure 6-21. Power-Supply Rejection Ratio vs Frequency



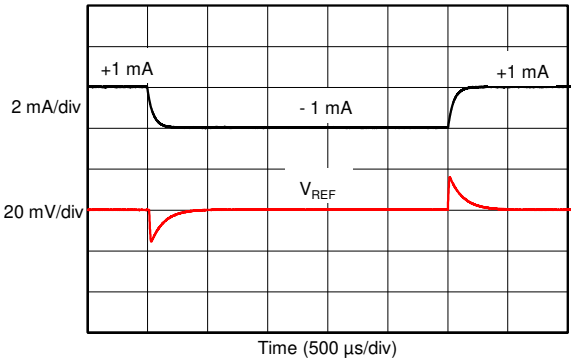
C_L = 1µF

Figure 6-22. Line Transient Response



C_L = 10µF

Figure 6-23. Line Transient Response

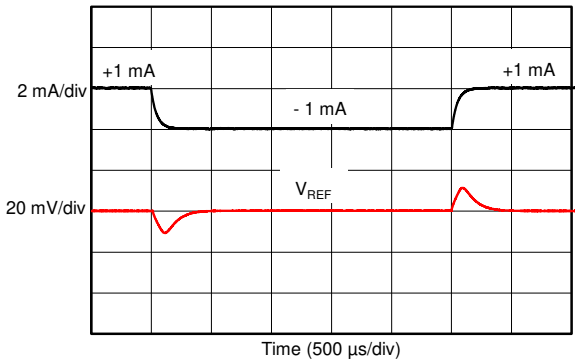


C_L = 1µF I_L = ±1mA step

Figure 6-24. Load Transient Response

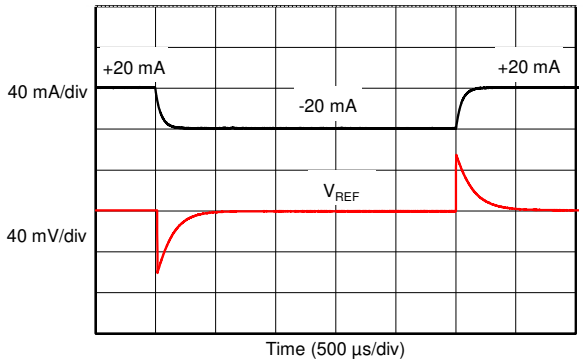
6.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0mA, V_{IN} = 5V power supply, C_L = 0µF, and 2.5V output, unless otherwise noted.



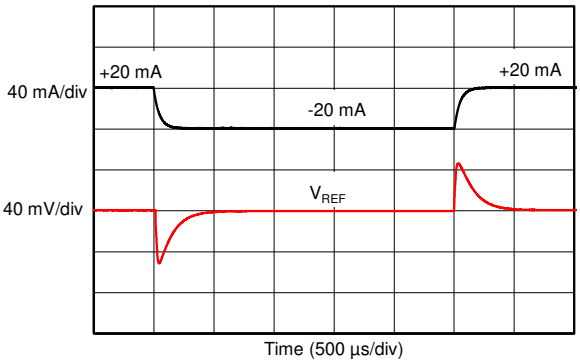
C_L = 10µF I_L = ±1mA step

Figure 6-25. Load Transient Response



C_L = 1µF I_L = ±20mA step

Figure 6-26. Load Transient Response



C_L = 10µF I_L = ±20mA step

Figure 6-27. Load Transient Response

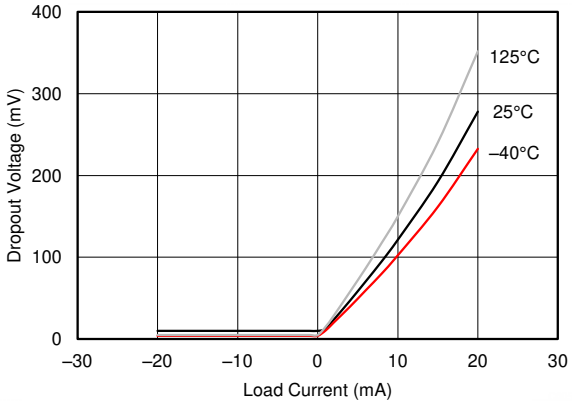
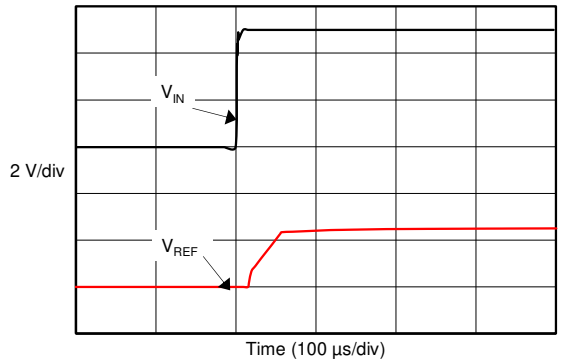
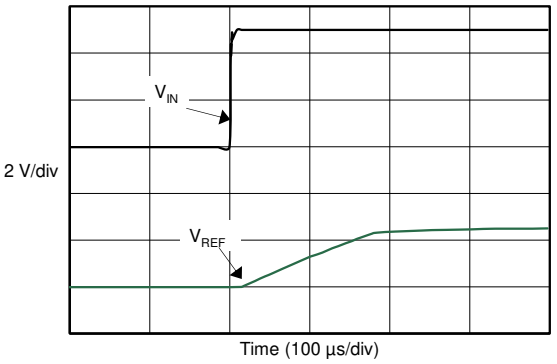


Figure 6-28. Minimum Dropout Voltage vs Load Current



C_L = 1µF

Figure 6-29. Turn-On Settling Time



C_L = 10µF

Figure 6-30. Turn-On Settling Time

6.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0mA, V_{IN} = 5V power supply, C_L = 0µF, and 2.5V output, unless otherwise noted.

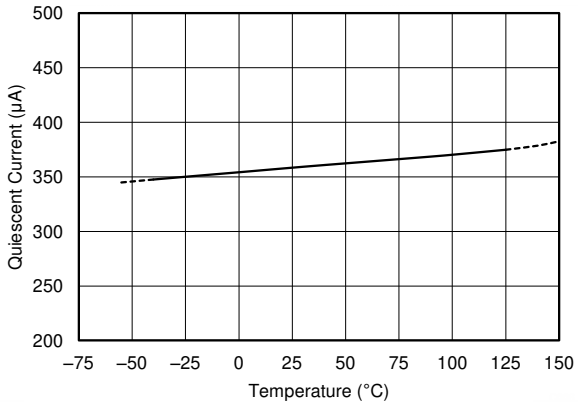


Figure 6-31. Quiescent Current vs Temperature

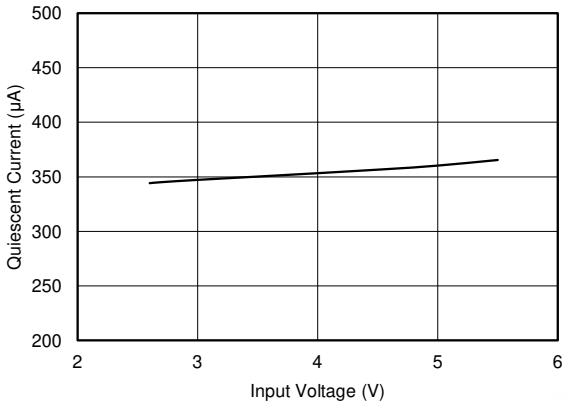
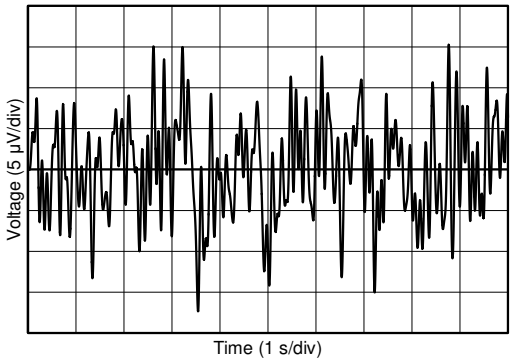
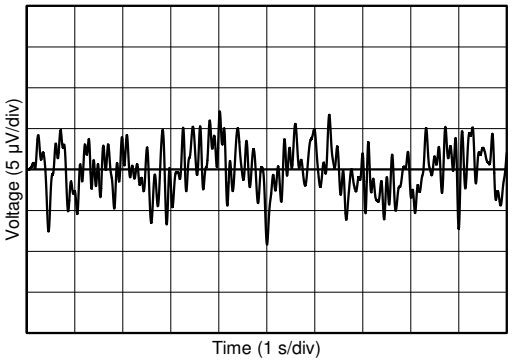


Figure 6-32. Quiescent Current vs Input Voltage



V_{REF} output

Figure 6-33. 0.1Hz to 10Hz Noise (V_{REF})



V_{BIAS} output

Figure 6-34. 0.1Hz to 10Hz Noise (V_{BIAS})

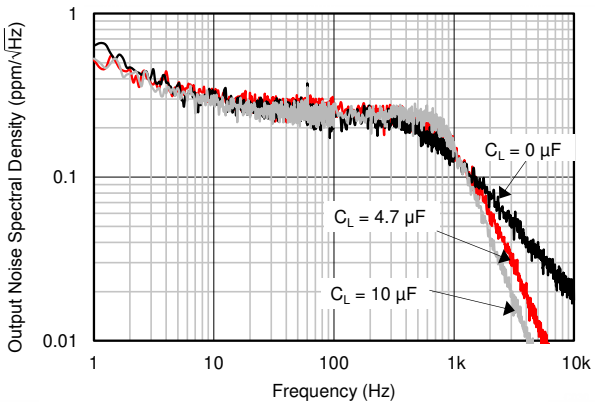
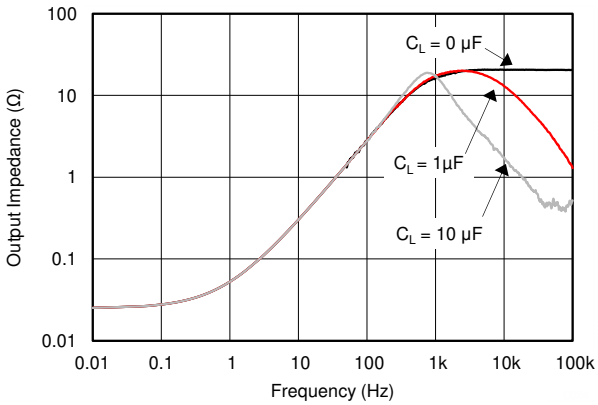


Figure 6-35. Output Voltage Noise Spectrum



V_{REF} output

Figure 6-36. Output Impedance vs Frequency (V_{REF})

6.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0mA, V_{IN} = 5V power supply, C_L = 0µF, and 2.5V output, unless otherwise noted.

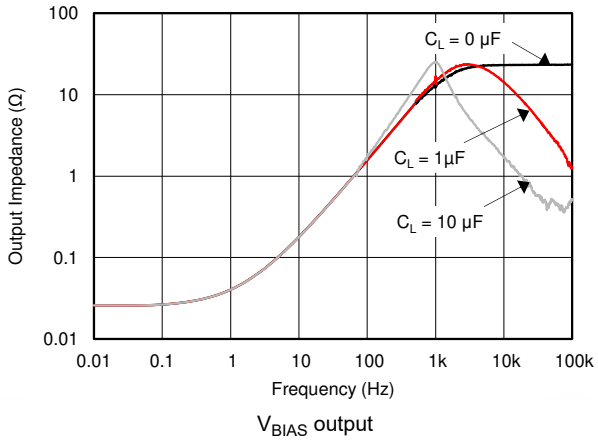


Figure 6-37. Output Impedance vs Frequency (V_{BIAS})

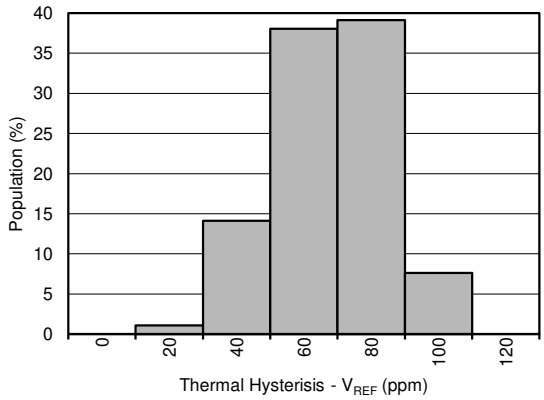


Figure 6-38. Thermal Hysteresis Distribution (V_{REF})

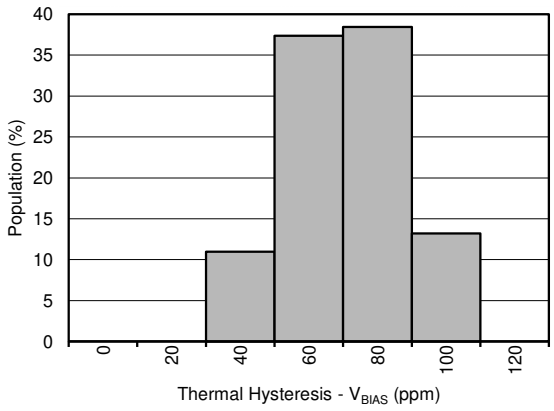


Figure 6-39. Thermal Hysteresis Distribution (V_{BIAS})

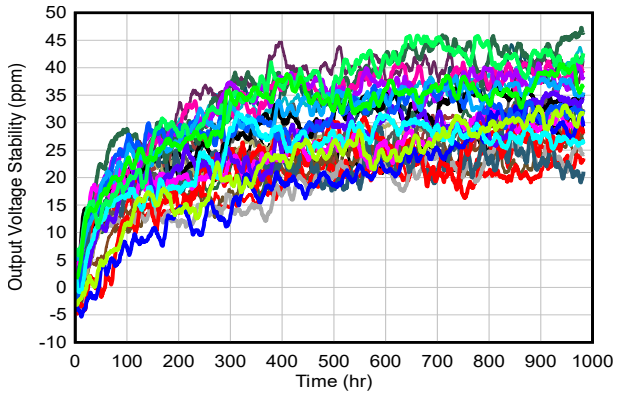


Figure 6-40. Long-Term Stability (First 1000 hours)

7 Parameter Measurement Information

7.1 Solder Heat Shift

The materials used in the manufacture of the REF20xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

To illustrate this effect, a total of 92 devices are soldered on four printed circuit boards [23 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 7-1. The printed circuit board is comprised of FR4 material. The board thickness is 1.57mm and the area is 171.54mm × 165.1mm.

The reference and bias output voltages are measured before and after the reflow process; the typical shift is displayed in Figure 7-2 and Figure 7-3. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the second pass to minimize its exposure to thermal stress.

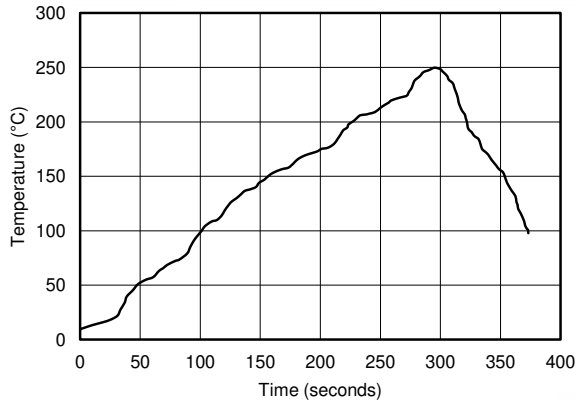


Figure 7-1. Reflow Profile

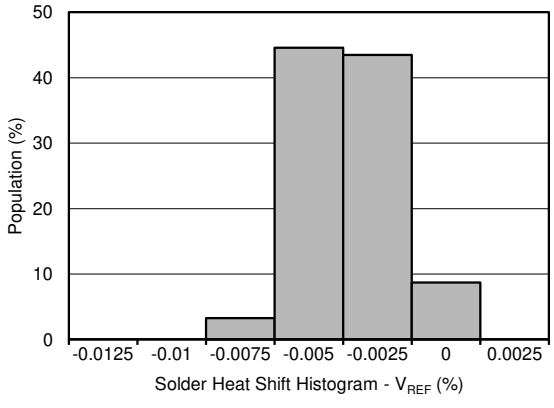


Figure 7-2. Solder Heat Shift Distribution, V_{REF} (%)

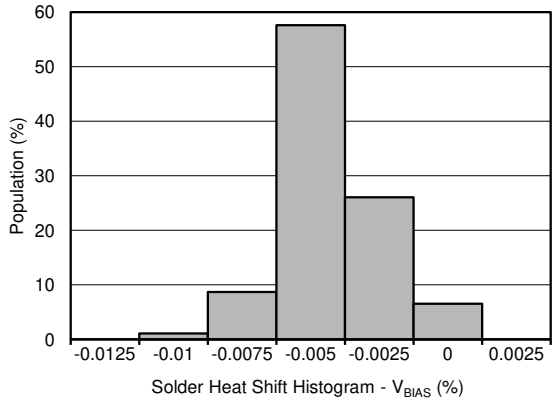


Figure 7-3. Solder Heat Shift Distribution, V_{BIAS} (%)

7.2 Long-Term Stability

The long term stability of the REF20xx is collected on 32 parts that are soldered onto Printed Circuit Boards without any slots or special layout considerations. The boards are then placed into an oven with air temperature maintained at T_A = 35°C. The V_{REF} output of the 32 parts is measured regularly. Typical long term stability is as shown in Figure 7-4.

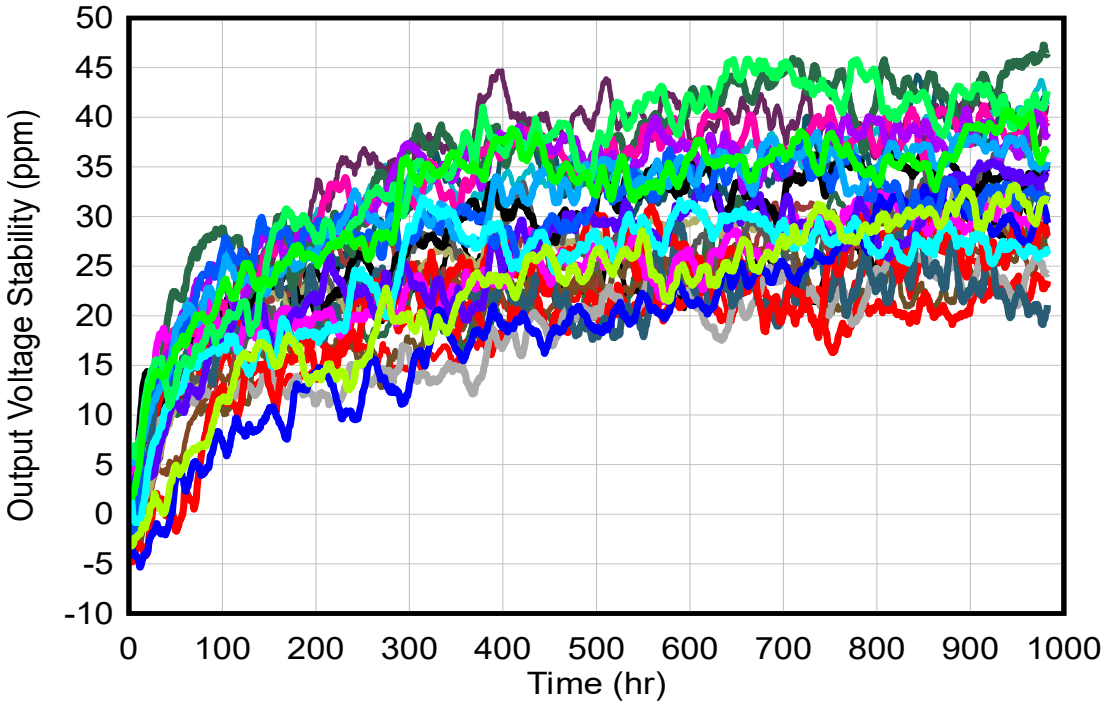


Figure 7-4. Long Term Stability – 1000 hours (V_{REF})

7.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF20xx soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis is calculated using Equation 1:

$$V_{HYST} = \left(\frac{|V_{PRE} - V_{POST}|}{V_{NOM}} \right) \times 10^6 (\text{ppm}) \quad (1)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device cycles from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C
- V_{NOM} = the specified output voltage

Figure 7-5 and Figure 7-6 show typical thermal hysteresis distribution.

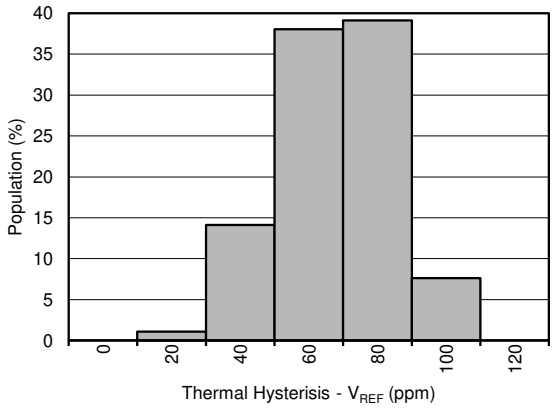


Figure 7-5. Thermal Hysteresis Distribution (V_{REF})

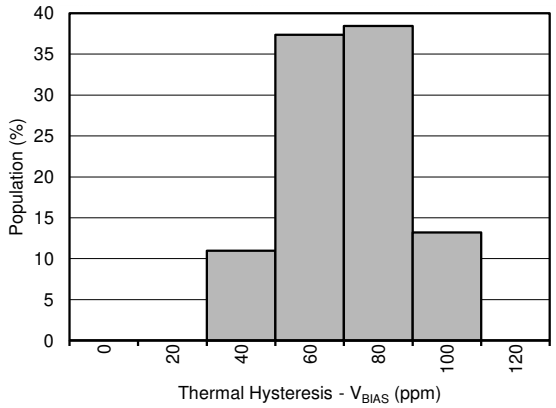


Figure 7-6. Thermal Hysteresis Distribution (V_{BIAS})

7.4 Noise Performance

Figure 7-7 and Figure 7-8 show typical 0.1Hz to 10Hz voltage noise. Device noise increases with output voltage and operating temperature. Use additional filtering to improve output noise levels. Verify that the output impedance does not degrade AC performance. Peak-to-peak noise measurement setup is shown in Figure 7-9.

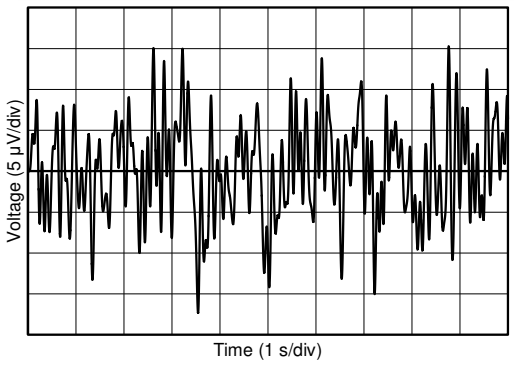


Figure 7-7. 0.1Hz to 10Hz Noise (V_{REF})

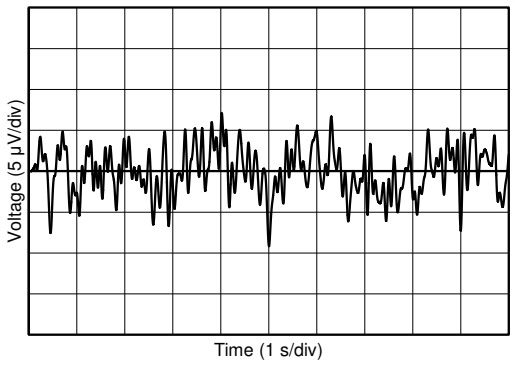


Figure 7-8. 0.1Hz to 10Hz Noise (V_{BIAS})

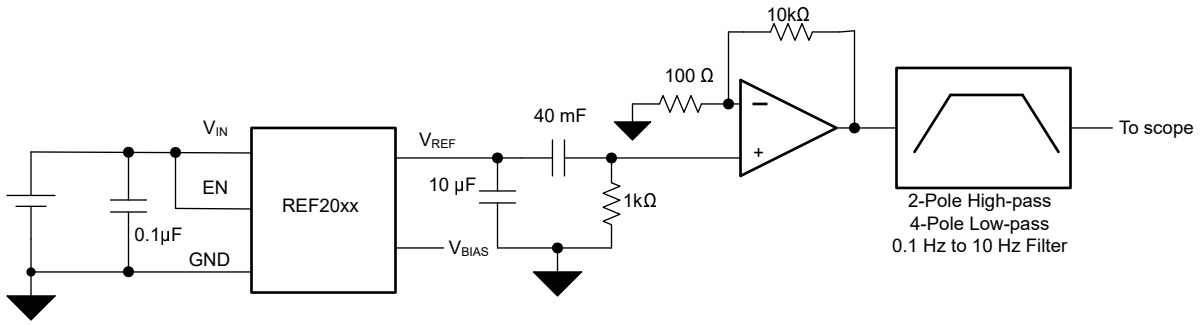


Figure 7-9. 0.1Hz to 10Hz Noise Measurement Setup

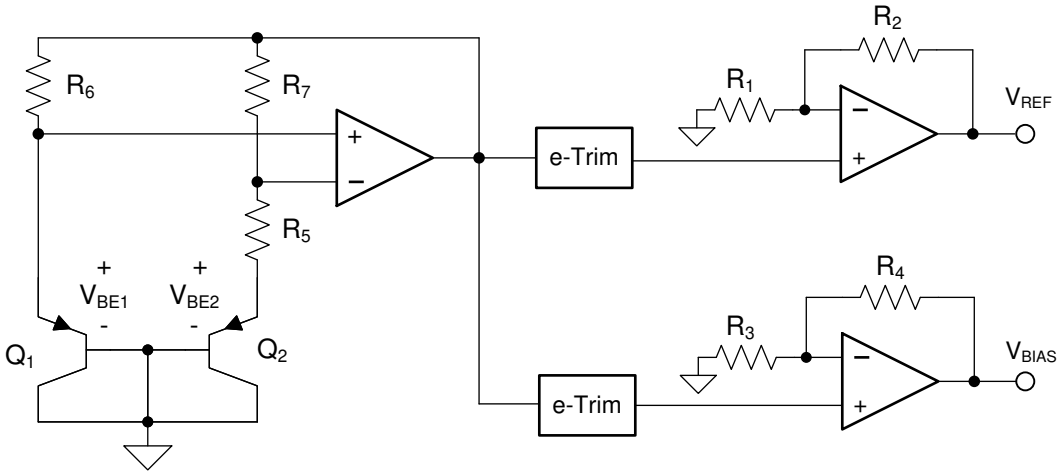
8 Detailed Description

8.1 Overview

The REF20xx are a family of dual-output, V_{REF} and V_{BIAS} (V_{REF} / 2) band-gap voltage references. Section 8.2 includes a block diagram of the basic band-gap topology and the two buffers used to derive the V_{REF} and V_{BIAS} outputs. Transistors Q_1 and Q_2 are biased so that the current density of Q_1 is greater than the current density of Q_2. The difference of the two base emitter voltages ($V_{BE1} – V_{BE2}$) has a positive temperature coefficient and is forced across resistor R_5. The voltage is amplified and added to the base emitter voltage of Q_2, which has a negative temperature coefficient. The resulting band-gap output voltage is almost independent of temperature. Two independent buffers are used to generate V_{REF} and V_{BIAS} from the band-gap voltage. The resistors R_1, R_2 and R_3, R_4 are sized such that $V_{BIAS} = V_{REF} / 2$.

e-Trim™ is a method of package-level trim for the initial accuracy and temperature coefficient of V_{REF} and V_{BIAS}, implemented during the final steps of manufacturing after the plastic molding process. The e-Trim method minimizes the influence of inherent transistor mismatch, as well as errors induced during package molding. e-Trim is implemented in the REF20xx to minimize the temperature drift and maximize the initial accuracy of both the V_{REF} and V_{BIAS} outputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 V_{REF} and V_{BIAS} Tracking

Most single-supply systems require an additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The V_{REF} and V_{BIAS} outputs of the REF20xx are generated from the same band-gap voltage as shown in Section 8.2. Hence, the outputs track each other across the full temperature range of –40°C to 125°C, with an accuracy of 7ppm/°C (maximum). The tracking accuracy increases to 6ppm/°C (maximum) when the temperature range is limited to –40°C to 85°C. The tracking error is calculated using the box method in Equation 2:

$$\text{Tracking Error} = \left(\frac{V_{DIFF[MAX]} - V_{DIFF[MIN]}}{V_{REF} \times \text{Temperature Range}}\right) \times 10^6 (\text{ppm}) \quad (2)$$

where

$$V_{DIFF} = V_{REF} - 2 \times V_{BIAS} \quad (3)$$

Figure 8-1 shows the tracking accuracy.

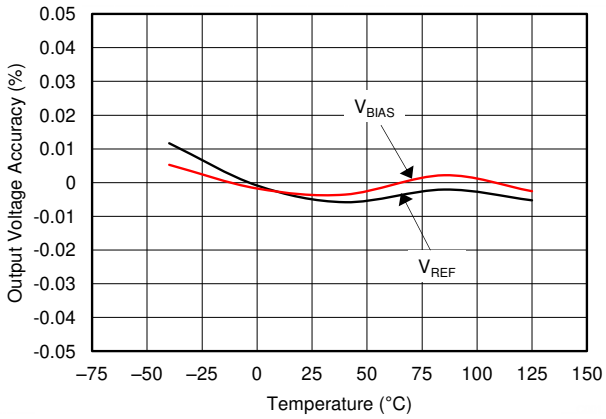


Figure 8-1. V_{REF} and V_{BIAS} Tracking versus Temperature

8.3.2 Low Temperature Drift

The REF20xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. Use Equation 4 to calculate the drift using the box method:

$$\text{Drift} = \left(\frac{V_{REF[MAX]} - V_{REF[MIN]}}{V_{REF} \times \text{Temperature Range}} \right) \times 10^6 (\text{ppm}) \quad (4)$$

8.3.3 Load Current

The REF20xx family is specified to deliver a current load of ±20mA per output. Both the V_{REF} and V_{BIAS} outputs of the device are protected from short circuits by limiting the output short-circuit current to 50mA. The device temperature increases according to Equation 5:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (5)$$

where

- T_J is junction temperature (°C)
- T_A is ambient temperature (°C)
- P_D is power dissipated (W)
- $R_{\theta JA}$ is junction-to-ambient thermal resistance (°C/W)

Verify that the REF20xx maximum junction temperature does not exceed the absolute maximum rating of 150°C.

8.4 Device Functional Modes

When the EN pin of the REF20xx is pulled high, the device is in active mode. The device is in active mode during normal operation. Place the REF20xx in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 5µA. See Section 6.5 for logic high and logic low voltage levels.

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The solution in the section accurately detect load currents from –2.5A to 2.5A and are:

- Low-drift
- Bidirectional
- Single-supply
- Low-side
- Current-sensing

The linear range of the output is from 250mV to 2.75V. Positive current is represented by output voltages from 1.5V to 2.75V. Negative current is represented by output voltages from 250mV to 1.5V. The difference amplifier is the INA213 current-shunt monitor, with the supply and reference voltages supplied by the low-drift REF2030.

Industrial applications with electronics in corrosive environments are susceptible to corrosive damage due to the exposure to heat, moisture, and corrosive gases. The combination of the following conditions in a given system lead to higher risk of corrosive damage:

1. Ventilated enclosures exposing underlying PCB.
2. PCBs not conformally coated.
3. Exposed-lead components with plating susceptible to corrosion.
4. Changes in plating techniques for RoHS compliance (for example, removal of Pb (lead) and certain types of plating).

To improve resistance to corrosion in harsh environments, the REF2025AISDDCR uses Matte-Sn plating with improved assembly process to reduce exposed Cu (copper), leading to improved corrosion resistance in Battelle Class III and similar harsh environments. The *S* in the part number identifies the special plating option. REF2025 versions that do not have the *S* continue to be available in industry standard NiPdAu processing technique.

9.2 Typical Application

9.2.1 Low-Side, Current-Sensing Application

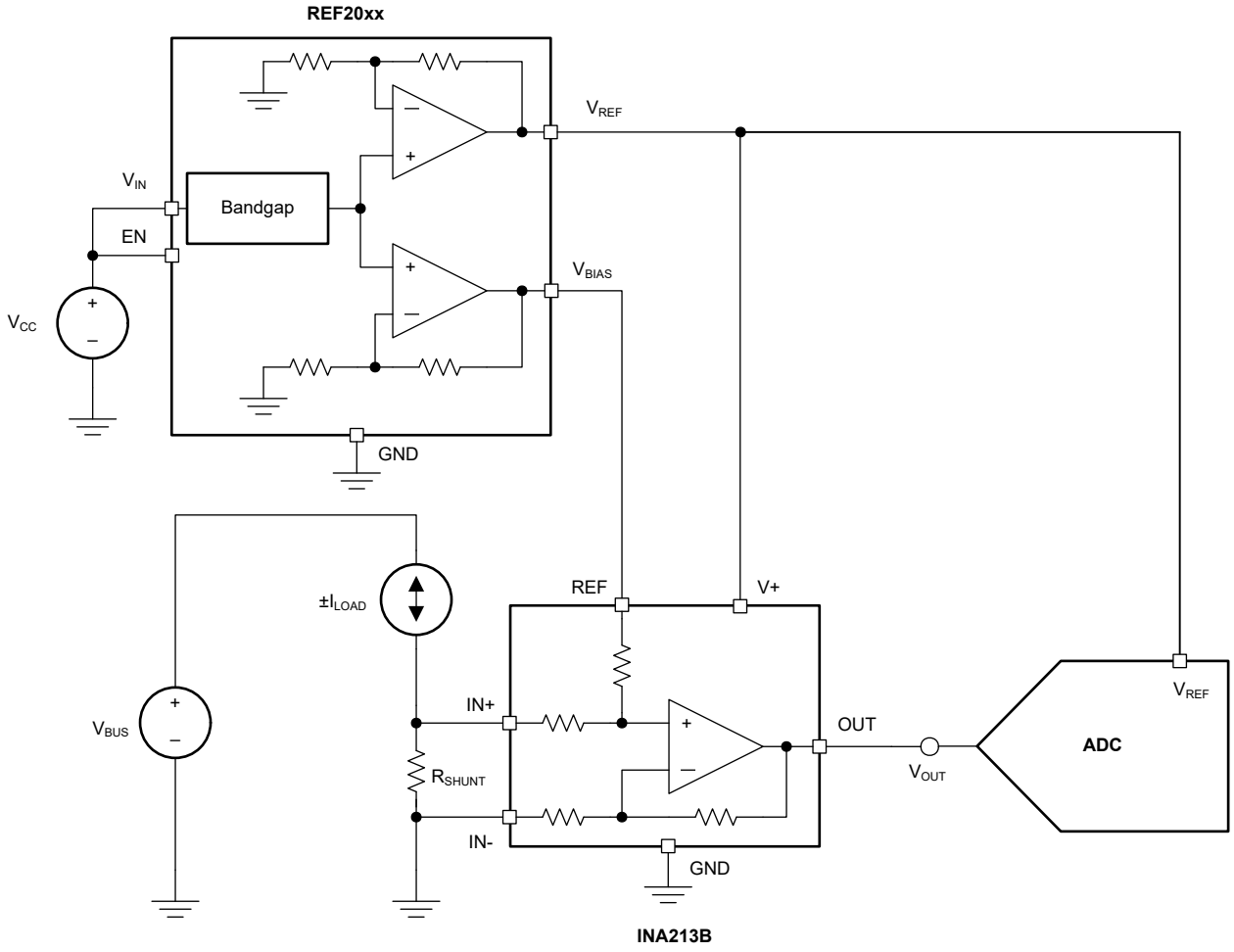


Figure 9-1. Low-Side, Current-Sensing Application

9.2.1.1 Design Requirements

The design requirements are as follows:

1. Supply voltage: 5.0V
2. Load current: ±2.5A
3. Output: 250mV to 2.75V
4. Maximum shunt voltage: ±25mV

9.2.1.2 Detailed Design Procedure

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore, the current-sensing solution is independent of the bus voltage, V_{BUS}. When sensing bidirectional currents, use a differential amplifier with a reference pin. This procedure allows for the differentiation between positive and negative currents by biasing the output stage to respond to negative input voltages. There are a variety of methods for supplying power (V+) and the reference voltage (V_{REF}, or V_{BIAS}) to the differential amplifier. For a low-drift solution, use a monolithic reference that supplies both power and the reference voltage. Figure 9-2 shows the general circuit topology for a low-drift, low-side, bidirectional, and current-sensing solution. This general circuit topology is particularly useful when interfacing with an ADC; see Figure 9-1. V_{REF} and V_{BIAS} track over temperature with better matching than alternate topologies. For a more detailed version of the design procedure, refer to the *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing* reference design.

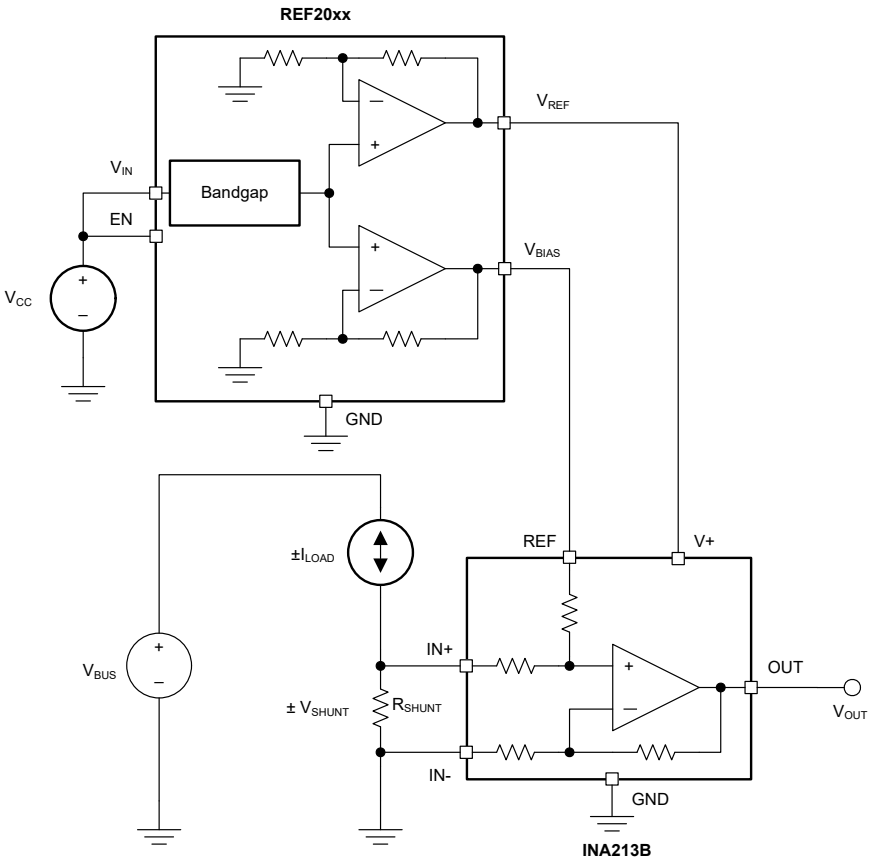


Figure 9-2. Low-Drift, Low-side, Bidirectional, Current-Sensing Circuit Topology

The transfer function for the circuit given in Figure 9-2 is as shown in Equation 6:

$$V_{OUT} = G \times (\pm V_{SHUNT}) + V_{BIAS} = G \times (\pm I_{LOAD} \times R_{SHUNT}) + V_{BIAS} \quad (6)$$

9.2.1.2.1 Shunt Resistor

Figure 9-2 shows the value of V_{SHUNT} as the ground potential for the system load. If the value of V_{SHUNT} is too large, issues can arise when interfacing with systems with a ground potential of 0V. A value of V_{SHUNT} that is too negative can violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore, limiting the voltage across the shunt resistor is important. Use Equation 7 to calculate the maximum value of R_{SHUNT}.

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} \quad (7)$$

Given that the maximum shunt voltage is ±25mV and the load current range is ±2.5A, use Equation 8 to calculate the maximum shunt resistance.

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} = \frac{25mV}{2.5A} = 10m\Omega \quad (8)$$

To minimize errors over temperature, select a low-drift shunt resistor. To minimize offset error, select a shunt resistor with the lowest tolerance. For this design, the Y14870R01000B9W resistor is used.

9.2.1.2.2 Differential Amplifier

Confirm that the differential amplifier used for this design includes the following features:

1. Single-supply (3V)
2. Reference voltage input
3. Low initial input offset voltage (V_{OS})
4. Low-drift
5. Fixed gain
6. Low-side sensing (input common-mode range below ground)

For this design, a current-shunt monitor (INA213) is used. Figure 9-3 shows the INA21x family topology. The INA213B specifications are found in the *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors* datasheet.

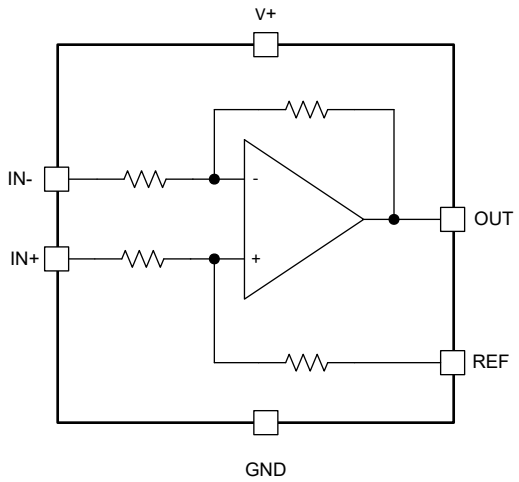


Figure 9-3. INA21x Current-Shunt Monitor Topology

The INA213B is an excellent choice for this application because all the required features are included. In general, instrumentation amplifiers (INAs) do not have the input common-mode swing to ground that is essential for this application. In addition, INAs require external resistors to set the gain, which is not desirable for low-drift applications. Difference amplifiers typically have larger input bias currents, which reduce solution accuracy at small load currents. Difference amplifiers typically have a gain of 1V/V. When the gain is adjustable, these amplifiers use external resistors that are not conducive to low-drift applications.

9.2.1.2.3 Voltage Reference

Confirm that the voltage reference for this application includes following features:

1. Dual output (3.0V and 1.5V)
2. Low drift
3. Low tracking errors between the two outputs

For this design, the REF2030 is used. The REF20xx topology is as shown in Section 8.2.

The REF2030 is an excellent choice for this application because of the dual output. The temperature drift of 8ppm/°C and initial accuracy of 0.05% make the errors resulting from the voltage reference minimal in this application. In addition, there is minimal mismatch between the two outputs and both outputs have excellent tracking across temperature, as shown in Figure 9-4 and Figure 9-5.

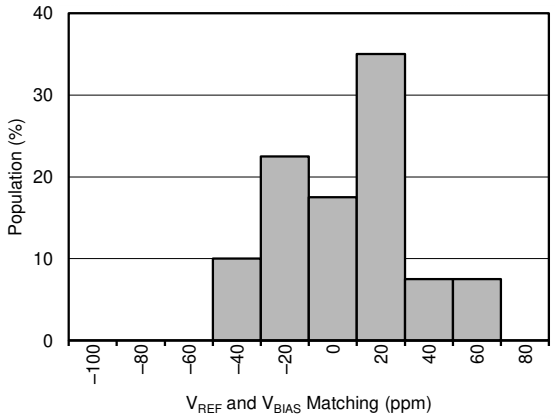


Figure 9-4. V_{REF} – 2 × V_{BIAS} Distribution (At T_A = 25°C)

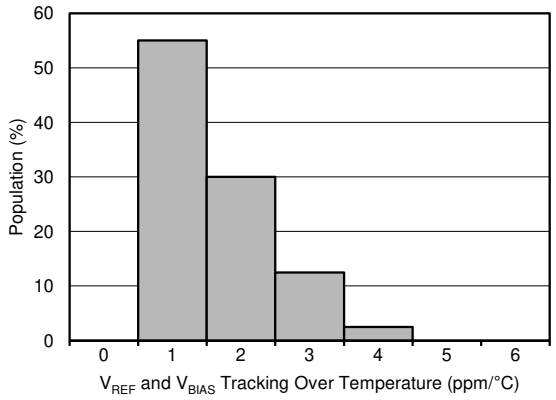


Figure 9-5. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature

9.2.1.2.4 Results

Table 9-1 summarizes the measured results.

Table 9-1. Measured Results

ERROR	UNCALIBRATED (%)	CALIBRATED (%)
Error across the full load current range (25°C)	±0.0355	±0.004
Error across the full load current range (–40°C to 125°C)	±0.0522	±0.0606

9.2.1.3 Application Curves

Performing a two-point calibration at 25°C removes the errors associated with offset voltage, gain error, and so forth. Figure 9-6, Figure 9-7, and Figure 9-8 show the measured error at different conditions. For a more detailed description on measurement procedure, calibration, and calculations, please refer to the *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Design* reference guide.

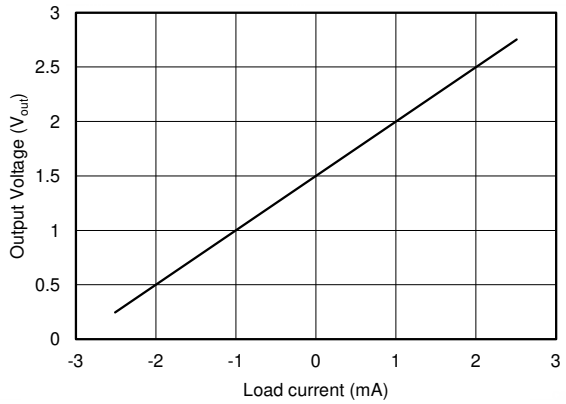


Figure 9-6. Measured Transfer Function

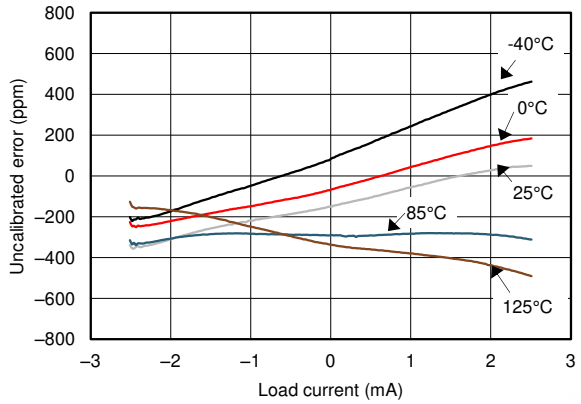


Figure 9-7. Uncalibrated Error vs Load Current

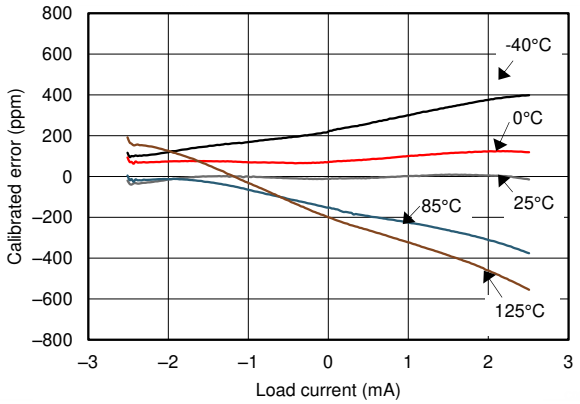


Figure 9-8. Calibrated Error vs Load Current

9.3 Power-Supply Recommendations

The REF20xx family of references feature an extremely low-dropout voltage. Operate the references of the REF20xx family with a supply of only 20mV above the output voltage. For loaded reference conditions, a typical dropout voltage versus load is shown in Figure 9-9. A supply bypass capacitor ranging between 0.1µF to 10µF is recommended.

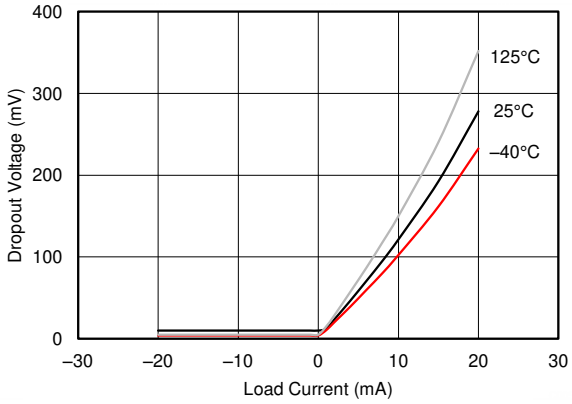


Figure 9-9. Dropout Voltage versus Load Current

9.4 Layout

9.4.1 Layout Guidelines

Figure 9-10 shows an example of a PCB layout for a data acquisition system using the REF2030. Some key considerations are:

- Connect low-ESR, 0.1µF ceramic bypass capacitors at V_{IN}, V_{REF}, and V_{BIAS} of the REF2030.
- Decouple other active devices in the system per the device specifications.
- Use a solid ground plane to distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

9.4.2 Layout Example

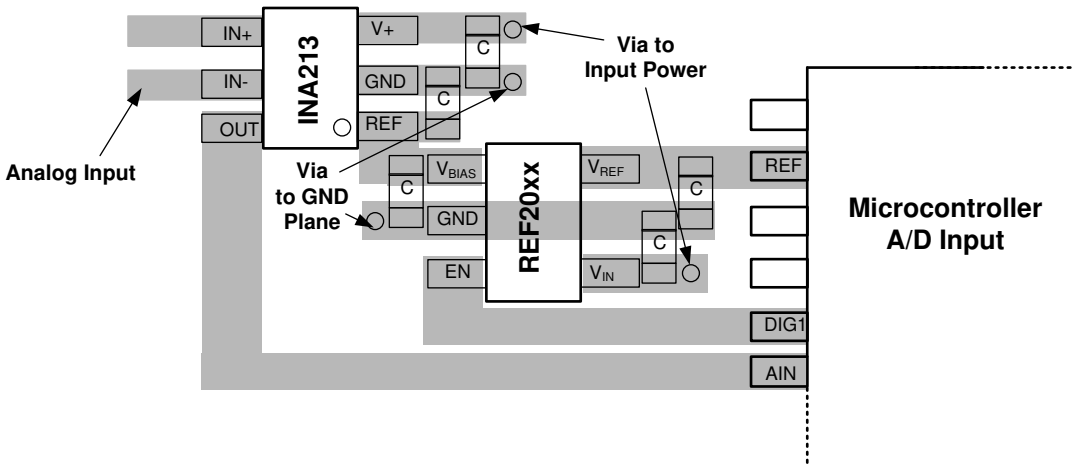


Figure 9-10. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors* data sheet
- Texas Instruments *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Design* reference design
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

e-Trim™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2022) to Revision F (June 2026)	Page
• Moved REF2025, REF2030, REF2033, REF2041 devices to the REF20 product folder on TI.com and updated the datasheet header	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision D (May 2018) to Revision E (January 2022)	Page
• Updated Applications section	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed *ESD Rating* table: changed HBM rating from ±4000V to ±2500V	5
• Updated Long-term stability value	6
• Added Long-Term Stability sub-section under Parameter Measurement Information section	15

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF2025AIDDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AIDDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AIDDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AIDDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AIDDCTG4	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AIDDCTG4.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM
REF2025AISDDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	1M98
REF2025AISDDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	1M98
REF2030AIDDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2030AIDDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2030AIDDCRG4	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2030AIDDCRG4.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2030AIDDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2030AIDDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM
REF2033AIDDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM
REF2033AIDDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF2033AIDDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM
REF2033AIDDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM
REF2033AIDDCTG4	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM
REF2033AIDDCTG4.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM
REF2041AIDDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM
REF2041AIDDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM
REF2041AIDDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM
REF2041AIDDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM
REF2041AIDDCTG4	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM
REF2041AIDDCTG4.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF REF20 :

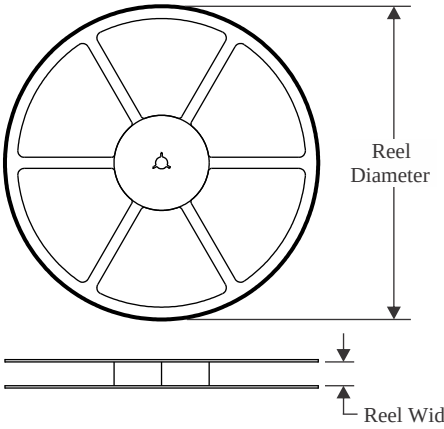
- Automotive : REF20-Q1

NOTE: Qualified Version Definitions:

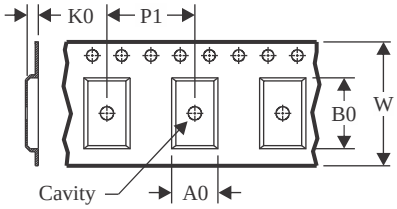
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

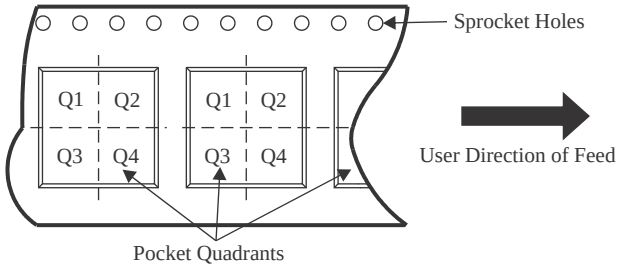


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

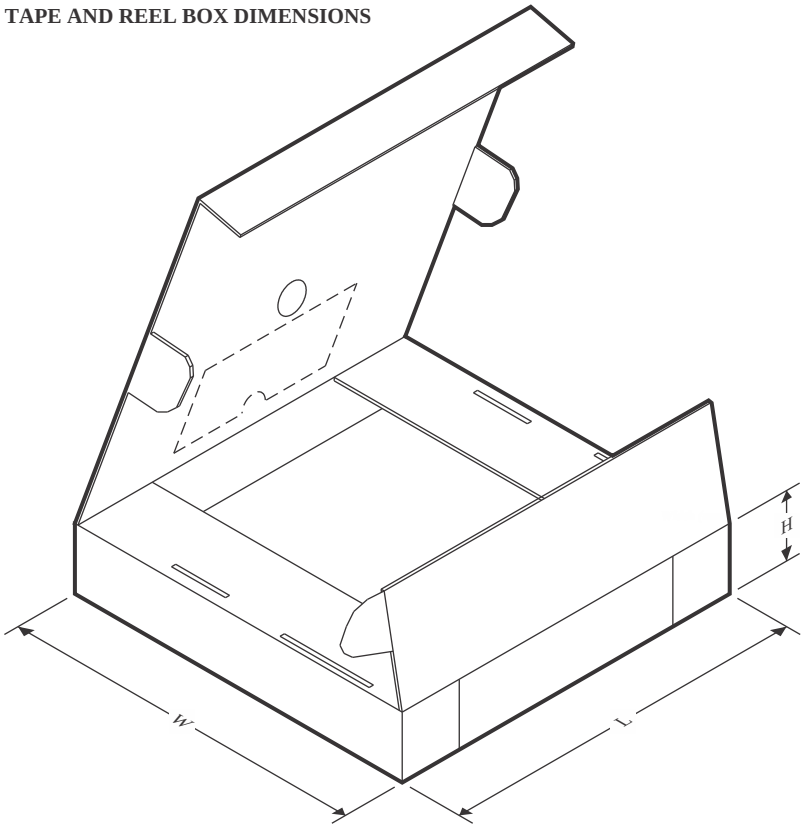


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF2025AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AIDDCTG4	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AISDDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCRG4	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF2033AIDDCTG4	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCTG4	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

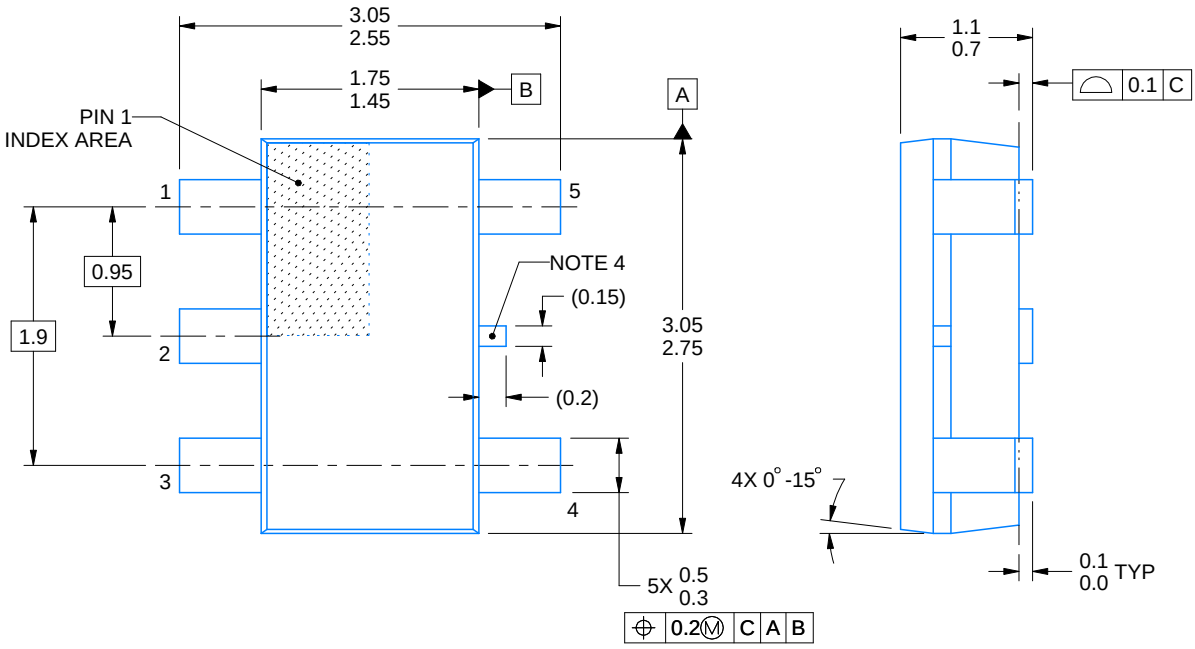
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF2025AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2025AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2025AIDDCTG4	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2025AISDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2030AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2030AIDDCRG4	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2030AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2033AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2033AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2033AIDDCTG4	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2041AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2041AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2041AIDDCTG4	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0

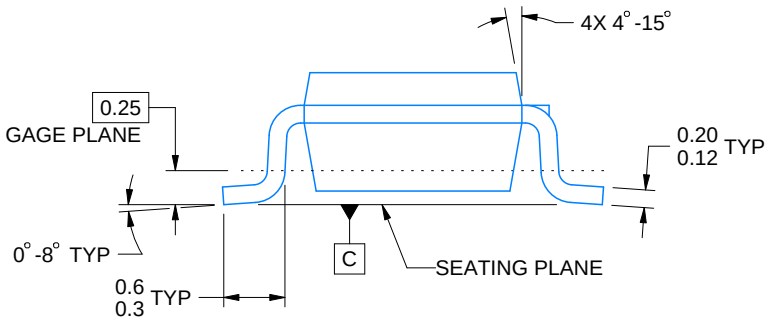
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR





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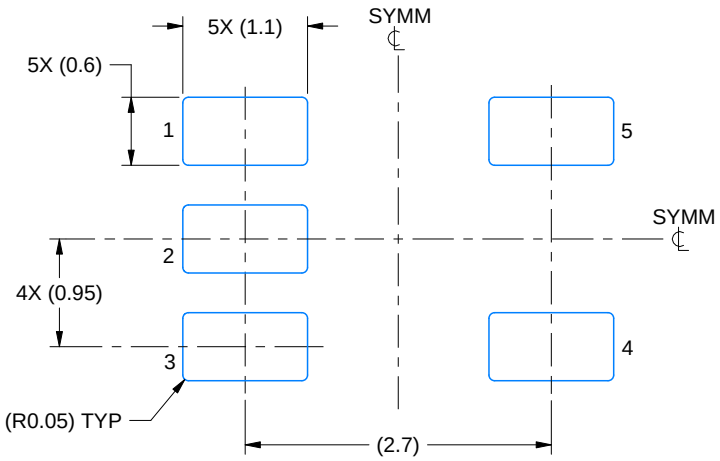
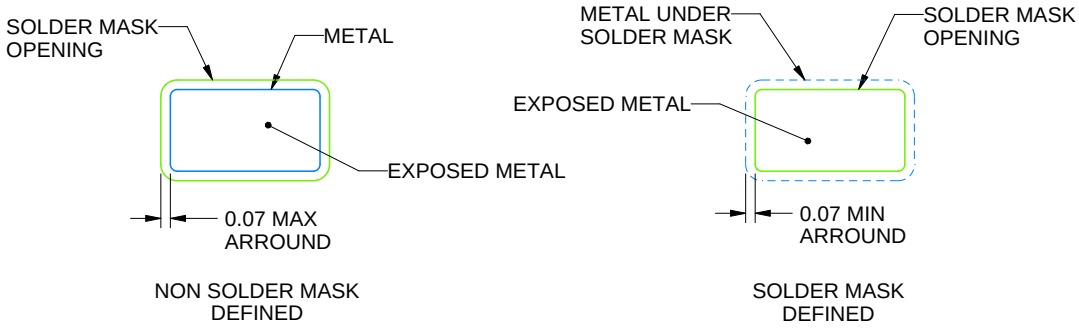
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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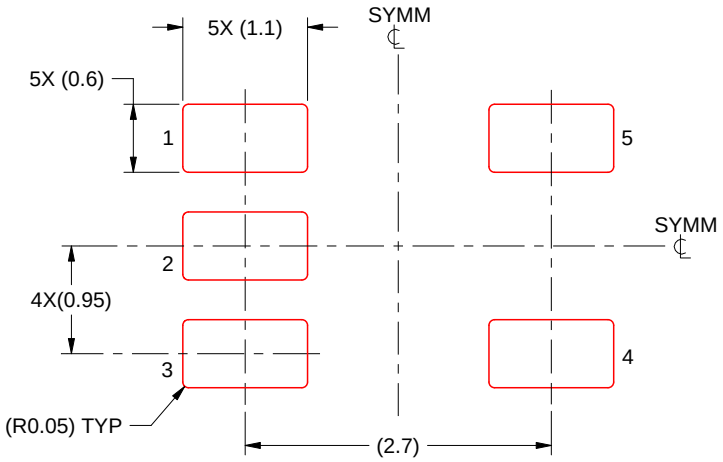
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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