# TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems

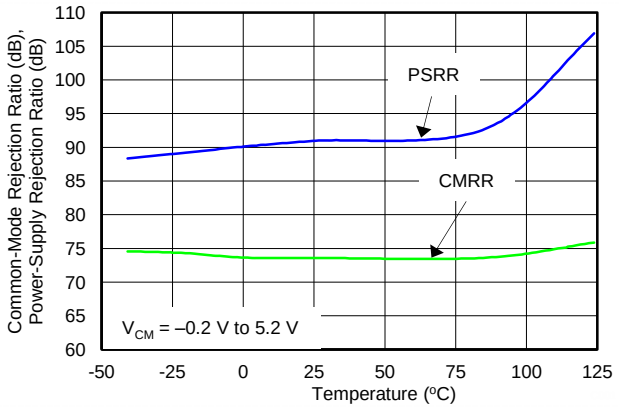
## 1 Features

- Precision Amplifiers for Cost-Sensitive Systems
- Low Quiescent Current: 75 µA/ch
- Supply Range: 1.8 V to 5.5 V
- Input Voltage Noise Density: 28 nV/√Hz at 1 kHz
- Rail-to-Rail Input and Output
- Gain Bandwidth: 1 MHz
- Low Input Bias Current: 1 pA
- Low Offset Voltage: 0.75 mV
- Unity-Gain Stable
- Internal RF and EMI Filter
- Extended Temperature Range: –40°C to +125°C

## 2 Applications

- Industrial and Consumer Electronics
- Portable Equipment
- Portable Blood Glucose Systems
- Smoke Detectors
- White Goods
- Power Banks

**CMRR and PSRR vs Temperature**




## 3 Description

The TLV600x family of single-, dual-, and quad-channel operational amplifiers is specifically designed for general-purpose applications. Featuring rail-to-rail input and output (RRIO) swings, low quiescent current (75 µA, typical), wide bandwidth (1 MHz) and low noise (28 nV/√Hz at 1 kHz), this family is attractive for a variety of applications that require a good balance between cost and performance, such as consumer electronics, smoke detectors, and white goods. The low-input-bias current (±1.0 pA, typical) enables the TLV600x to be used in applications with megaohm source impedances.

The robust design of the TLV600x provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 150 pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM).

The devices are optimized for operation at voltages as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V), and are specified over the extended temperature range of –40°C to +125°C.

The single-channel TLV6001 is available in SC70-5 and SOT23-5 packages. The dual-channel TLV6002 is offered in SOIC-8 and VSSOP-8 packages, and the quad-channel TLV6004 is offered in a TSSOP-14 package.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV6001 | SC70 (5) | 2.00 mm × 1.25 mm |
| | SOT-23 (5) | 2.90 mm × 1.60 mm |
| TLV6002 | SOIC (8) | 4.90 mm × 3.91 mm |
| | VSSOP (8) | 3.00 mm × 3.00 mm |
| TLV6004 | TSSOP (14) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

**Changes from Revision C (December 2016) to Revision D** — **Page**

- Changed inverting input pin to noninverting input pin in *Pin Functions: TLV6001* table ... 3
- Changed inverting input pin to noninverting input pin in *Pin Functions: TLV6001R* table ... 4
- Changed inverting input pin to noninverting input pin in *Pin Functions: TLV6001U* table ... 4
- Changed "Sample and Buy" to "Order Now" in *Related Links* table ... 21

**Changes from Revision B (October 2016) to Revision C** — **Page**

- Changed all pin outs in *Pin Configuration and Functions* section to reflect correct pin names and order ... 3

**Changes from Revision A (July 2016) to Revision B** — **Page**

- Added TLV6001R pinout drawing to *Pin Configurations and Functions* section ... 4
- Added TLV6001U pinout drawing to *Pin Configurations and Functions* section ... 4

**Changes from Original (June 2016) to Revision A** — **Page**

- Changed Product Status from Product Preview to Production Data ... 1
- Changed formatting of the *Related Documentation* section. ... 21
- Changed wording of the *Receiving Notification of Documentation Updates* section ... 21

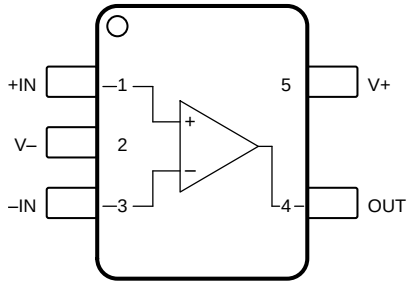

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## 5 Device Comparison Table

| DEVICE | NO. OF CHANNELS | PACKAGE-LEADS | | | | |
|---|---|---|---|---|---|---|
| | | SC70 | SOT-23 | SOIC | VSSOP | TSSOP |
| TLV6001 | 1 | 5 | 5 | — | — | — |
| TLV6002 | 2 | — | — | 8 | 8 | — |
| TLV6004 | 4 | — | — | — | — | 14 |

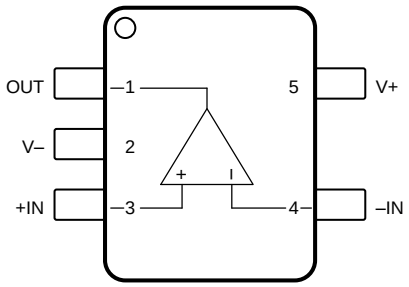
## 6 Pin Configuration and Functions

**TLV6001: DCK Package**
**5-Pin SC70**
**Top View**




Not to scale

**TLV6001: DBV Package**
**5-Pin SOT-23**
**Top View**



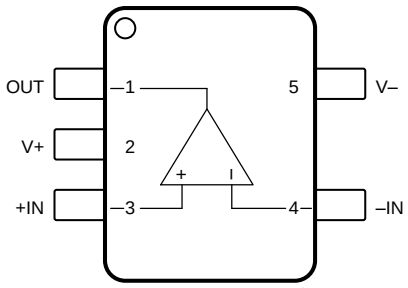

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**Pin Functions: TLV6001**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DCK (SC70) | DBV (SOT-23) | | |
| –IN | 3 | 4 | I | Inverting input |
| +IN | 1 | 3 | I | Noninverting input |
| OUT | 4 | 1 | O | Output |
| V– | 2 | 2 | — | Negative (lowest) power supply |
| V+ | 5 | 5 | — | Positive (highest) power supply |

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**TLV6001R: DBV Package**
**5-Pin SOT-23**
**Top View**

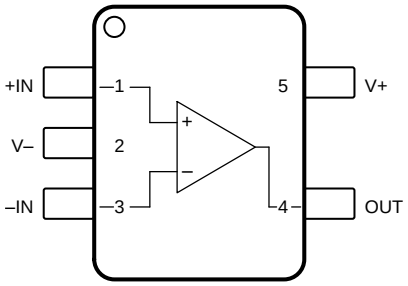



Not to scale

## Pin Functions: TLV6001R

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN | 4 | I | Inverting input |
| +IN | 3 | I | Noninverting input |
| OUT | 1 | O | Output |
| V– | 5 | — | Negative (lowest) power supply |
| V+ | 2 | — | Positive (highest) power supply |

**TLV6001U: DBV Package**
**5-Pin SOT-23**
**Top View**



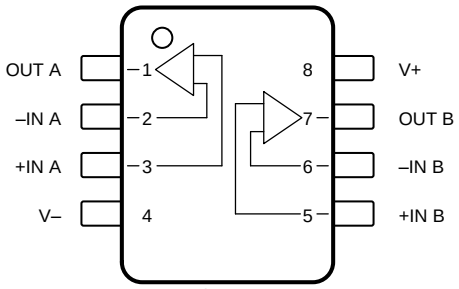

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## Pin Functions: TLV6001U

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN | 3 | I | Inverting input |
| +IN | 1 | I | Noninverting input |
| OUT | 4 | O | Output |
| V– | 2 | — | Negative (lowest) power supply |
| V+ | 5 | — | Positive (highest) power supply |


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**TLV6002: D, DGK Packages**
**8-Pin SOIC, 8-Pin VSSOP**
**TLV6002 Top View**



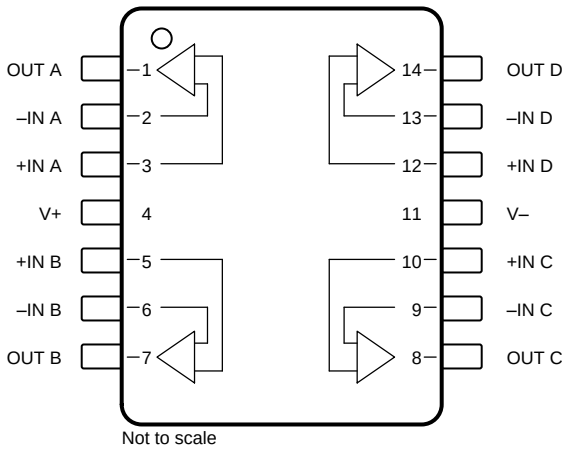

Not to scale

## Pin Functions: TLV6002

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | D (SOIC) | DGK (VSSOP) | | |
| –IN A | 2 | 2 | I | Inverting input, channel A |
| –IN B | 6 | 6 | I | Inverting input, channel B |
| +IN A | 3 | 3 | I | Noninverting input, channel A |
| +IN B | 5 | 5 | I | Noninverting input, channel B |
| OUT A | 1 | 1 | O | Output, channel A |
| OUT B | 7 | 7 | O | Output, channel B |
| V– | 4 | 4 | — | Negative (lowest) power supply |
| V+ | 8 | 8 | — | Positive (highest) power supply |

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**TLV6004: PW Package**
**14-Pin TSSOP**
**Top View**




Not to scale

## Pin Functions: TLV6004

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| –IN C | 9 | I | Inverting input, channel C |
| –IN D | 13 | I | Inverting input, channel D |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| +IN C | 10 | I | Noninverting input, channel C |
| +IN D | 12 | I | Noninverting input, channel D |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| OUT C | 8 | O | Output, channel C |
| OUT D | 14 | O | Output, channel D |
| V– | 11 | — | Negative (lowest) power supply |
| V+ | 4 | — | Positive (highest) power supply |


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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | Supply voltage | | 7 | V |
| | Signal input pins, voltage(2) | (V–) – 0.5 | (V+) + 0.5 | V |
| Current | Signal input pins, current(2) | –10 | 10 | mA |
| | Output short-circuit(3) | Continuous | | mA |
| Temperature | Operating, $T_A$ | –40 | 150 | °C |
| | Junction, $T_J$ | | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage | 1.8 | 5.5 | V |
| $T_A$ | Specified temperature range | –40 | 125 | °C |

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## 7.4 Thermal Information: TLV6001

| THERMAL METRIC(1) | | TLV6001 | | UNIT |
|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | |
| | | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 228.5 | 281.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 99.1 | 91.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 54.6 | 59.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.7 | 1.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 53.8 | 58.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Thermal Information: TLV6002

| THERMAL METRIC(1) | | TLV6002 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 138.4 | 191.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 89.5 | 61.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 78.6 | 111.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 29.9 | 5.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 78.1 | 110.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.6 Thermal Information: TLV6004

| THERMAL METRIC(1) | | TLV6004 | UNIT |
|---|---|---|---|
| | | PW (TSSOP) | |
| | | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 121.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 49.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 62.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 5.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 62.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


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## 7.7 Electrical Characteristics: $V_S$= 1.8 V to 5 V (±0.9 V to ±2.75 V)(1)

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, and $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | | | 0.75 | 4.5 | mV |
| $dV_{OS}/dT$ | $V_{OS}$ vs temperature | $T_A$ = –40°C to 125°C | | 2 | | µV/°C |
| PSRR | Power-supply rejection ratio | | | 86 | | dB |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $T_A$ = 25°C | | ±1.0 | | pA |
| $I_{OS}$ | Input offset current | | | ±1.0 | | pA |
| **INPUT IMPEDANCE** | | | | | | |
| $Z_{ID}$ | Differential | | | 100 \|\| 1 | | MΩ \|\| pF |
| $Z_{IC}$ | Common-mode | | | 1 \|\| 5 | | $10^{13}$Ω \|\| pF |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{CM}$ | Common-mode voltage range | No phase reversal, rail-to-rail input | (V–) – 0.2 | | (V+) + 0.2 | V |
| CMRR | Common-mode rejection ratio | $V_{CM}$ = –0.2 V to 5.7 V | 60 | 76 | | dB |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | 0.3 V < $V_O$ < (V+) – 0.3 V, $R_L$ = 2 kΩ | 90 | 110 | | |
| | Phase margin | $V_S$ = 5.0 V, G = +1 | | 65 | | degrees |
| **OUTPUT** | | | | | | |
| $V_O$ | Voltage output swing from supply rails | $R_L$ = 100 kΩ | | 5 | | mV |
| | | $R_L$ = 2 kΩ | | 75 | 100 | mV |
| $I_{SC}$ | Short-circuit current | | | ±15 | | mA |
| $R_O$ | Open-loop output impedance | | | 2300 | | Ω |
| **FREQUENCY RESPONSE** | | | | | | |
| GBW | Gain-bandwidth product | | | 1 | | MHz |
| SR | Slew rate | | | 0.5 | | V/µs |
| $t_S$ | Settling time | To 0.1%, $V_S$ = 5.0 V, 2-V step , G = +1 | | 5 | | µs |
| **NOISE** | | | | | | |
| | Input voltage noise (peak-to-peak) | f = 0.1 Hz to 10 Hz | | 6 | | $\mu V_{PP}$ |
| $e_n$ | Input voltage noise density | f = 1 kHz | | 28 | | nV/√Hz |
| $i_n$ | Input current noise density | f = 1 kHz | | 5 | | fA/√Hz |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Specified voltage range | | 1.8 (±0.9) | | 5.5 (±2.75) | V |
| $I_Q$ | Quiescent current per amplifier | $I_O$ = 0 mA, $V_S$ = 5.0 V | | 75 | 100 | µA |
| | Power-on time | $V_S$ = 0 V to 5 V, to 90% $I_Q$ level | | 10 | | µs |

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25ºC, unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.

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## 7.8 Typical Characteristics: Table of Graphs

**Table 1. Table of Graphs**

| TITLE | FIGURE |
|---|---|
| Open-Loop Gain and Phase vs Frequency | Figure 1 |
| Quiescent Current vs Supply Voltage | Figure 2 |
| Offset Voltage Production Distribution | Figure 3 |
| Offset Voltage vs Common-Mode Voltage (Maximum Supply) | Figure 4 |
| CMRR and PSRR vs Frequency (RTI) | Figure 5 |
| 0.1-Hz to 10-Hz Input Voltage Noise (5.5 V) | Figure 6 |
| Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V) | Figure 7 |
| Input Bias and Offset Current vs Temperature | Figure 8 |
| Open-Loop Output Impedance vs Frequency | Figure 9 |
| Maximum Output Voltage vs Frequency and Supply Voltage | Figure 10 |
| Output Voltage Swing vs Output Current (over Temperature) | Figure 11 |
| Closed-Loop Gain vs Frequency, G = 1, –1, 10 (1.8 V) | Figure 12 |
| Small-Signal Step Response, Noninverting (1.8 V) | Figure 13 |
| Small-Signal Step Response, Noninverting ( 5.5 V) | Figure 14 |
| Large-Signal Step Response, Noninverting (1.8 V) | Figure 15 |
| Large-Signal Step Response, Noninverting ( 5.5 V) | Figure 16 |
| No Phase Reversal | Figure 17 |
| EMIRR IN+ vs Frequency | Figure 18 |


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## 7.9 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = 5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, and $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

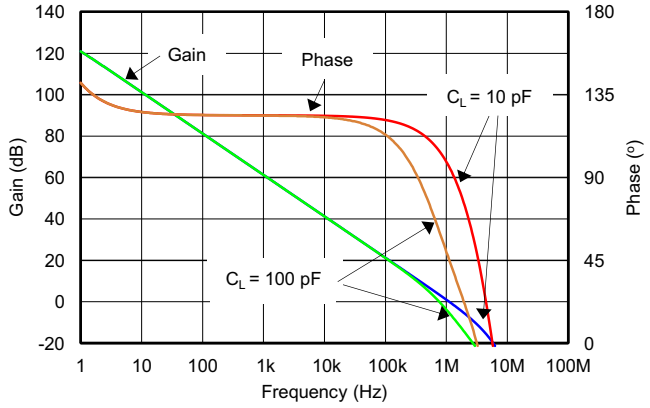



**Figure 1. Open-Loop Gain and Phase vs Frequency**

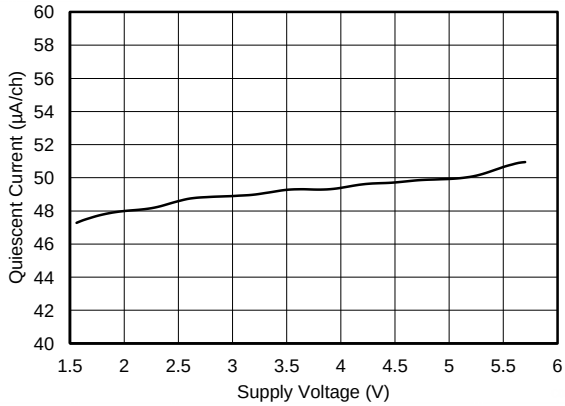



**Figure 2. Quiescent Current vs Supply**

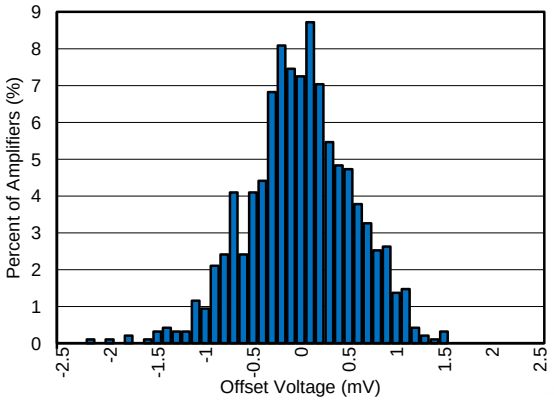



**Figure 3. Offset Voltage Production Distribution**

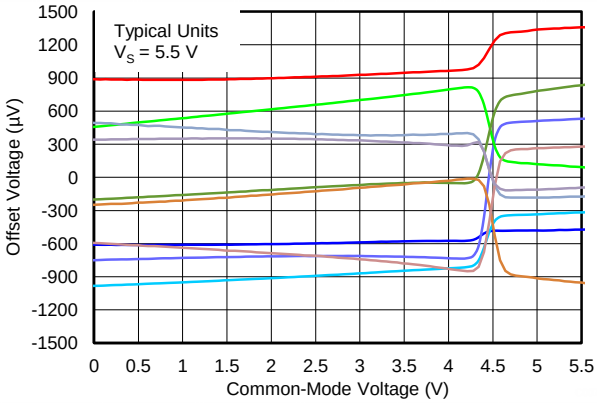



**Figure 4. Offset Voltage vs Common-Mode Voltage**

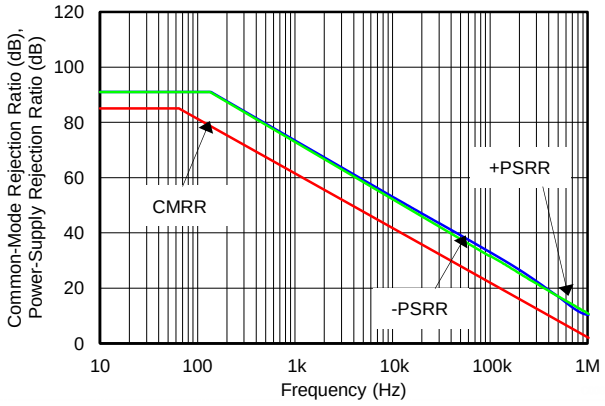



**Figure 5. CMRR and PSRR vs Frequency (Referred-to-Input)**

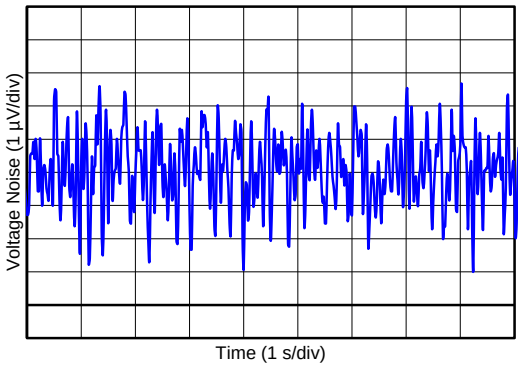



**Figure 6. 0.1-Hz to 10-Hz Input Voltage Noise**

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## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, and $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

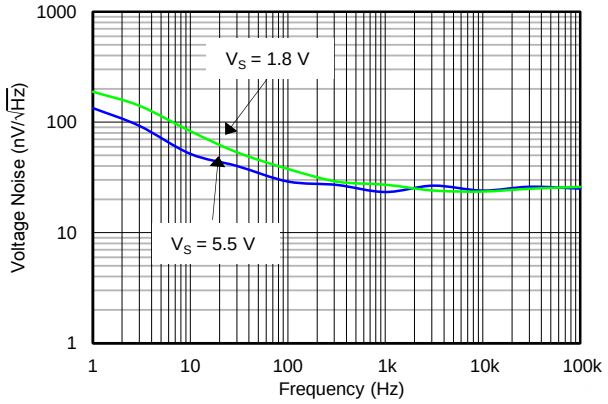



**Figure 7. Input Voltage Noise Spectral Density vs Frequency**

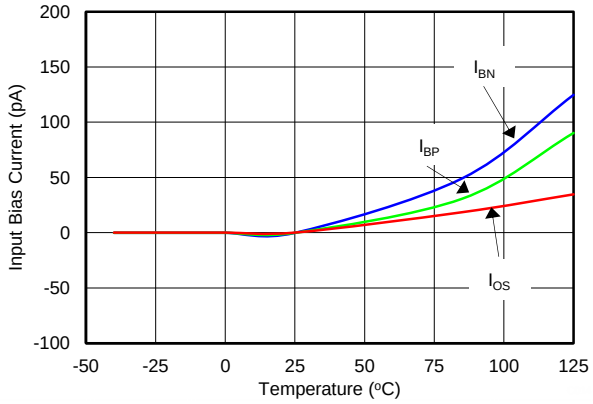



**Figure 8. Input Bias and Offset Current vs Temperature**

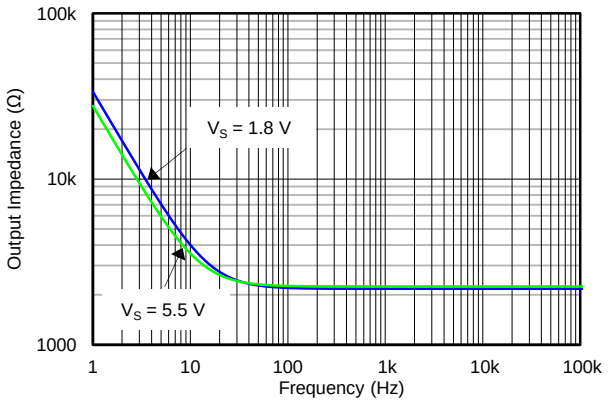



**Figure 9. Open-Loop Output Impedance vs Frequency**

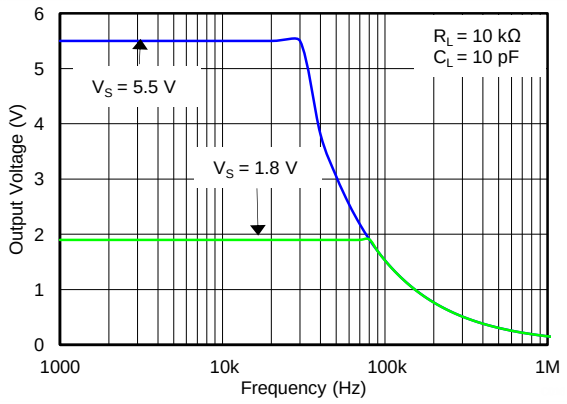



**Figure 10. Maximum Output Voltage vs Frequency and Supply Voltage**

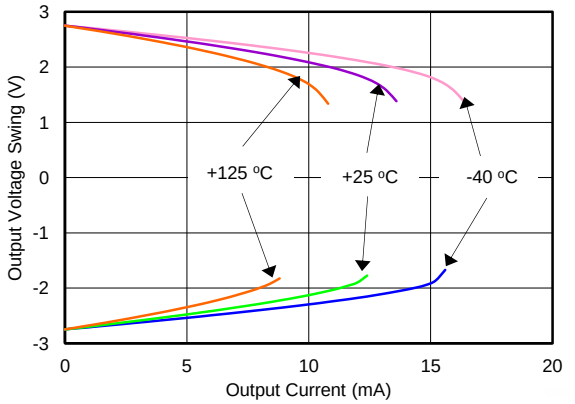



**Figure 11. Output Voltage Swing vs Output Current (Over Temperature)**

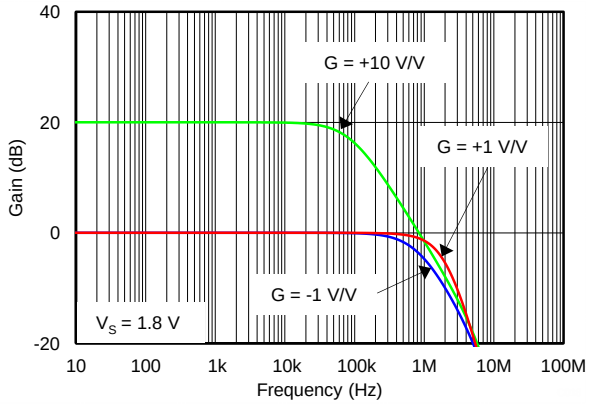



**Figure 12. Closed-Loop Gain vs Frequency (Minimum Supply)**


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## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, and $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

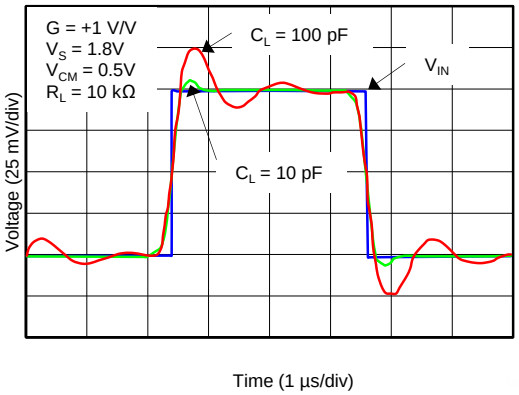



**Figure 13. Small-Signal Pulse Response (Minimum Supply)**

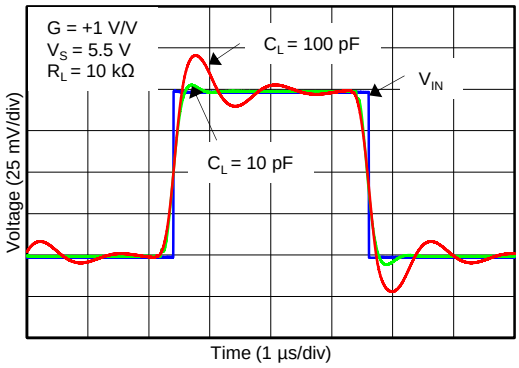



**Figure 14. Small-Signal Pulse Response (Maximum Supply)**

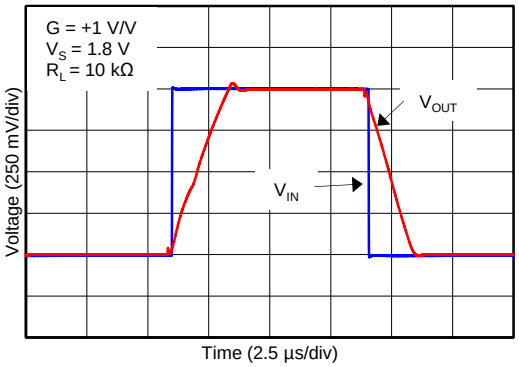



**Figure 15. Large-Signal Pulse Response (Minimum Supply)**

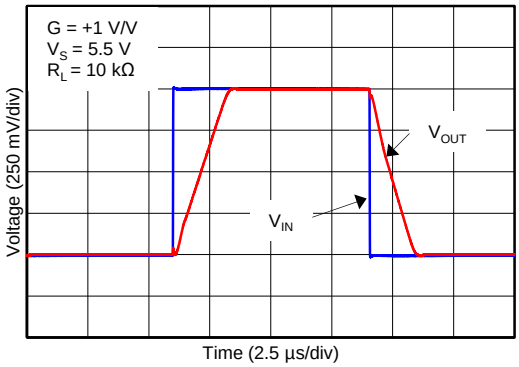



**Figure 16. Large-Signal Pulse Response (Maximum Supply)**

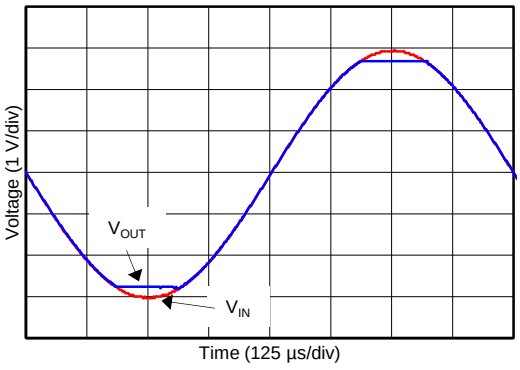



**Figure 17. No Phase Reversal**

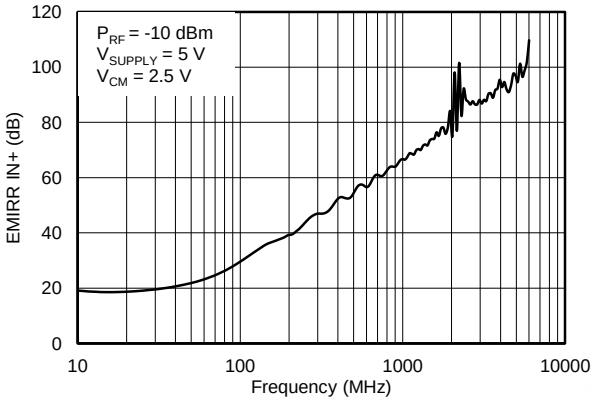


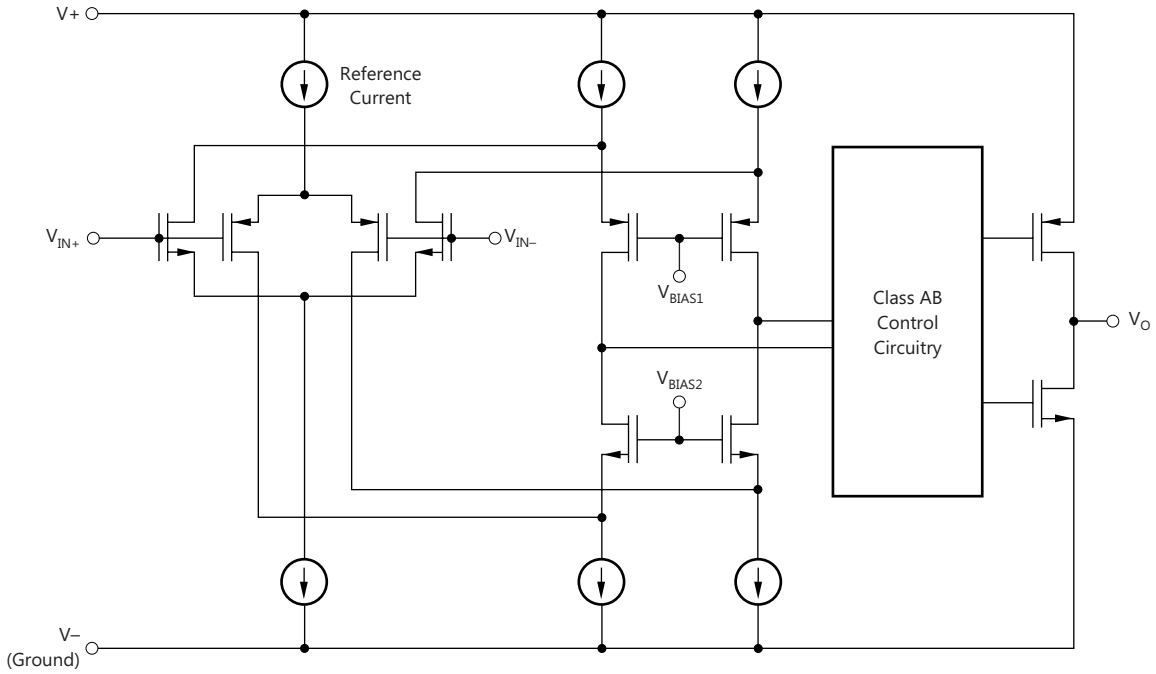

**Figure 18. EMIRR IN+ vs Frequency**

# 8 Detailed Description

## 8.1 Overview

The TLV600x family of operational amplifiers are general-purpose, low-cost devices that are suitable for a wide range of portable applications. Rail-to-rail input and output swings, low quiescent current, and wide dynamic range make the op amps well-suited for driving sampling analog-to-digital converters (ADCs) and other single-supply applications.

## 8.2 Functional Block Diagram




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## 8.3 Feature Description

### 8.3.1 Operating Voltage

The TLV600x series is fully specified and tested from 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Parameters that vary with supply voltage are illustrated in the *Typical Characteristics* section.

### 8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV600x series extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 200 mV above the positive supply, while the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1.3 V. There is a small transition region, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region may vary up to 300 mV with process variation. Thus, the transition region (both stages on) may range from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to device operation outside this region.

### 8.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the TLV600x delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 100 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails, as shown in Figure 11.

### 8.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the TLV600x is specified in several ways so the best match for a given application may be used; see *Electrical Characteristics*. First, the CMRR of the device in the common-mode range below the transition region [$V_{CM}$ < (V+) – 1.3 V] is given. This specification is the best indicator of the capability of the device when the application requires the use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at ($V_{CM}$ = –0.2 V to 5.7 V). This last value includes the variations seen through the transition region, as shown in Figure 4.

### 8.3.5 Capacitive Load and Stability

The TLV600x is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the TLV600x may become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op amp in the unity-gain (+1-V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the TLV600x remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some capacitors ($C_L$ greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains.

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## Feature Description (continued)

One technique for increasing the capacitive load drive capability of the amplifier when it operates in a unity-gain configuration is to insert a small resistor, typically 10!~ !~~Ω to 20!~ !~~Ω, in series with the output, as shown in Figure 19. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

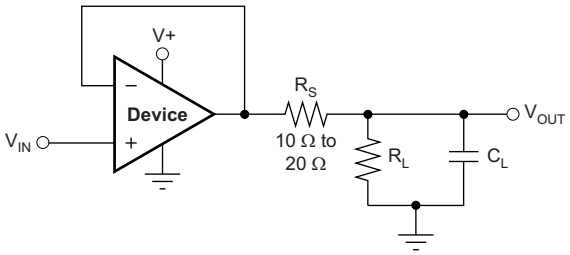



**Figure 19. Improving Capacitive Load Drive**

### 8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op amp pin functions may be affected by EMI, the signal input pins are likely to be the most susceptible. The TLV600x family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Common-mode and differential mode filtering are provided by this filter. The filter is designed for a cutoff frequency of approximately 35 MHz (–3 dB), with a !~ roll-off!~ rolloff of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. Figure 18 illustrates the results of this testing on the TLV600x family. Detailed information may be found in *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

## 8.4 Device Functional Modes

The TLV600x have a single functional mode. The devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

## 8.5 Input and ESD Protection

The TLV600x incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. The ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the *Absolute Maximum Ratings* table. Figure 20 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

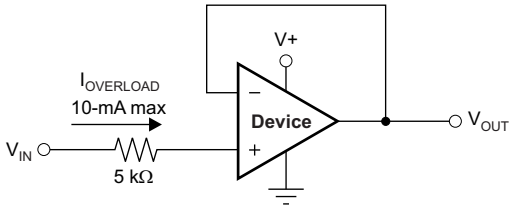



**Figure 20. Input Current Protection**


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# 9 Application and Implementation

**NOTE**

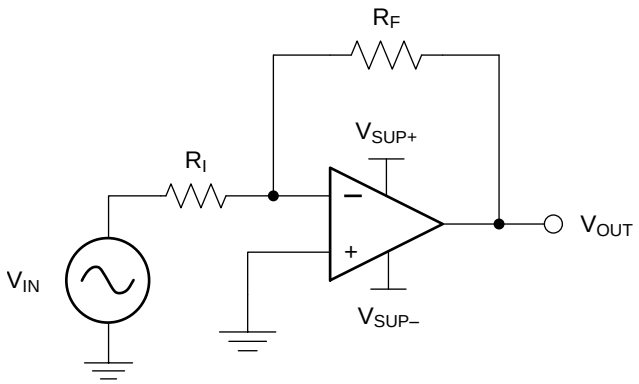
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TLV600x is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. The devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the TLV600x to be used in any single-supply application.

## 9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in Figure 21. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier makes negative input voltages positive on the output. In addition, amplification may be added by selecting the input resistor $R_I$ and the feedback resistor $R_F$.




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**Figure 21. Application Schematic**

### 9.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range ($V_{CM}$) and the output voltage swing to the rails ($V_O$) must be considered. For instance, this application scales a signal of ±0.5 V (1 V) to ±1.8 V (3.6 V). Setting the supply at ±2.5 V is sufficient to accommodate this application.

### 9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

## Typical Application (continued)

When the desired gain is determined, choose a value for $R_I$ or $R_F$. Choosing a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that large resistors (hundreds of kilohms) draw the smallest current but generate the highest noise. Small resistors (100s of ohms) generate low noise but draw high current. This example uses 10 kΩ for $R_I$, meaning 36 kΩ is used for $R_F$. The values are determined by Equation 3:

$$A_V = -\frac{R_F}{R_I} \tag{3}$$

### 9.2.3 Application Curve

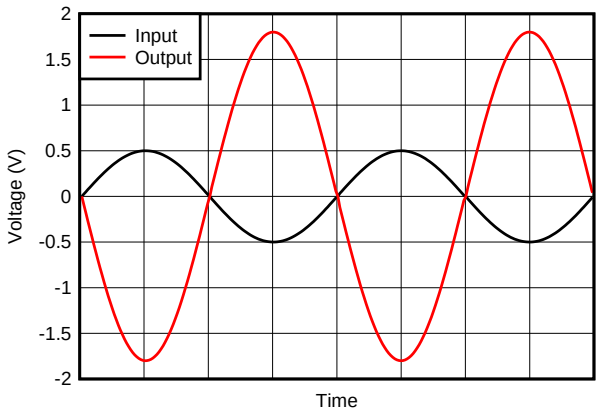



**Figure 22. Inverting Amplifier Input and Output**

## 9.3 System Examples

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in Figure 23.

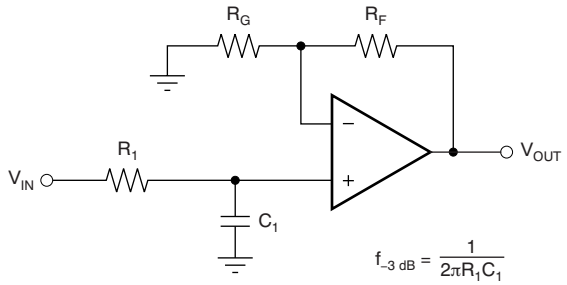



**Figure 23. Single-Pole Low-Pass Filter**


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### System Examples (continued)

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter may be used for this task, as shown in Figure 24. For best results, the amplifier must have a bandwidth that is eight to 10 times the filter frequency bandwidth. Failure to follow this guideline may result in phase shift of the amplifier.

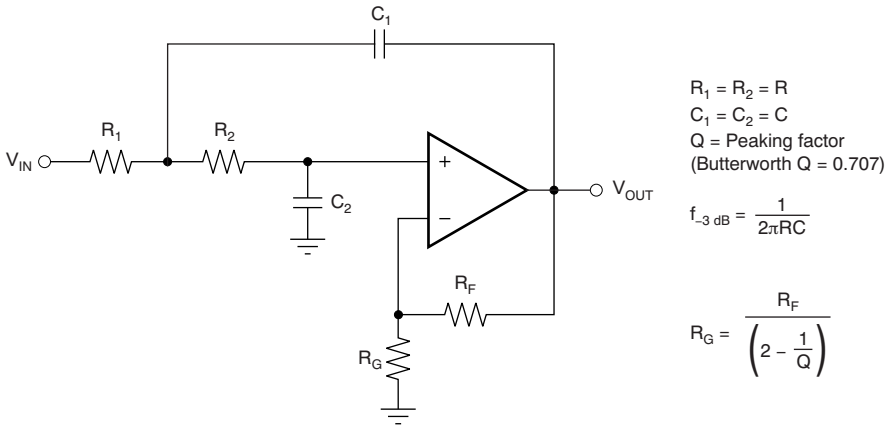



**Figure 24. Two-Pole, Low-Pass, Sallen-Key Filter**

## 10 Power Supply Recommendations

The TLV600x is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

**CAUTION**

Supply voltages larger than 7 V may permanently damage the device. (See the *Absolute Maximum Ratings* table).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

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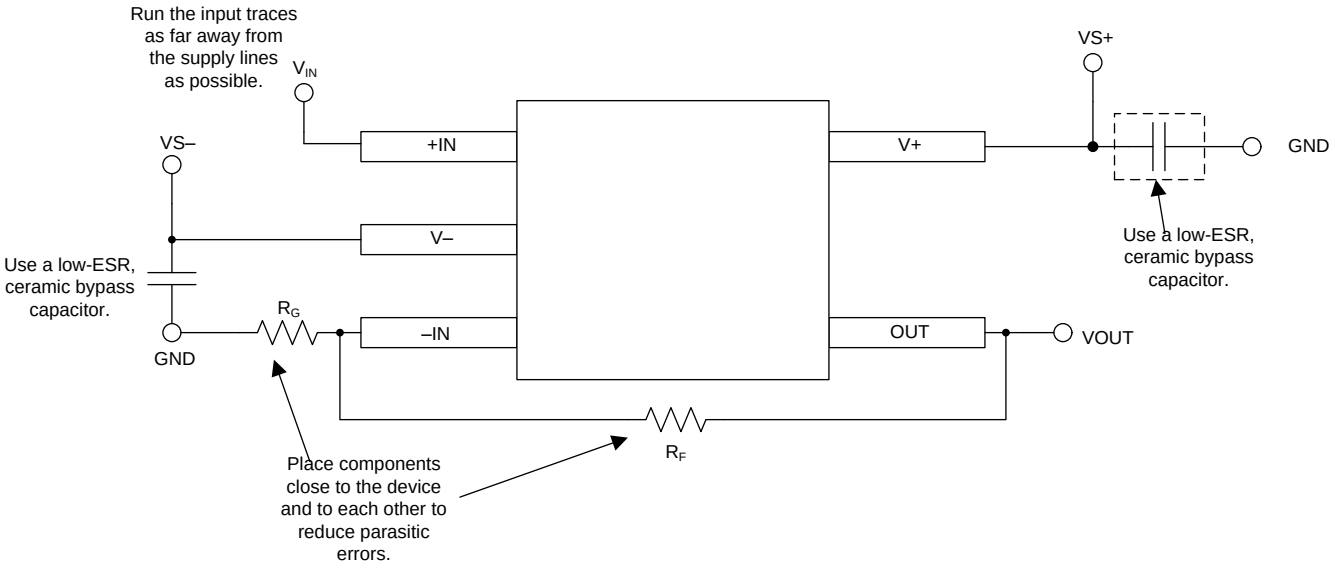
# 11 Layout

## 11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise may propagate into analog circuitry through the power pins of the circuit and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If the traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep $R_F$ and $R_G$ close to the inverting input in order to minimize parasitic capacitance, as shown in Figure 25.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Example




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**Figure 25. Operational Amplifier Board Layout for Noninverting Configuration**

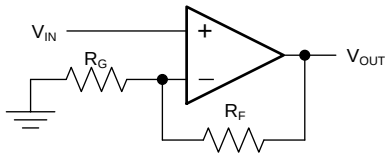



**Figure 26. Schematic Representation of Figure 25**


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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

- *EMI Rejection Ratio of Operational Amplifiers* (SBOA128)
- *Circuit Board Layout Techniques* (SLOA089)

## 12.2 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TLV6001 | Click here | Click here | Click here | Click here | Click here |
| TLV6002 | Click here | Click here | Click here | Click here | Click here |
| TLV6004 | Click here | Click here | Click here | Click here | Click here |

## 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV6001IDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 14W2 |
| TLV6001IDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14W2 |
| TLV6001IDBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 14W2 |
| TLV6001IDBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14W2 |
| TLV6001IDCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN \| POST-PLAT AG SPOT | Level-2-260C-1 YEAR | -40 to 125 | 13X |
| TLV6001IDCKR.A | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 13X |
| TLV6001IDCKT | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| SN \| POST-PLAT AG SPOT | Level-2-260C-1 YEAR | -40 to 125 | 13X |
| TLV6001IDCKT.A | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 13X |
| TLV6001RIDBVR | NRND | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 16O2 |
| TLV6001RIDBVR.A | NRND | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 16O2 |
| TLV6001RIDBVT | NRND | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 16O2 |
| TLV6001RIDBVT.A | NRND | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 16O2 |
| TLV6001UIDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 16P2 |
| TLV6001UIDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 16P2 |
| TLV6001UIDBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 16P2 |
| TLV6001UIDBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 16P2 |
| TLV6002IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 14TV |
| TLV6002IDGKR.A | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14TV |
| TLV6002IDGKRG4 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14TV |
| TLV6002IDGKRG4.A | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14TV |
| TLV6002IDGKT | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU \| SN \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 14TV |
| TLV6002IDGKT.A | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14TV |
| TLV6002IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | (TL6002, V6002) |
| TLV6002IDR.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | (TL6002, V6002) |
| TLV6002IDRG4 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | V6002 |
| TLV6002IDRG4.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | V6002 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV6004IPWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | TLV6004 |
| TLV6004IPWR.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV6004 |
| TLV6004IPWRG4 | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV6004 |
| TLV6004IPWRG4.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV6004 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV6001, TLV6002 :**

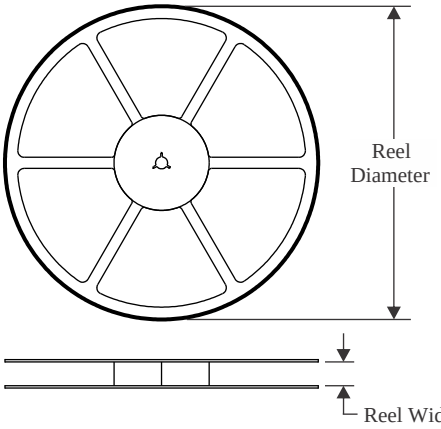
- Automotive : TLV6001-Q1, TLV6002-Q1

NOTE: Qualified Version Definitions:

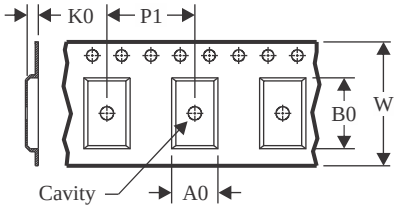
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

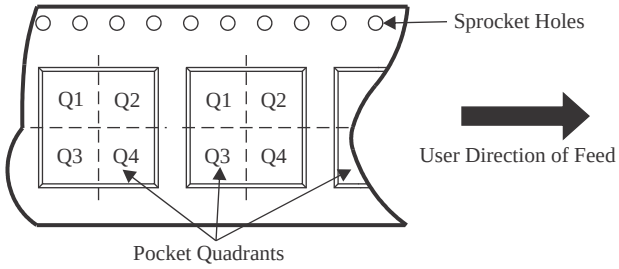



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

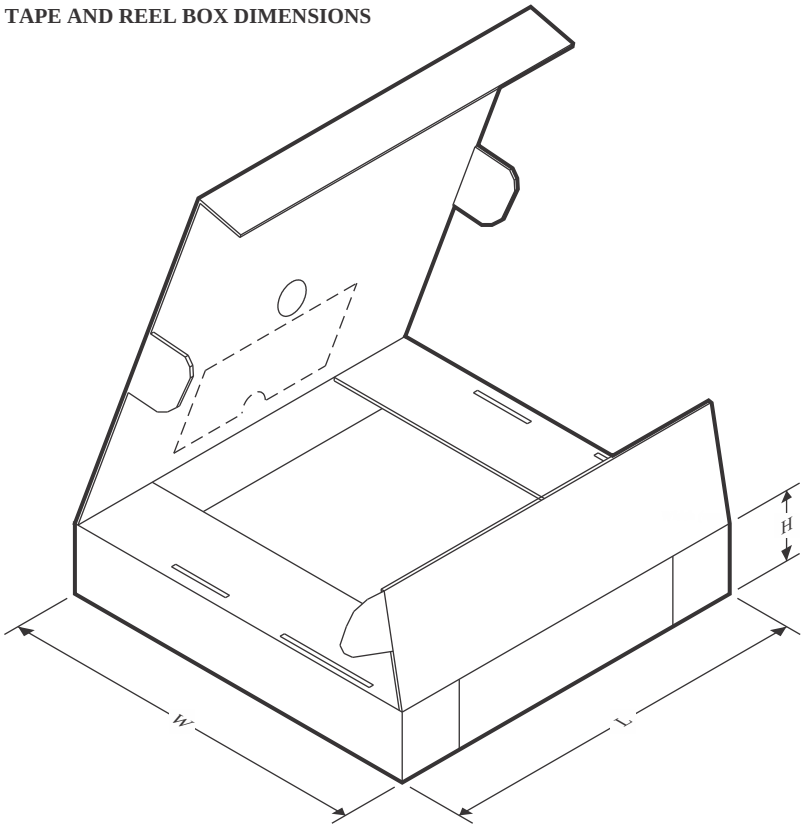



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV6001IDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV6001IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV6001IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV6001IDCKR | SC70 | DCK | 5 | 3000 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV6001IDCKT | SC70 | DCK | 5 | 250 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV6001RIDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV6001RIDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV6001UIDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV6001UIDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV6001UIDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV6002IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV6002IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV6002IDGKRG4 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV6002IDGKT | VSSOP | DGK | 8 | 250 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV6002IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV6002IDRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV6004IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV6004IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV6004IPWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV6001IDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TLV6001IDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV6001IDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV6001IDCKR | SC70 | DCK | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TLV6001IDCKT | SC70 | DCK | 5 | 250 | 208.0 | 191.0 | 35.0 |
| TLV6001RIDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV6001RIDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV6001UIDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TLV6001UIDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV6001UIDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV6002IDGKR | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV6002IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 36.0 |
| TLV6002IDGKRG4 | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV6002IDGKT | VSSOP | DGK | 8 | 250 | 353.0 | 353.0 | 32.0 |
| TLV6002IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV6002IDRG4 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV6004IPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TLV6004IPWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

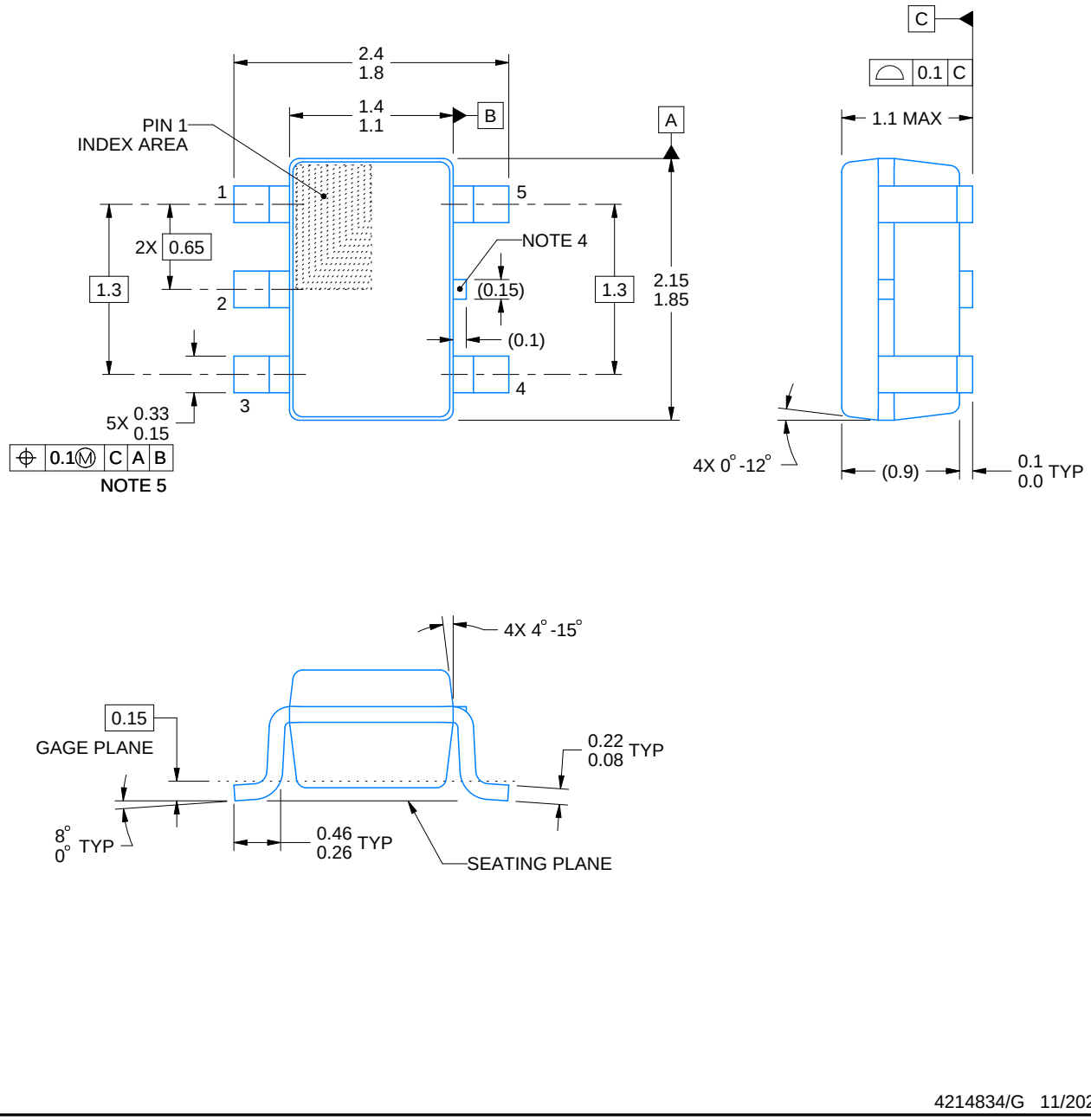
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV6004IPWRG4 | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

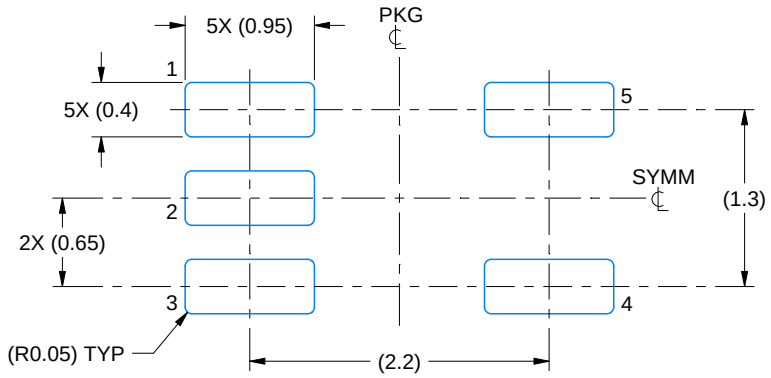
SMALL OUTLINE TRANSISTOR



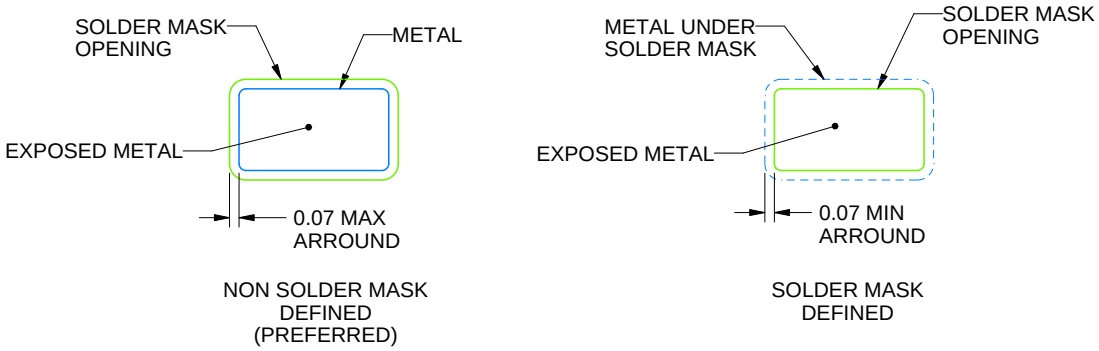

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

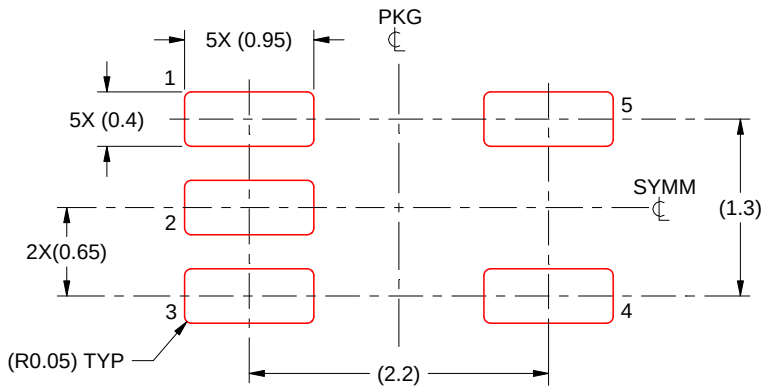



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

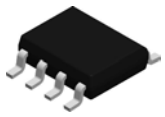



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

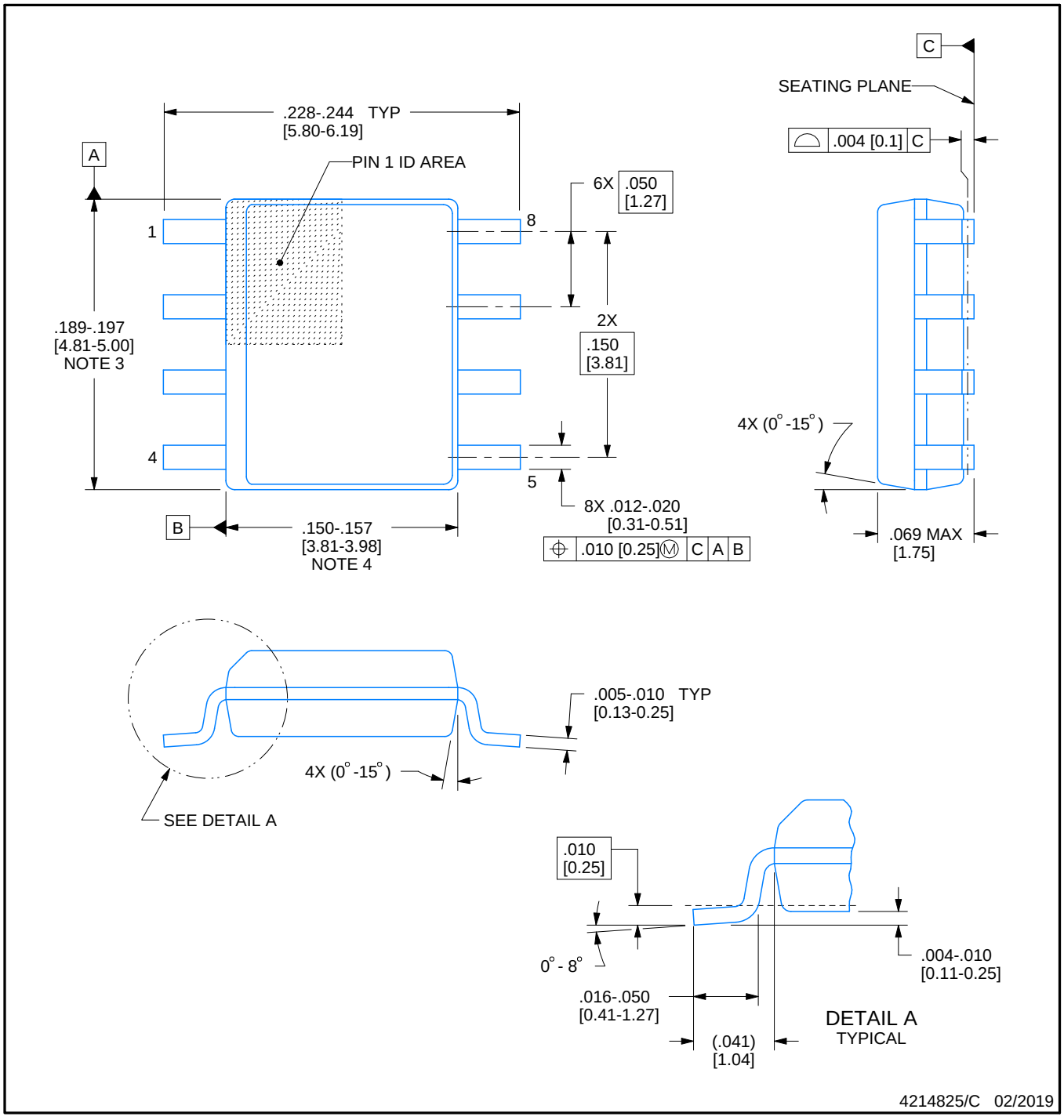


# PACKAGE OUTLINE

## D0008A

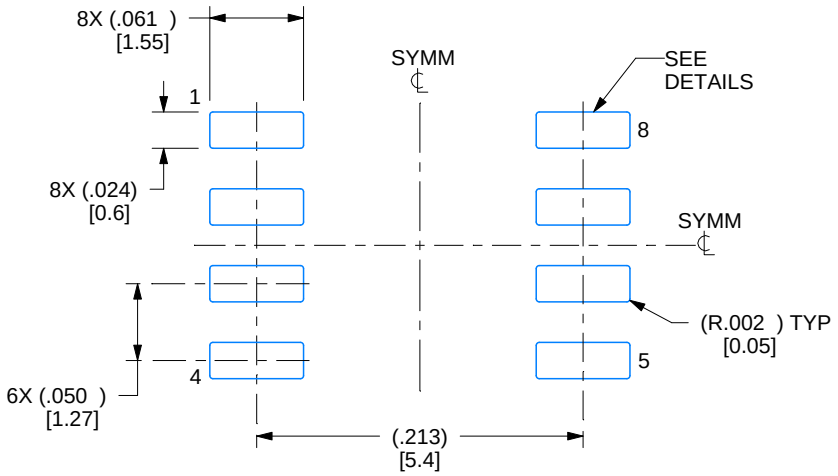
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

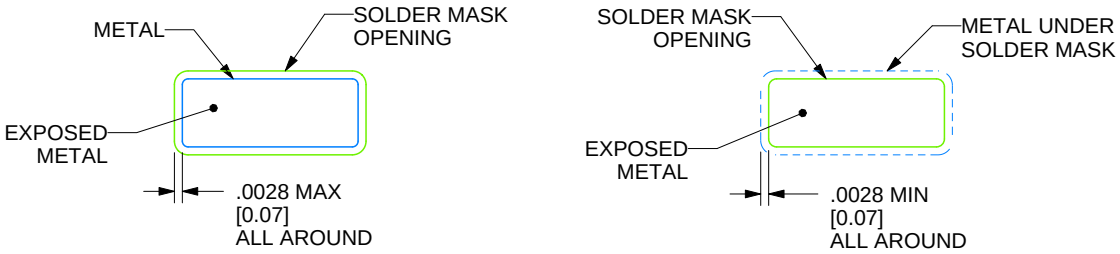



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

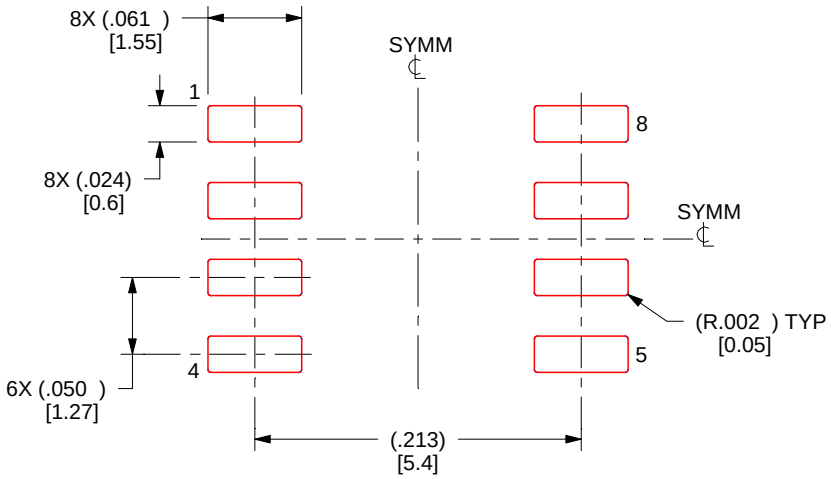
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

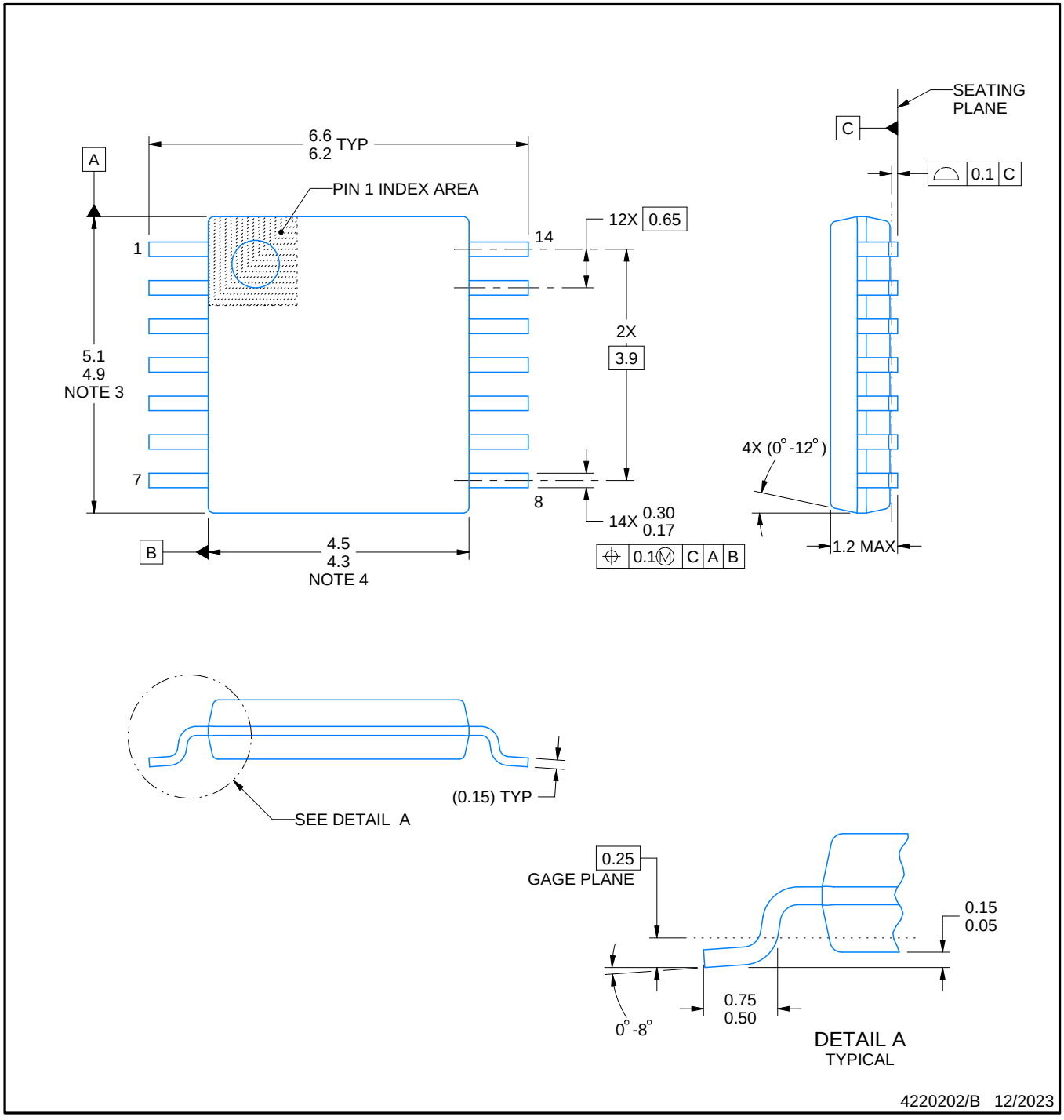
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0014A

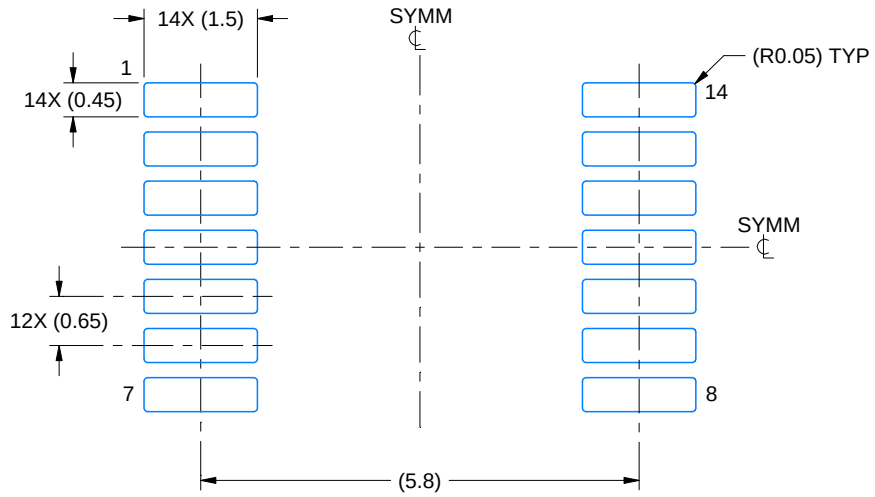
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

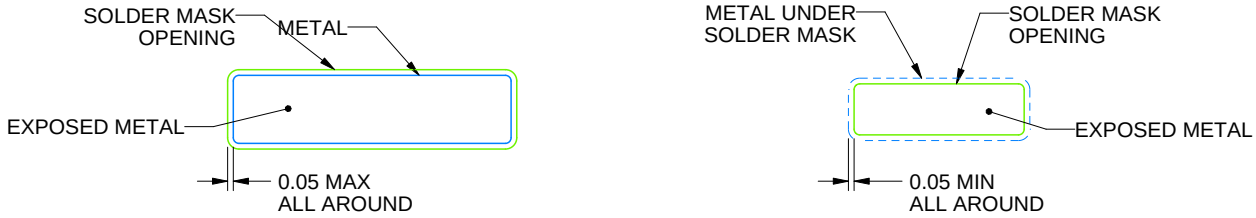



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

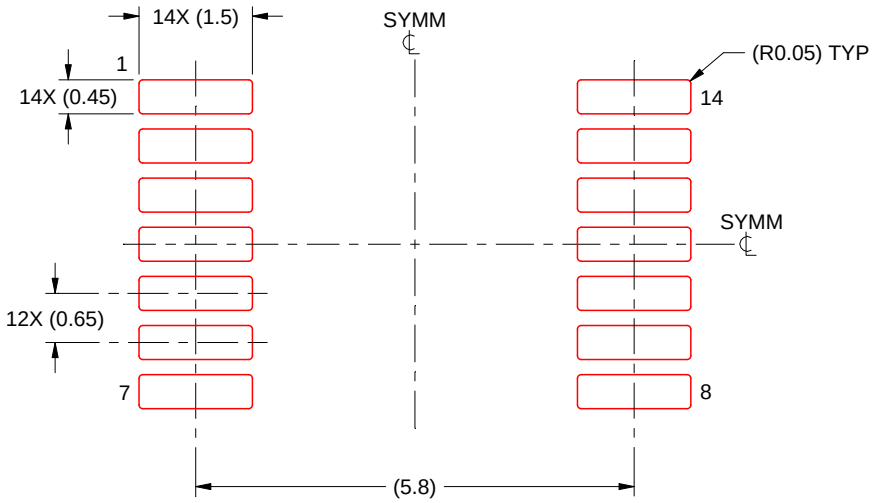



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

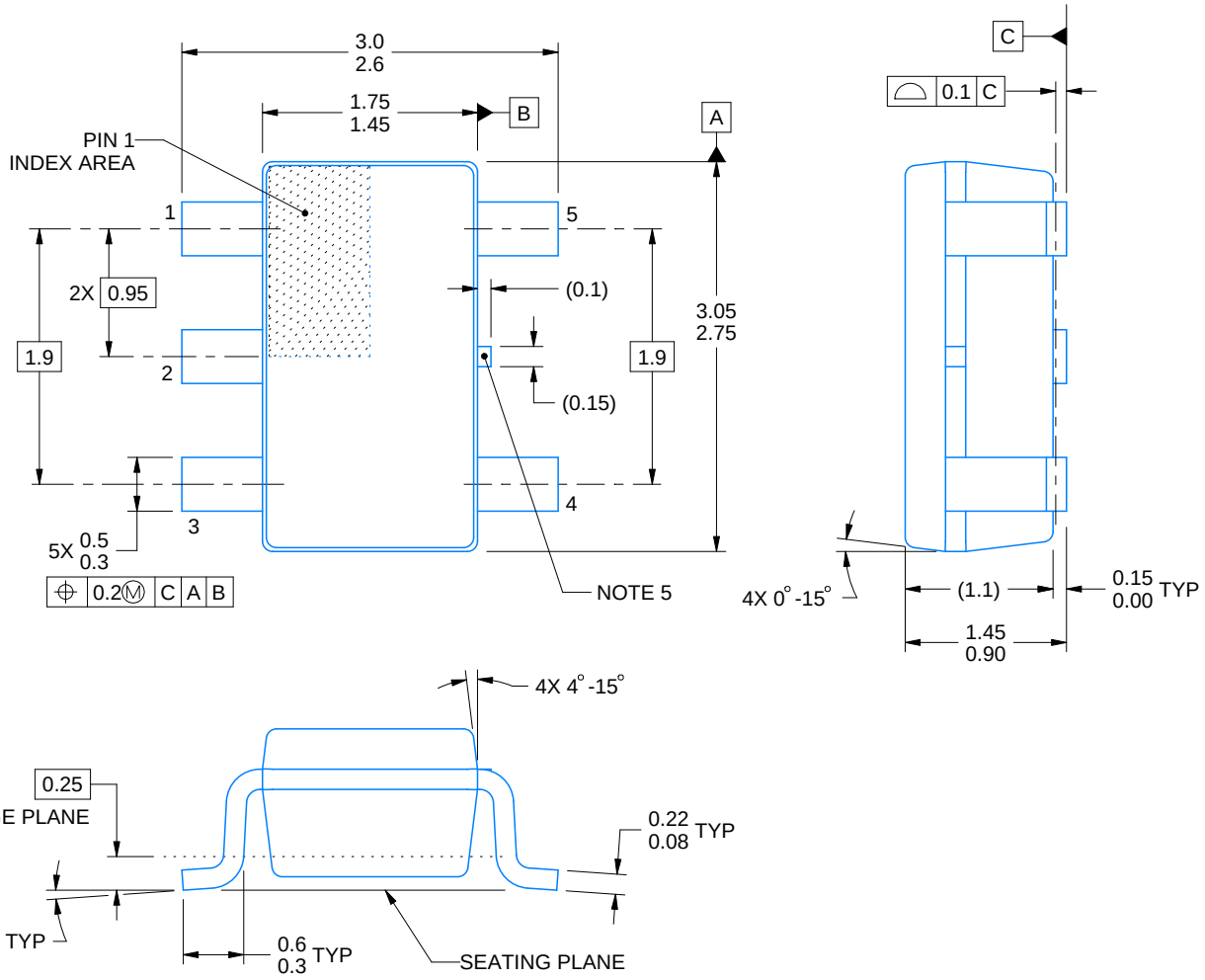
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

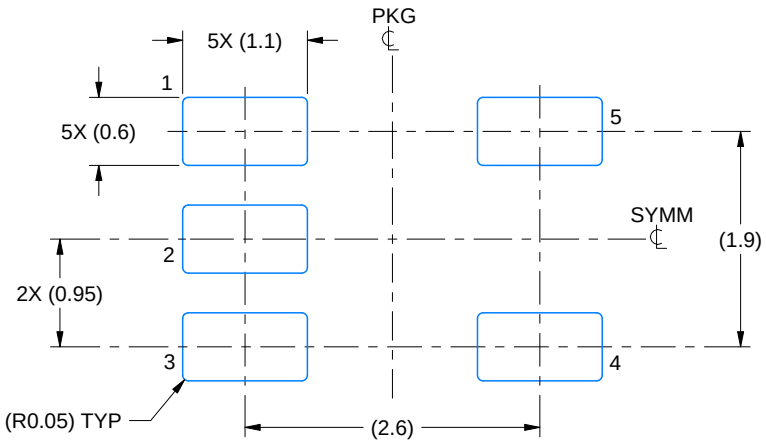
SMALL OUTLINE TRANSISTOR



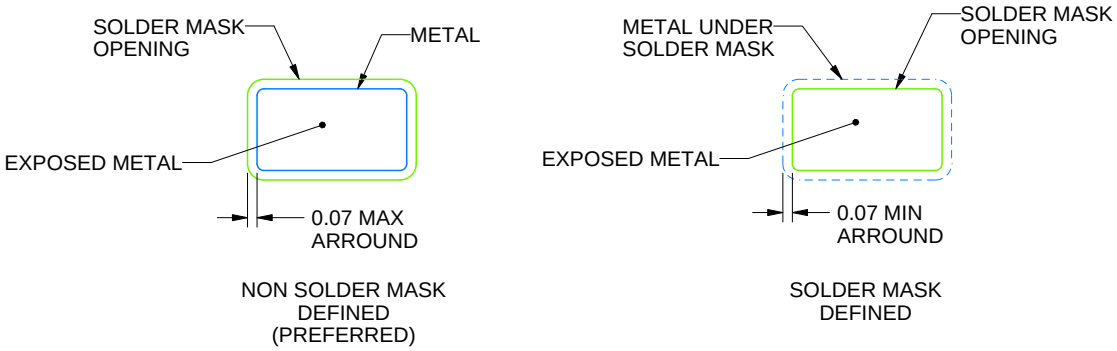

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

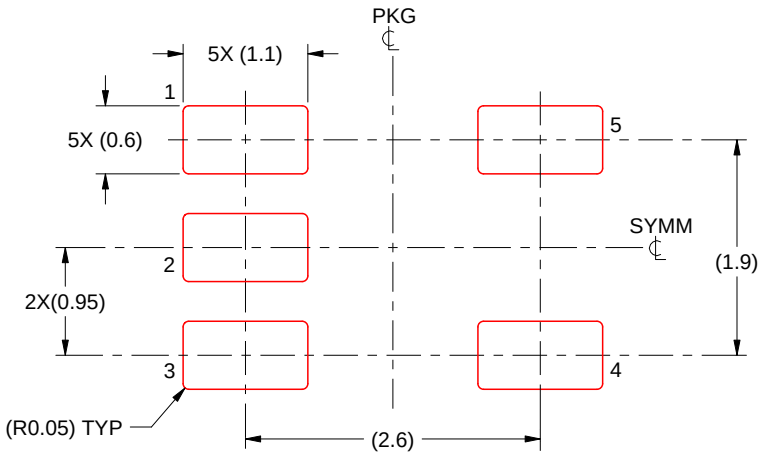



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

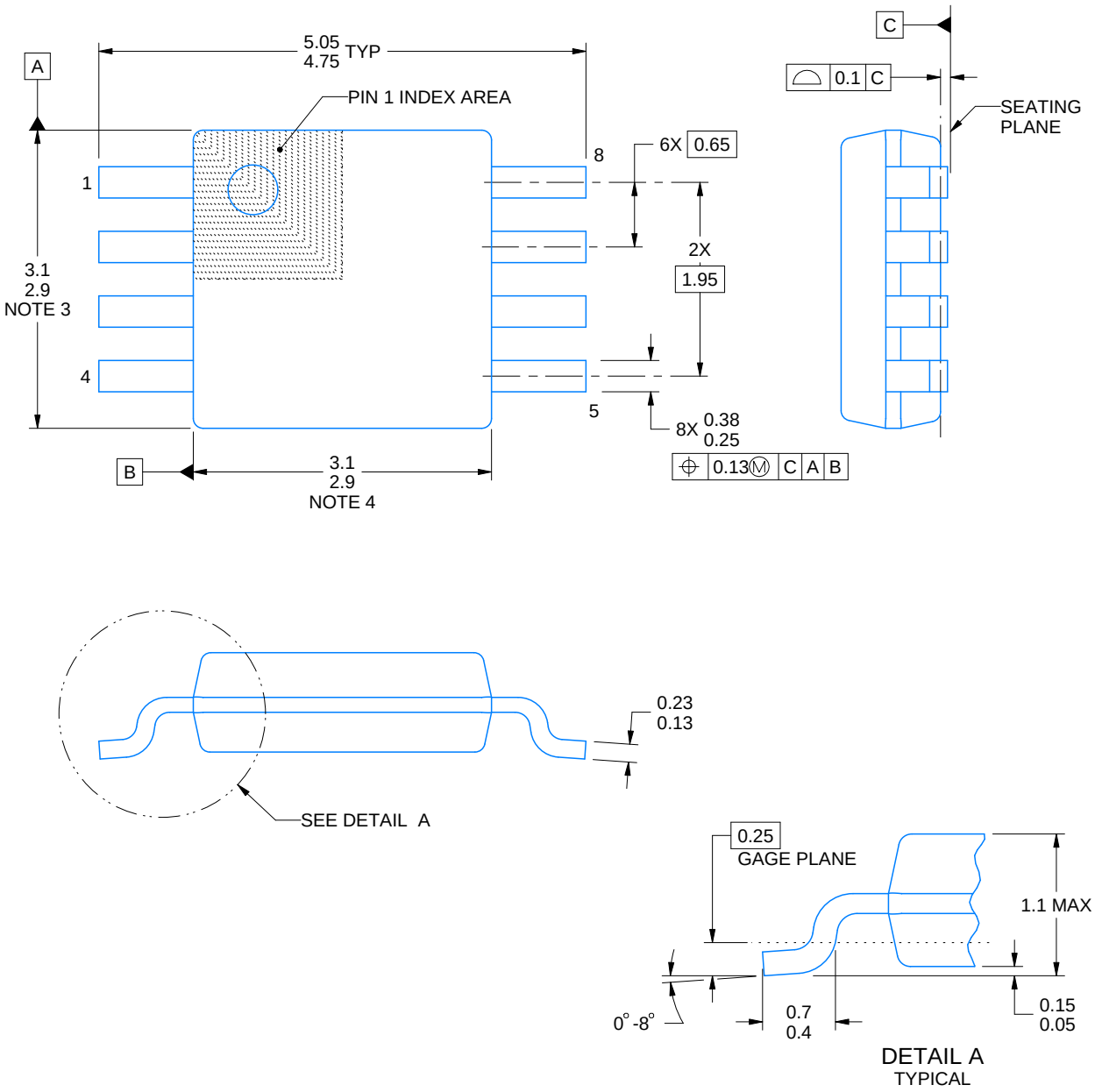
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

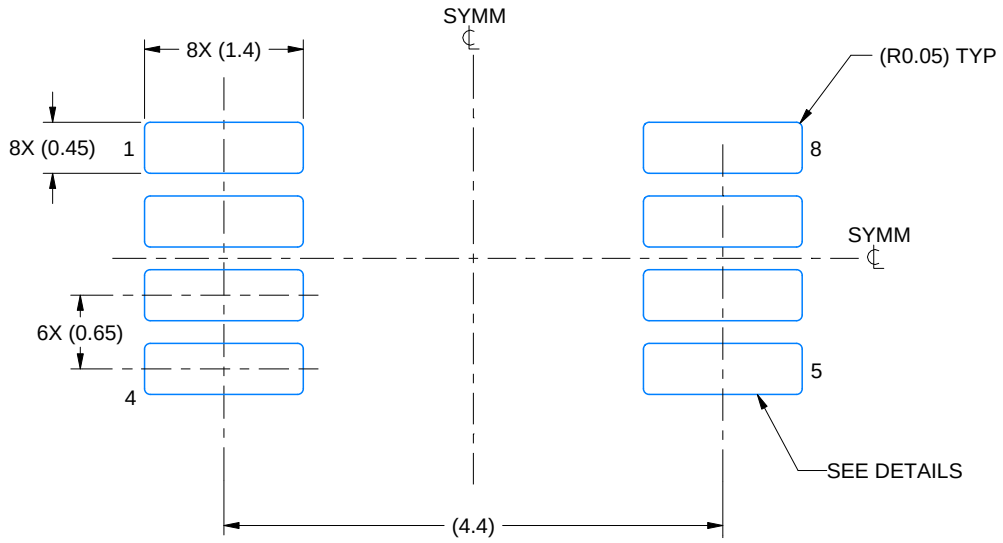
SMALL OUTLINE PACKAGE



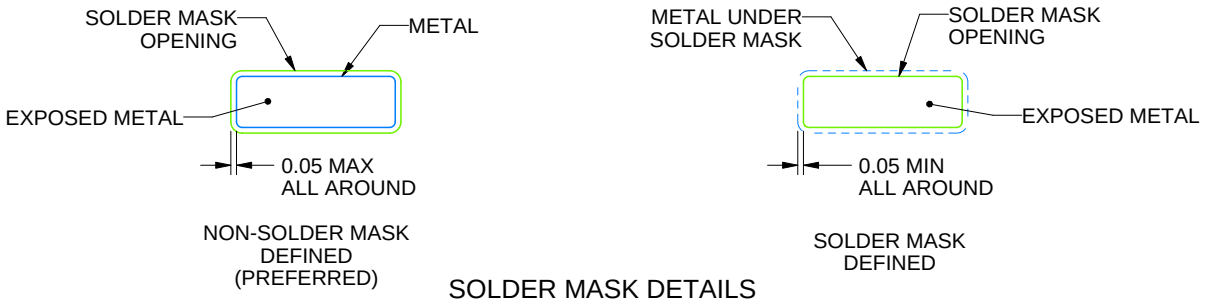

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

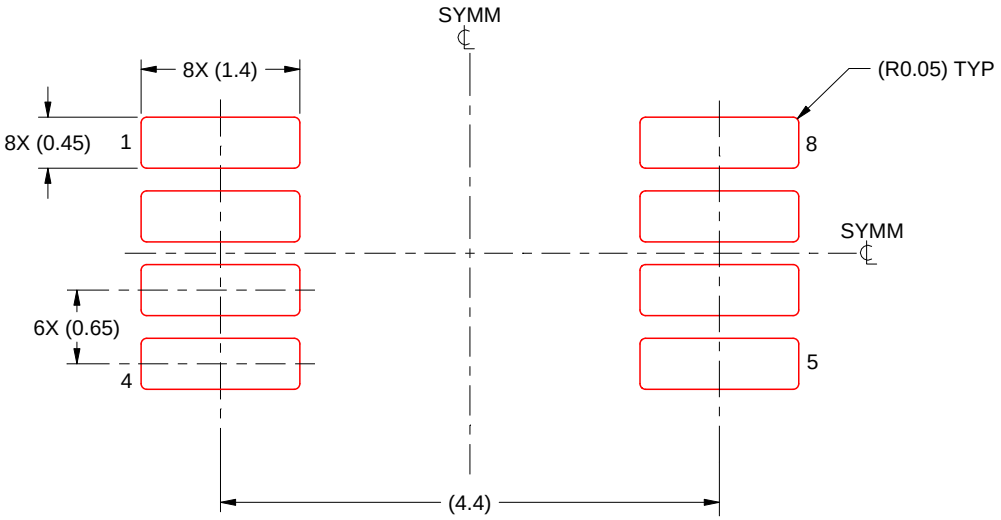



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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