LMH5401-SP radiation hardened 6.5-GHz, low-noise, low-power, gain-configurable fully differential amplifier

1 Features

- QMLV (QML class V) MIL-PRF-38535 qualified, SMD 5962R1721401VXC
  - Radiation hardness assurance (RHA) up to 100-krad(Si) total ionizing dose (TID)
  - Single event latch-up (SEL) immune to LET = 85 MeV-cm^2/mg
  - Qualified over the military temperature range (–55°C to 125°C)
- Gain bandwidth product (GBP): 6.5 GHz
- Excellent linearity performance: DC to 2 GHz
- Slew rate: 17,500 V/µs
- Low HD2, HD3 distortion (500 mV_{PP}, 100 Ω, SE-DE, Gv = 17 dB)(1):
  - 100 MHz: HD2 at –91 dBc, HD3 at –95 dBc
  - 200 MHz: HD2 at –86 dBc, HD3 at –85 dBc
  - 500 MHz: HD2 at –80 dBc, HD3 at –80 dBc
  - 1 GHz: HD2 at –53 dBc, HD3 at –70 dBc
  - 2 GHz: HD2 at –68 dBc, HD3 at –56 dBc
- Low IMD2, IMD3 distortion (1 V_{PP}, 100 Ω, SE-DE, Gv = 17 dB)(1):
  - 500 MHz: IMD2 at –90 dBc, IMD3 at –79 dBc
  - 1 GHz: IMD2 at –80 dBc, IMD3 at –61 dBc
  - 2 GHz: IMD2 at –64 dBc, IMD3 at –42 dBc
- High OIP2, OIP3. Gp = 8 dB(1)
  - 500 MHz: OIP2 at 91 dBm, OIP3 at 47.7 dBm
  - 1 GHz: OIP2 at 80 dBm, OIP3 at 37.5 dBm
- Input voltage noise: 1.25 nV/√Hz
- Input current noise: 3.5 pA/√Hz
- Supports single- and dual-supply operation
- Current consumption: 60 mA
- Power-down feature

(1) Power Gain (Gp) = 8 dB; Voltage Gain (Gv) = 17 dB; RL_{total} = 200 Ω. See *Output Reference Nodes and Gain Nomenclature* section for more details.

2 Applications

- Balun replacement: DC to 2 GHz
- GSPS ADC drivers
- DAC buffers
- IF, RF, and baseband gain blocks
- SAW filter buffers and drivers
- Level shifters
- Radiation hardened application

3 Description

The LMH5401-SP is a very high-performance, radiation hardened, differential amplifier optimized for radio frequency (RF), intermediate frequency (IF), or high-speed, dc-coupled, time-domain applications. The device is ideal for dc- or ac-coupled applications that may require a single-ended-to-differential (SE-DE) conversion when driving an analog-to-digital converter (ADC). The LMH5401-SP generates very low levels of second- and third-order distortion when operating in SE-DE or differential-to-differential (DE-DE) mode.

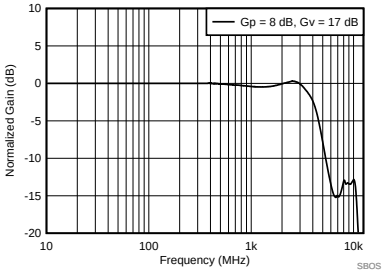
Device Information(1)

PART NUMBER	GRADE	PACKAGE
5962R1721401VXC	Radiation Hardness Assured	14-pin LCCC [FFK] 5.50 mm × 6.00 mm
5962-1721401V2C	QMLV	
LMH5401FFK\EM	Engineering Samples(2)	
LMH5401EVMCVAL	Ceramic Evaluation Board	—

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

LMH5401-SP Small Signal Frequency Response



LMH5401-SP Driving an ADC12D1620QML

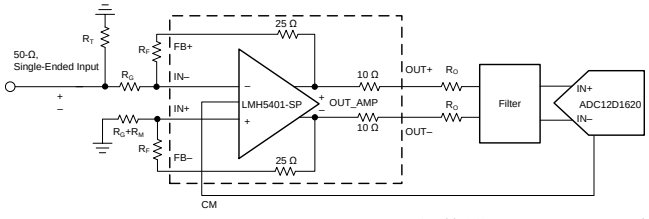


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Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Description (continued) ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics: V_S = 5 V ... 5
7.6 Electrical Characteristics: V_S = 3.3 V ... 7
7.7 Typical Characteristics: 5 V ... 10
7.8 Typical Characteristics: 3.3 V ... 16
8 Parameter Measurement Information ... 20
8.1 Output Reference Nodes and Gain Nomenclature ... 20
8.2 ATE Testing and DC Measurements ... 21
8.3 Frequency Response ... 21
8.4 S-Parameters ... 22
8.5 Frequency Response with Capacitive Load ... 22
8.6 Distortion ... 22
8.7 Noise Figure ... 22
8.8 Pulse Response, Slew Rate, and Overdrive Recovery ... 22
8.9 Power Down ... 23
8.10 V_{CM} Frequency Response ... 23
8.11 Test Schematics ... 23
9 Detailed Description ... 25
9.1 Overview ... 25
9.2 Functional Block Diagram ... 25
9.3 Feature Description ... 25
9.4 Device Functional Modes ... 31
10 Application and Implementation ... 32
10.1 Application Information ... 32
10.2 Typical Application ... 36
10.3 Do's and Don'ts ... 45
11 Power Supply Recommendations ... 46
11.1 Supply Voltage ... 46
11.2 Single Supply ... 46
11.3 Split Supply ... 46
11.4 Supply Decoupling ... 46
12 Layout ... 47
12.1 Layout Guidelines ... 47
12.2 Layout Example ... 47
13 Device and Documentation Support ... 48
13.1 Device Support ... 48
13.2 Documentation Support ... 48
13.3 Receiving Notification of Documentation Updates ... 48
13.4 Community Resources ... 48
13.5 Trademarks ... 49
13.6 Electrostatic Discharge Caution ... 49
13.7 Glossary ... 49
14 Mechanical, Packaging, and Orderable Information ... 49

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2018) to Revision B — **Page**

- Changed Figure 1 ... 10
- Added Figure 7 ... 10
- Added Figure 8 ... 10
- Added Figure 14 ... 11
- Added Figure 15 ... 11

Changes from Original (December 2017) to Revision A — **Page**

- Added RHA device ... 1
- Changed V_S = 5 V PSRR values (–44 dB, –48 dB) from MIN : to MAX ... 6
- Changed V_S = 3.3 V PSRR values (–44 dB, –48 dB) from MIN : to MAX ... 8

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5 Description (continued)

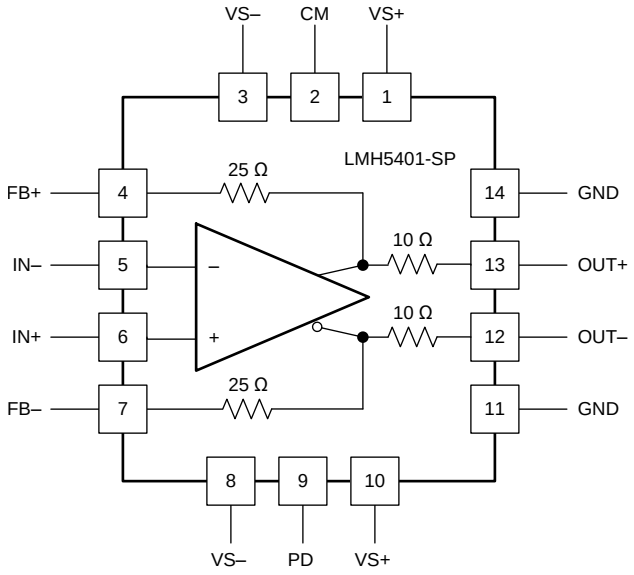
The amplifier is optimized for use in both SE-DE and DE-DE systems. The device has unprecedented usable bandwidth from dc to 2 GHz. The LMH5401-SP can be used for SE-DE conversions in the signal chain without external baluns in a wide range of applications such as test and measurement, broadband communications, and high-speed data acquisition.

A common-mode reference input pin is provided to align the amplifier output common-mode with the ADC input requirements. Power supplies between 3.3 V and 5 V can be selected and dual-supply operation is supported when required by the application. A power-down feature is also available for power savings.

This level of performance is achieved at a very low power level of 300 mW when a 5-V supply is used. The device is fabricated in Texas Instruments' advanced complementary BiCMOS process and is available in a space-saving, LCCC-14 package for higher performance.

6 Pin Configuration and Functions

FFK Package
14-Pin LCCC
Top View



Pin Functions

PIN		I/O/P[1]	DESCRIPTION
NAME	NO.		
CM	2	I	Input pin to set amplifier output common-mode voltage.
FB–	7	O	Negative output feedback component connection.
FB+	4	O	Positive output feedback component connection.
GND	11, 14	P	Printed circuit board (PCB) ground.
IN–	5	I	Negative input pin.
IN+	6	I	Positive input pin.
OUT–	12	O	Negative output pin.
OUT+	13	O	Positive output pin.
PD	9	I	Power-down (logic 1 = power down).
VS–	3, 8	P	Negative supply voltage.
VS+	1, 10	P	Positive supply voltage.

(1) I = input, O = output, P = power

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7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Power supply		5.5	V
	Input voltage	(VS–) – 0.7	(VS+) + 0.7	
Current	Input current		10	mA
	Output current (sourcing or sinking) OUT+, OUT–		100	
Continuous power dissipation		See *Thermal Information* table		
Temperature	Maximum junction temperature, T_J		150	°C
	Maximum junction temperature, continuous operation, long-term reliability		125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V_S = VS+ – VS–)	3.15	5	5.25	V
Operating junction temperature, T_J	–55		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		LMH5401-SP FFK (LCCC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	106.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	64.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	68.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	63.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics: V_S = 5 V

The specifications shown below correspond to the respectively identified subgroup temperature (see Table 1), unless otherwise noted. VS+ = 5 V; VS– = 0 V; V_{CM} = 2.5 V; RL_{total} = 200-Ω differential(1); Gp = 8 dB (Gv = 17 dB); single-ended input, differential output, and R_S = 50 Ω (unless otherwise noted)(2).

PARAMETER		TEST CONDITIONS	SUBGROUP(3)	MIN	TYP	MAX	UNIT
AC PERFORMANCE							
GBP	Gain bandwidth product	Gp = 8 dB			6.5		GHz
SSBW	Small-signal, –3-dB bandwidth	V_L = 100 mV_{PP}			4.2		GHz
LSBW	Large-signal, –3-dB bandwidth	V_L = 1.0 V_{PP}			4		GHz
	Bandwidth for ±0.5-dB flatness	V_L = 1.0 V_{PP}			2.9		GHz
SR	Slew rate	2-V step			17500		V/µs
	Rise and fall time	1-V step, 10% to 90%			80		ps
	Overdrive recovery	Overdrive = ±0.5 V			300		ps
	Output balance error	f = 1 GHz			–47		dBc
z_o	Output impedance	At dc, differential	[1, 2, 3]	13	20	25	Ω
	0.1% settling time	2 V, R_L = 200 Ω			1		ns
HD2	Second-order harmonic distortion	f = 100 MHz, V_L = 1 V_{PP}			–91		dBc
		f = 200 MHz, V_L = 1 V_{PP}			–86		
		f = 500 MHz, V_L = 1 V_{PP}			–80		
		f = 1 GHz, V_L = 1 V_{PP}			–53		
		f = 2 GHz, V_L = 1 V_{PP}			–68		
HD3	Third-order harmonic distortion	f = 100 MHz, V_L = 1 V_{PP}			–95		dBc
		f = 200 MHz, V_L = 1 V_{PP}			–85		
		f = 500 MHz, V_L = 1 V_{PP}			–80		
		f = 1 GHz, V_L = 1 V_{PP}			–70		
		f = 2 GHz, V_L = 1 V_{PP}			–56		
IMD2	Second-order intermodulation	f = 500 MHz, V_L = 1 V_{PP} per tone			–90		dBc
		f = 1 GHz, V_L = 1 V_{PP} per tone			–80		
		f = 2 GHz, V_L = 1 V_{PP} per tone			–64		
OIP2	Second-order output intercept point	f = 500 MHz, VL = 1 V_{PP}, matched load			91		dBm
		f = 1000 MHz, VL = 1 V_{PP}, matched load			80		
IMD3	Third-order intermodulation	f = 500 MHz, V_L = 0.25 V_{PP} per tone			–79		dBc
		f = 1 GHz, V_L = 0.25 V_{PP} per tone			–61		
		f = 2 GHz, V_L = 0.25 V_{PP} per tone			–42		
OIP3	Third-order output intercept point	f = 500 MHz, VL = 1 V_{PP}, unmatched load			47.7		dBm
		f = 1000 MHz, VL = 1 V_{PP}, unmatched load			37.5		
NOISE PERFORMANCE							
e_n	Input voltage noise density				1.25		nV/√Hz
i_n	Input noise current				3.5		pA/√Hz
NF	Noise figure	R_S = 50 Ω, SE-DE, 200 MHz See Figure 57			9.6		dB
INPUT							
V_{IO}	Input offset voltage		[1, 2, 3]		±0.5	±5	mV
I_{IB}	Input bias current		[1, 2, 3]		70	150	µA
I_{IO}	Input offset current		[1, 2, 3]		±1	±20	µA
	Differential resistance	Open-loop			4600		Ω
V_{ICL}	Input common-mode low voltage		[1, 2, 3]		VS–	(VS–) + 0.41	V

(1) Please see the *Output Reference Nodes and Gain Nomenclature* section.
(2) The input resistance and corresponding gain are obtained with the external resistance added.
(3) For subgroup definitions, please see Table 1.

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Electrical Characteristics: V_S = 5 V (continued)

The specifications shown below correspond to the respectively identified subgroup temperature (see Table 1), unless otherwise noted. VS+ = 5 V; VS– = 0 V; V_{CM} = 2.5 V; RL_{total} = 200-Ω differential(1); Gp = 8 dB (Gv = 17 dB); single-ended input, differential output, and R_S = 50 Ω (unless otherwise noted)(2).

PARAMETER		TEST CONDITIONS	SUBGROUP(3)	MIN	TYP	MAX	UNIT
V_{ICH}	Input common-mode high voltage		[1, 2, 3]	(VS+) – 1.41	(VS+) – 1.2		V
CMRR	Common-mode rejection ratio	Differential, 1-V_{PP} input shift, dc			72		dBc
OUTPUT							
V_{OCRH}	Output voltage range, high	Measured single-ended	[1, 2, 3]	(VS+) – 1.3	(VS+) – 1.1		V
V_{OCRL}	Output voltage range, low	Measured single-ended	[1, 2, 3]	(VS–) + 1.3	(VS–) + 1.1		V
V_{OD}	Differential output voltage swing	Differential			5.8		V_{PP}
I_{OD}	Differential output current	V_O = 0 V(4)	[1, 2, 3]	40	50		mA
POWER SUPPLY							
V_S	Supply voltage		[1, 2, 3]	3.15		5.25	V
PSRR	Power-supply rejection ratio	VS–	[1, 2, 3]		–80	–44	dB
		VS+	[1, 2, 3]		–82	–48	
I_Q	Quiescent current	PD = 0	[1, 2, 3]	46	60	78	mA
		PD = 1	[1, 2, 3]	1	3	6	
OUTPUT COMMON-MODE CONTROL PIN (V_{CM})							
SSBW	Small-signal bandwidth	V_{OCM} = 100 mV_{PP}			1.2		GHz
	V_{CM} slew rate	V_{OCM} = 500 mV_{PP}			2900		V/µs
	V_{CM} voltage range low	Differential gain shift < 1 dB	[1, 2, 3]		(VS–) + 1.4	(VS–) + 2	V
	V_{CM} voltage range high	Differential gain shift < 1 dB	[1, 2, 3]	(VS+) – 2	(VS+) – 1.4		V
	V_{CM} gain	V_{CM} = 0 V	[1, 2, 3]	0.98	1.0	1.01	V/V
	V_{OCM} output common-mode offset from V_{CM} input voltage	V_{CM} = 0 V			–27		mV
V_{OCM}	Common-mode offset voltage	Output-referred			0.4		mV
POWER DOWN (PD PIN)							
V_T	Enable or disable voltage threshold	Device powers on below 0.8 V, device powers down above 1.2 V	[1, 2, 3]	0.9	1.1	1.2	V
	Power-down quiescent current		[1, 2, 3]	1	3	6	mA
	PD bias current	PD = 2.5 V	[1, 2, 3]		10	±100	µA
	Turn-on time delay	Time to V_O = 90% of final value			10		ns
	Turn-off time delay	Time to V_O = 10% of original value			10		ns

(4) This test shorts the outputs to ground (mid supply) then sources or sinks 60 mA and measures the deviation from the initial condition.

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7.6 Electrical Characteristics: V_S = 3.3 V

The specifications shown below correspond to the respectively identified subgroup temperature (see Table 1), unless otherwise noted. VS+ = 3.3 V; VS– = 0 V; V_{CM} = 1.65 V; RL_{total} = 200-Ω differential(1); Gp = 8 dB (Gv = 17 dB); single-ended input, differential output, and input and output referenced to midsupply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section.

PARAMETER		TEST CONDITIONS	SUBGROUP(2)	MIN	TYP	MAX	UNIT
AC PERFORMANCE							
GBP	Gain bandwidth product	Gp = 8 dB			6.5		GHz
SSBW	Small-signal, –3-dB bandwidth	V_L = 100 mV_{PP}			4		GHz
LSBW	Large-signal, –3-dB bandwidth	V_L = 1 V_{PP}			3.8		GHz
	Bandwidth for ±0.5-dB flatness	V_L = 1 V_{PP}			2.6		GHz
SR	Slew rate	2-V step			17500		V/µs
	Rise and fall time	1-V step, 10% to 90%			90		ps
	Overdrive recovery	Overdrive = ±0.5 V			400		ps
	Output balance error	f = 1 GHz			–47		dBc
z_o	Output impedance	At dc	[1, 2, 3]	13	20	25	Ω
	0.1% settling time	2 V, R_L = 200 Ω			1		ns
HD2	Second-order harmonic distortion	f = 100 MHz, V_L = 500 mV_{PP}			–93		dBc
		f = 200 MHz, V_L = 500 mV_{PP}			–87		
		f = 500 MHz, V_L = 500 mV_{PP}			–75.2		
		f = 1 GHz, V_L = 500 mV_{PP}			–58		
HD3	Third-order harmonic distortion	f = 100 MHz, V_L = 500 m V_{PP}			–83		dBc
		f = 200 MHz, V_L = 500 mV_{PP}			–76		
		f = 500 MHz, V_L = 500 mV_{PP}			–59		
		f = 1 GHz, V_L = 500 mV_{PP}			–53		
IMD2	Second-order intermodulation distortion	f = 500 MHz, V_L = 0.25 V_{PP} per tone			–94		dBc
		f = 1 GHz, V_L = 0.25 V_{PP} per tone			–83		
		f = 2 GHz, V_L = 0.25 V_{PP} per tone			–68		
OIP2	Second-order output intercept point	f = 500 MHz, VL = 1 V_{PP}, matched load			70		dBm
		f = 1000 MHz, VL = 1 V_{PP}, matched load			54		
IMD3	Third-order intermodulation distortion	f = 500 MHz, V_L = 0.25 V_{PP} per tone			–74		dBc
		f = 1 GHz, V_L = 0.25 V_{PP} per tone			–63		
		f = 2 GHz, V_L = 0.25 V_{PP} per tone			–49		
OIP3	Third-order output intercept point	f = 500 MHz, VL = 1 V_{PP}, unmatched load			33		dBm
		f = 1000 MHz, VL = 1 V_{PP}, unmatched load			26.5		
NOISE PERFORMANCE							
e_n	Input voltage noise density				1.25		nV/√Hz
i_n	Input noise current				3.5		pA/√Hz
NF	Noise figure	R_S = 50 Ω, SE-DE, G = 12 dB, 200 MHz			11.9		dB
INPUT							
V_{IO}	Input offset voltage				±0.5	±5	mV
I_{IB}	Input bias current				70	150	µA
I_{IO}	Input offset current				±1	±20	µA
Z_{id}	Differential impedance				4600		Ω
V_{ICL}	Input common-mode low voltage		[1, 2, 3]		(VS–)	(VS–) + 0.41	V

(1) Please see the *Output Reference Nodes and Gain Nomenclature* section.
(2) For subgroup definitions, please see Table 1.

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Electrical Characteristics: V_S = 3.3 V (continued)

The specifications shown below correspond to the respectively identified subgroup temperature (see Table 1), unless otherwise noted. VS+ = 3.3 V; VS– = 0 V; V_{CM} = 1.65 V; RL_{total} = 200-Ω differential(1); Gp = 8 dB (Gv = 17 dB); single-ended input, differential output, and input and output referenced to midsupply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section.

PARAMETER		TEST CONDITIONS	SUBGROUP(2)	MIN	TYP	MAX	UNIT
V_{ICH}	Input common-mode high voltage		[1, 2, 3]	(VS+) – 1.41	(VS+) – 1.2		V
CMRR	Common-mode rejection ratio	Differential, 1-V_{PP} input shift, dc			–72		dBc
OUTPUT							
V_{OCRH}	Output voltage range, high	Measured single-ended	[1, 2, 3]	(VS+) – 1.3	(VS+) – 1.1		V
V_{OCRL}	Output voltage range, low	Measured single-ended	[1, 2, 3]	(VS–) + 1.3	(VS–) + 1.1		V
V_{OD}	Differential output voltage swing	Differential			2.8		V_{PP}
I_{OD}	Differential output current	V_O = 0 V(3)	[1, 2, 3]	30	40		mA
POWER SUPPLY							
V_S	Supply voltage		[1, 2, 3]	3.15		5.25	V
PSRR	Power-supply rejection ratio	VS–	[1, 2, 3]		–80	–44	dB
		VS+	[1, 2, 3]		–84	–48	
I_Q	Quiescent current	PD = 0	[1, 2, 3]	44	54	63	mA
		PD = 1	[1, 2, 3]	1	1.6	5	
OUTPUT COMMON-MODE CONTROL PIN (V_{CM})							
SSBW	Small-signal bandwidth	V_{OCM} = 200 mV_{PP}			3		GHz
	V_{CM} voltage range low	Differential gain shift < 1 dB	[1, 2, 3]		(VS–) + 1.35	(VS–) + 1.55	V
	V_{CM} voltage range high	Differential gain shift < 1 dB	[1, 2, 3]	(VS+) – 1.55	(VS+) – 1.35		V
	V_{CM} gain	V_{CM} = 0 V	[1, 2, 3]	0.98	1	1.01	V/V
	V_{OCM} output common-mode offset from V_{CM} input voltage	V_{CM} = 0 V			–27		mV
V_{OCM}	Common-mode offset voltage	Output-referred			0.4		mV
POWER DOWN (PD PIN)							
V_T	Enable or disable voltage threshold	Device powers on below 0.8 V, device powers down above 1.2 V	[1, 2, 3]	0.9	1.1	1.2	V
	Power-down quiescent current		[1, 2, 3]	1	1.6	6	mA
	PD bias current	PD = 2.5 V	[1, 2, 3]		10	±100	µA
	Turn-on time delay	Time to V_O = 90% of final value			10		ns
	Turn-off time delay	Time to V_O = 10% of original value			10		ns

(3) This test shorts the outputs to ground (mid supply) then sources or sinks 60 mA and measures the deviation from the initial condition.

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Table 1. Quality Conformance Inspection(1)

SUBGROUP	DESCRIPTION	TEMPERATURE (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

(1) MIL-STD-883, Method 5005 - Group A

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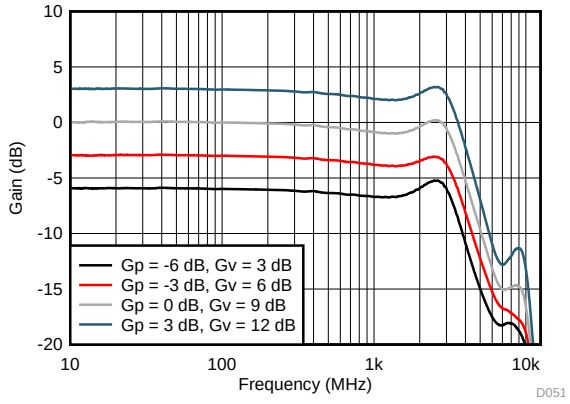
7.7 Typical Characteristics: 5 V

at T_A = 25°C, VS+ = 5 V; VS– = 0 V; V_{CM} = 2.5 V, RL_{total} = 200-Ω differential(1) (R_O = 40 Ω each), Gp = 8 dB (Gv = 17 dB), single-ended input and differential output, and input and output pins referenced to mid supply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 54 to Figure 57)



See *Stability, Noise Gain, and Signal Gain* for more details

Figure 1. SE-DE Small Signal Frequency Response for Low Gain

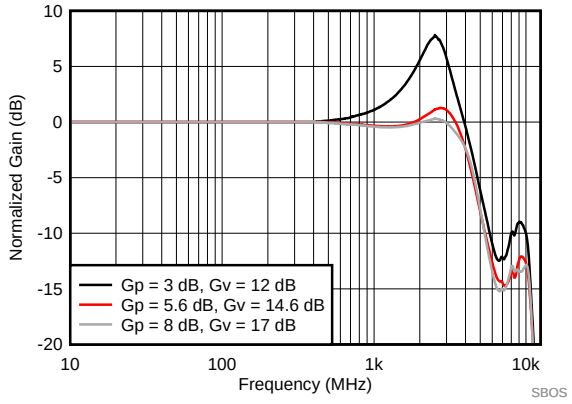


Figure 2. SE-DE Small Signal Frequency Response vs Gain

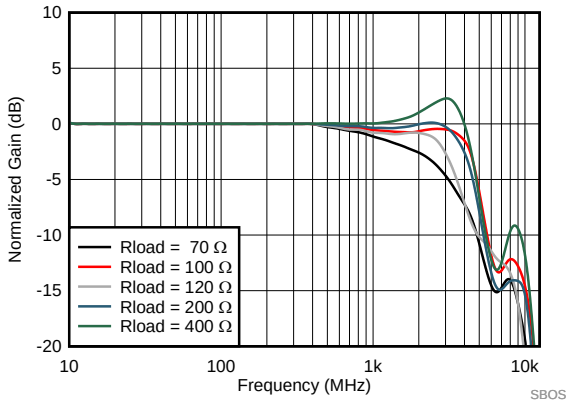


Figure 3. SE-DE Small Signal Frequency Response vs Rload

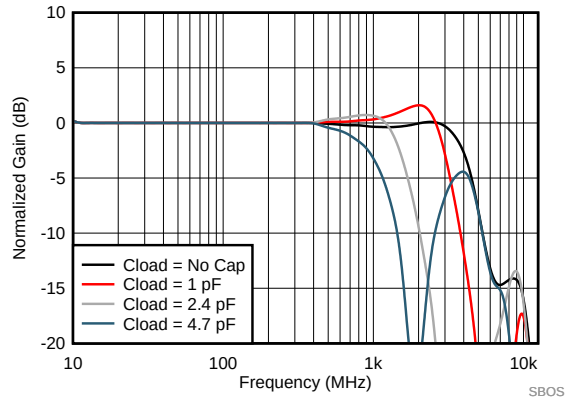


Figure 4. SE-DE Small Signal Frequency Response vs Cload

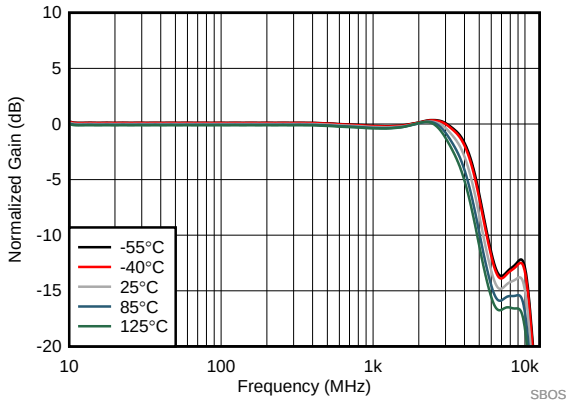


Figure 5. SE-DE Small Signal Frequency Response vs Temperature

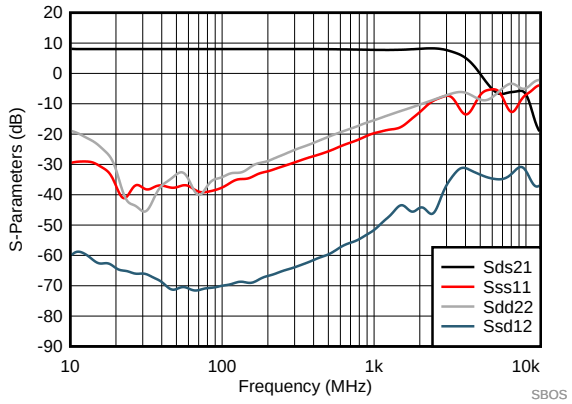


Figure 6. SE-DE Small Signal S-Parameters

(1) Please see the *Output Reference Nodes and Gain Nomenclature* section.

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Typical Characteristics: 5 V (continued)

at T_A = 25°C, VS+ = 5 V; VS– = 0 V; V_{CM} = 2.5 V, RL_{total} = 200-Ω differential() (R_O = 40 Ω each), Gp = 8 dB (Gv = 17 dB), single-ended input and differential output, and input and output pins referenced to mid supply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 54 to Figure 57)

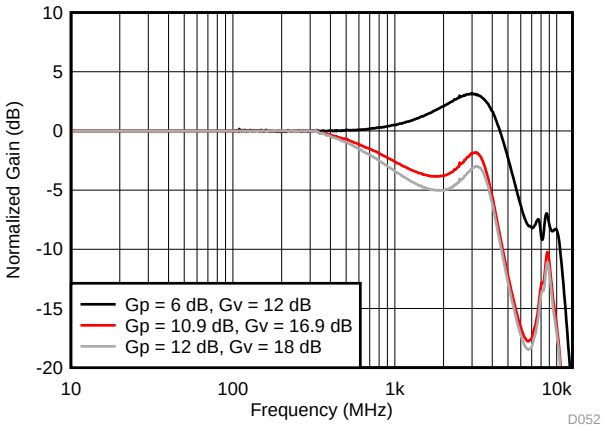

Figure 7. DIFF-DIFF Small Signal Frequency Response vs Gain

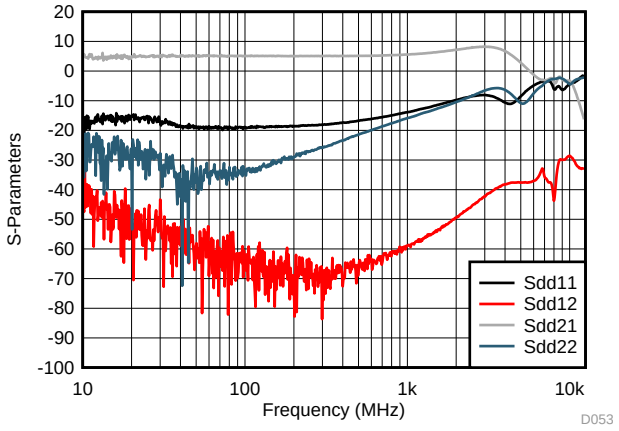

Figure 8. DIFF-DIFF Small Signal S-Parameters

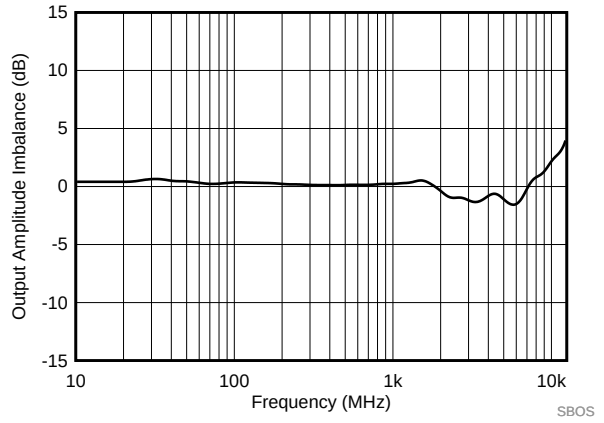

Figure 9. SE-DE Amplitude Imbalance

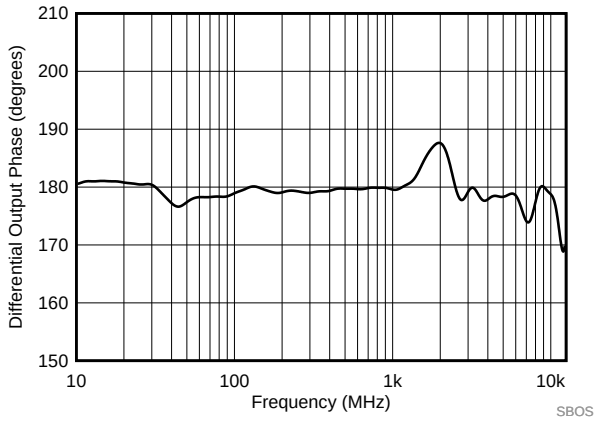

Figure 10. SE-DE Phase Imbalance

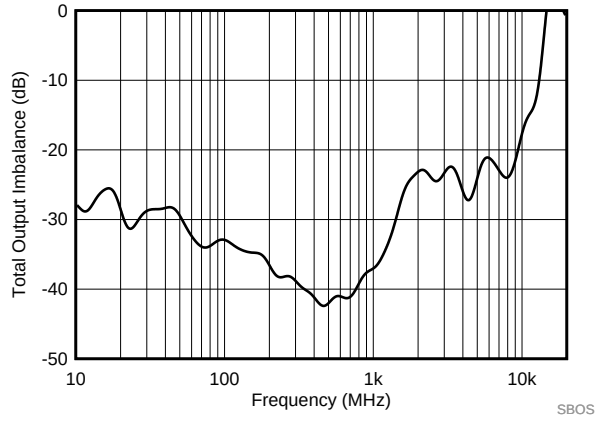

Figure 11. SE-DE Total Imbalance

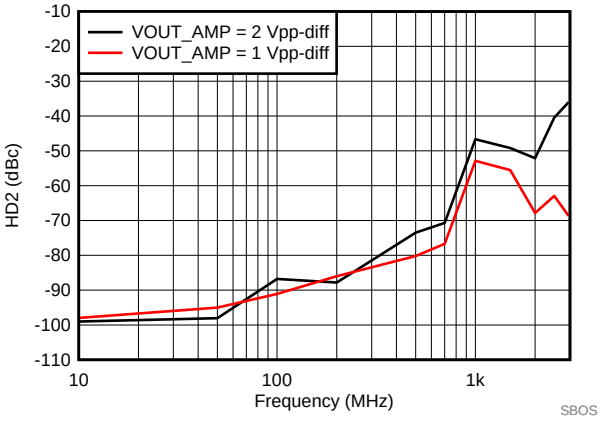

Figure 12. SE-DE 2nd Order Harmonic Distortion vs Frequency

Typical Characteristics: 5 V (continued)

at T_A = 25°C, VS+ = 5 V; VS– = 0 V; V_{CM} = 2.5 V, RL_{total} = 200-Ω differential() (R_O = 40 Ω each), Gp = 8 dB (Gv = 17 dB), single-ended input and differential output, and input and output pins referenced to mid supply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 54 to Figure 57)

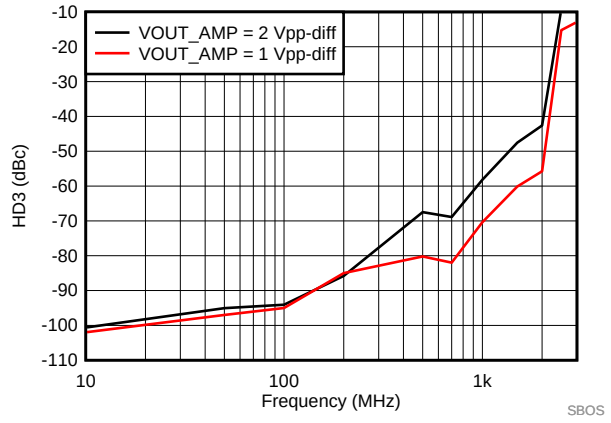

Figure 13. SE-DE 3rd Order Harmonic Distortion vs Frequency

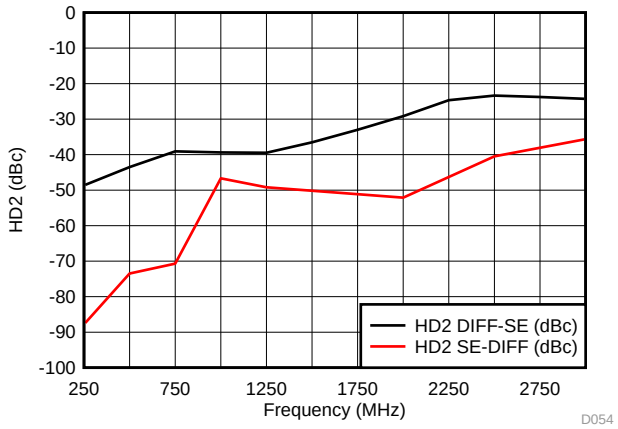

Figure 14. DE-SE 2nd Order Harmonic Distortion vs Frequency

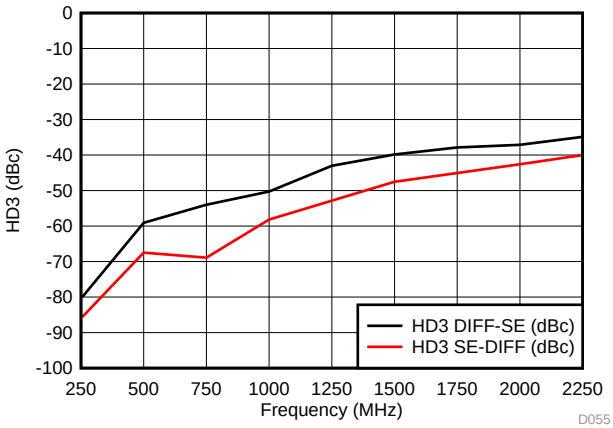

Figure 15. DE-SE 3rd Order Harmonic Distortion vs Frequency

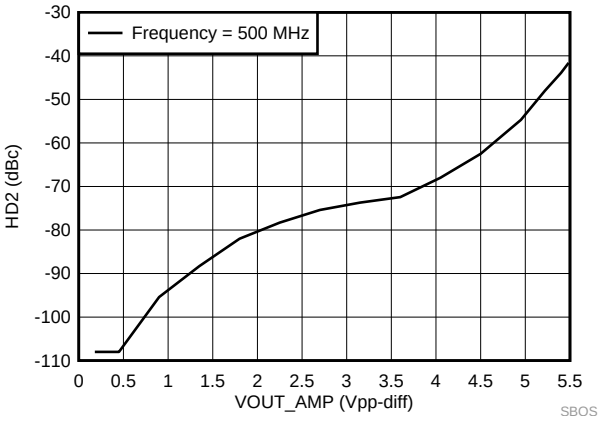

Figure 16. SE-DE 2nd Order Harmonic Distortion vs Vout

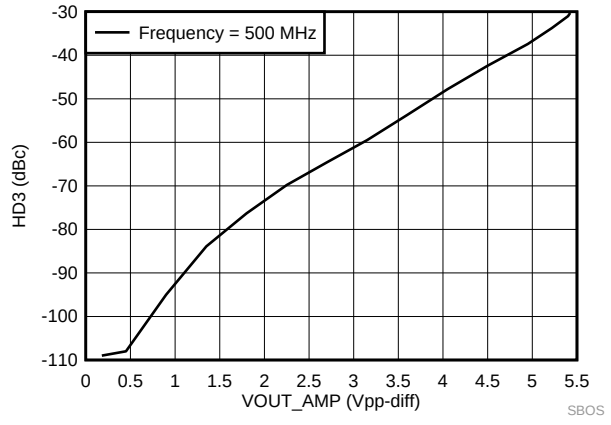

Figure 17. SE-DE 3rd Order Harmonic Distortion vs Vout

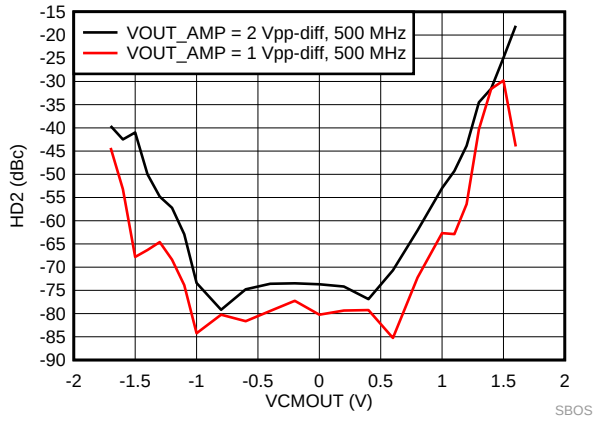

Figure 18. SE-DE 2nd Order Harmonic Distortion vs Output Common Mode Voltage

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Typical Characteristics: 5 V (continued)

at T_A = 25°C, VS+ = 5 V; VS– = 0 V; V_{CM} = 2.5 V, RL_{total} = 200-Ω differential() (R_O = 40 Ω each), Gp = 8 dB (Gv = 17 dB), single-ended input and differential output, and input and output pins referenced to mid supply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 54 to Figure 57)

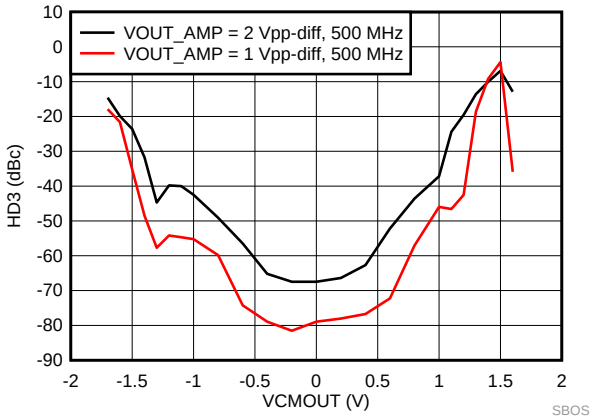


Figure 19. SE-DE 3rd Order Harmonic Distortion vs Output Common Mode Voltage

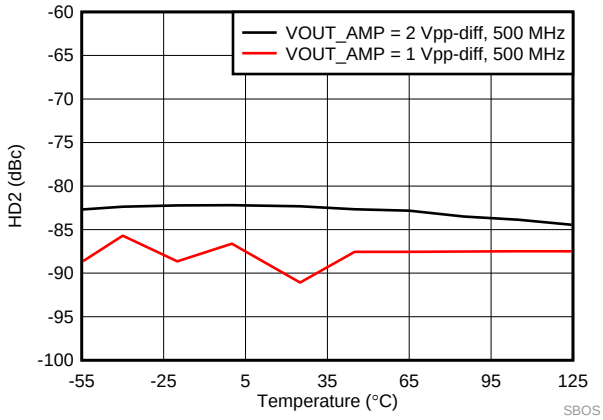


Figure 20. SE-DE 2nd Order Harmonic Distortion vs Temperature

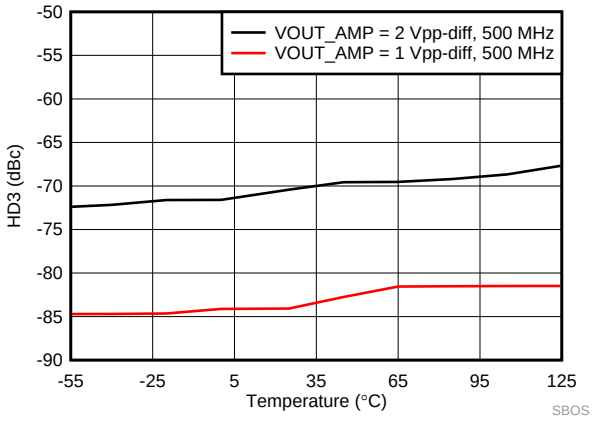


Figure 21. SE-DE 3rd Order Harmonic Distortion vs Temperature

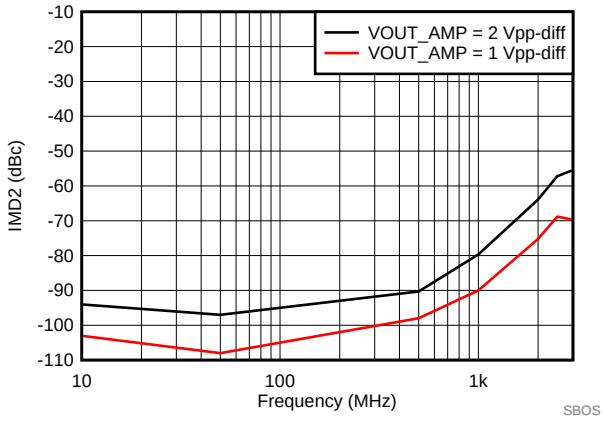


Figure 22. SE-DE 2nd Order Intermodulation Distortion vs Frequency

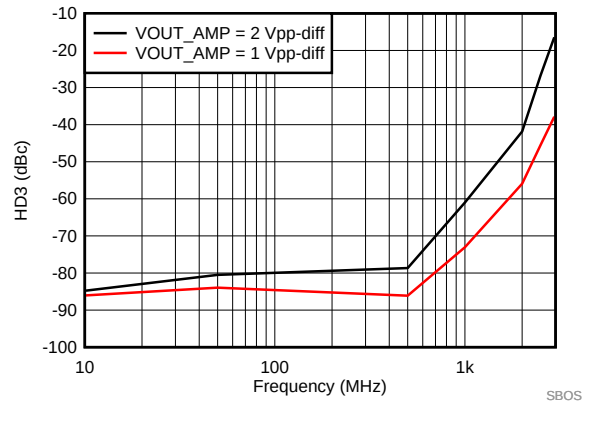


Figure 23. SE-DE 3rd Order Intermodulation Distortion vs Frequency

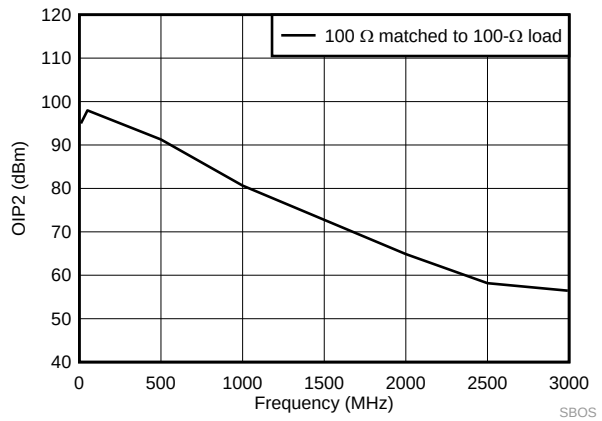
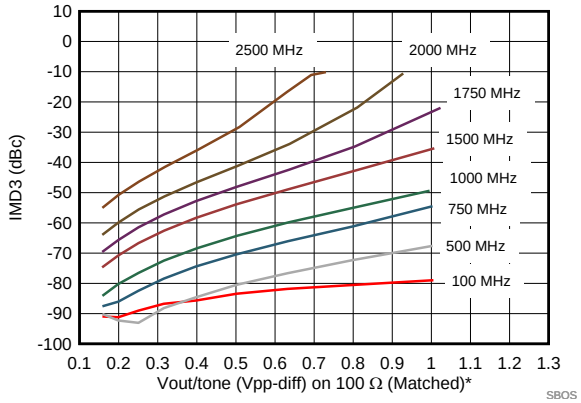


Figure 24. SE-DE Output 2nd Order Intercept Point

Typical Characteristics: 5 V (continued)

at T_A = 25°C, VS+ = 5 V; VS– = 0 V; V_{CM} = 2.5 V, RL_{total} = 200-Ω differential() (R_O = 40 Ω each), Gp = 8 dB (Gv = 17 dB), single-ended input and differential output, and input and output pins referenced to mid supply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 54 to Figure 57)



*See *Output Reference Nodes and Gain Nomenclature* for more details

Figure 25. SE-DE 3rd Order Intermodulation Distortion vs Vout (Matched Load)

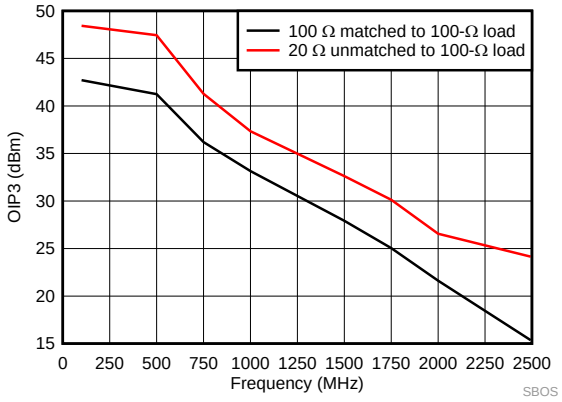
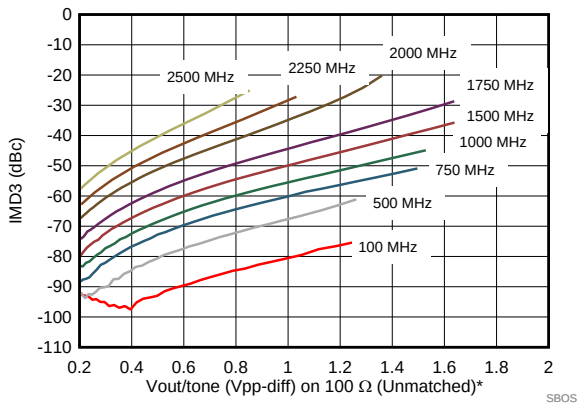


Figure 26. SE-DE Output 3rd Order Intercept Point



*See *Output Reference Nodes and Gain Nomenclature* for more details

Figure 27. SE-DE 3rd Order Intermodulation Distortion vs Vout (Unmatched Load)

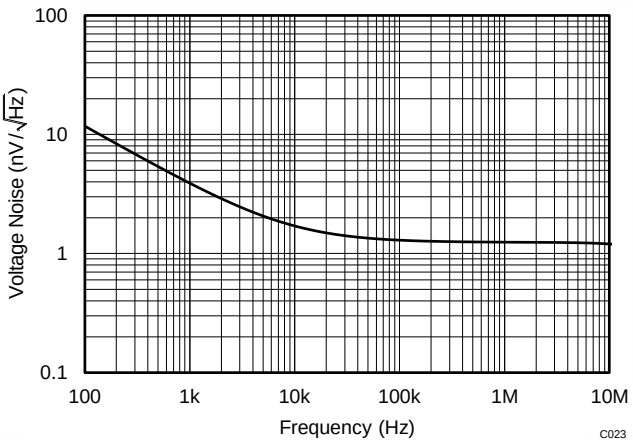


Figure 28. Input-Referred Voltage Noise

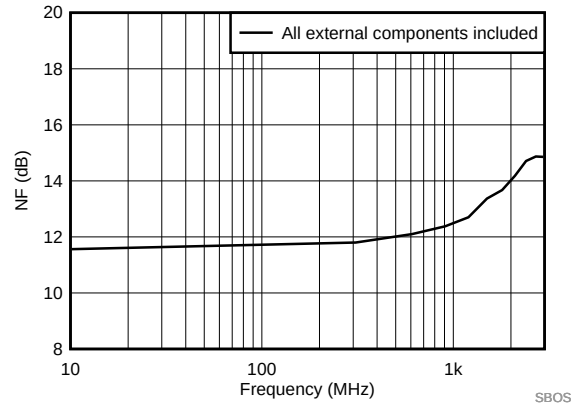


Figure 29. SE-DE Noise Figure vs Frequency

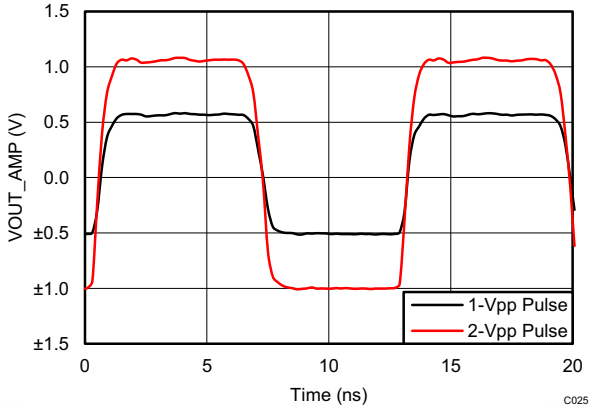


Figure 30. SE-DE Output Signal Pulse Response

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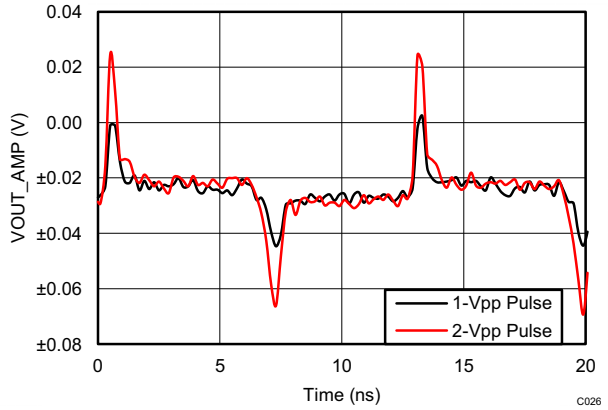
Typical Characteristics: 5 V (continued)

at T_A = 25°C, VS+ = 5 V; VS– = 0 V; V_{CM} = 2.5 V, RL_{total} = 200-Ω differential() (R_O = 40 Ω each), Gp = 8 dB (Gv = 17 dB), single-ended input and differential output, and input and output pins referenced to mid supply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 54 to Figure 57)



VCM @ AMPOUT Node; VCM = (Vo+ + Vo–) / 2

Figure 31. SE-DE Output Common Mode Pulse Response

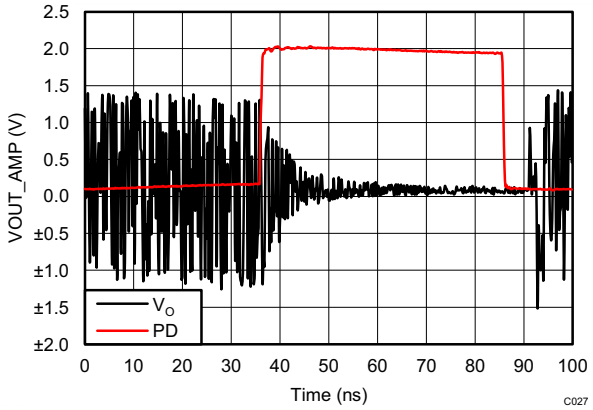


Figure 32. Power Down Timing

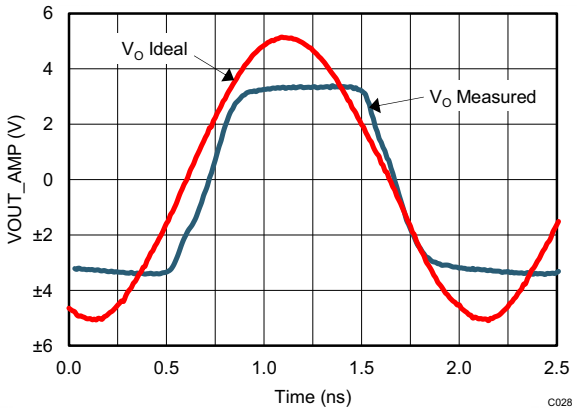


Figure 33. Overdrive Recovery

7.8 Typical Characteristics: 3.3 V

at T_A = 25°C, VS+ = 3.3 V; VS– = 0 V; V_{CM} = 1.65 V, RL_{total} = 200-Ω differential(1) (R_O = 40 Ω each), Gp = 8 dB (Gv = 17 dB), single-ended input and differential output, and input and output pins referenced to midsupply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 54 to Figure 57)

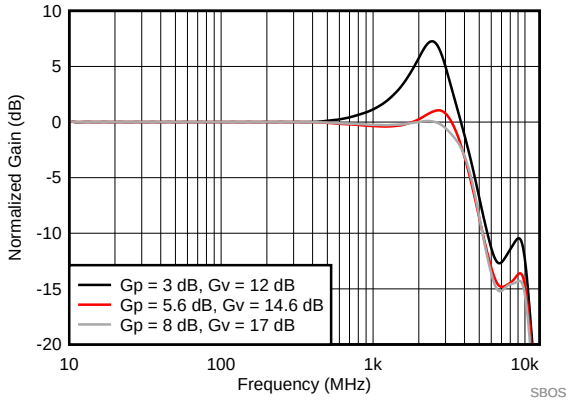


Figure 34. SE-DE Small Signal Frequency Response vs Gain

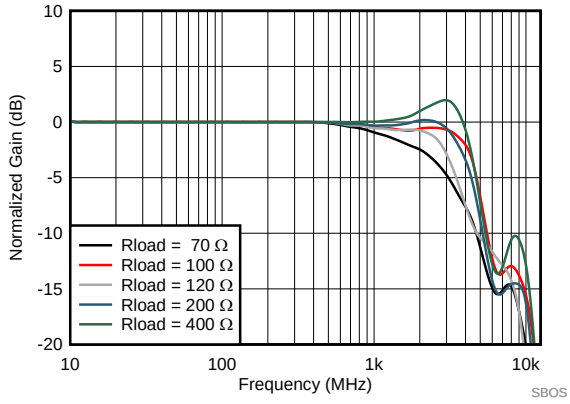


Figure 35. SE-DE Small Signal Frequency Response vs Rload

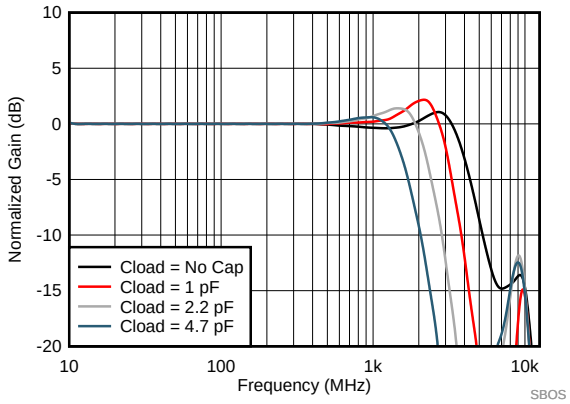


Figure 36. SE-DE Small Signal Frequency Response vs Cload

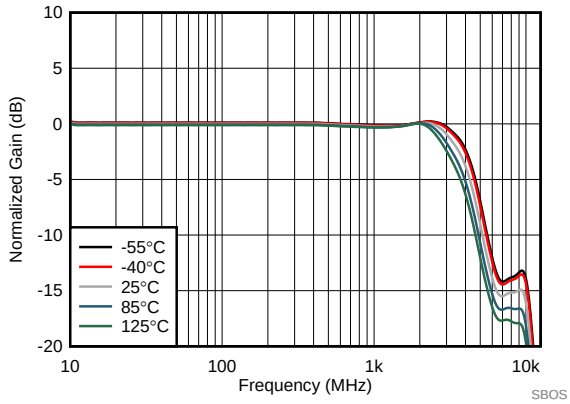


Figure 37. SE-DE Small Signal Frequency Response vs Temperature

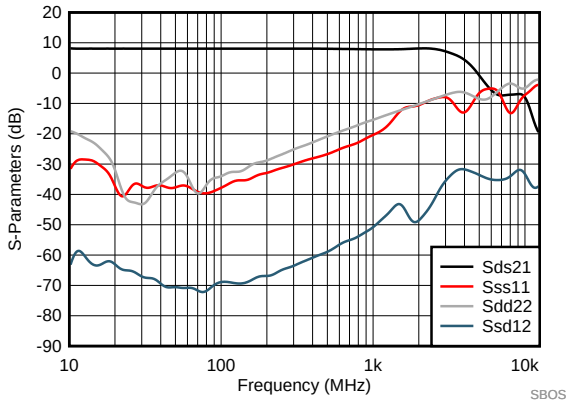


Figure 38. SE-DE Small Signal S-Parameters

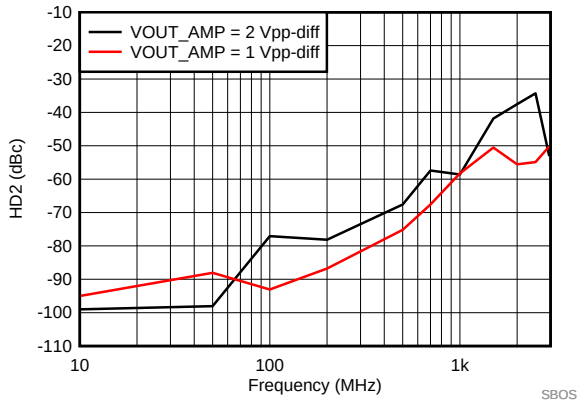


Figure 39. SE-DE 2nd Order Harmonic Distortion vs Frequency

(1) Please see the *Output Reference Nodes and Gain Nomenclature* section.

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Typical Characteristics: 3.3 V (continued)

at T_A = 25°C, VS+ = 3.3 V; VS– = 0 V; V_{CM} = 1.65 V, RL_{total} = 200-Ω differential[0] (R_O = 40 Ω each), Gp = 8 dB (Gv = 17 dB), single-ended input and differential output, and input and output pins referenced to midsupply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 54 to Figure 57)

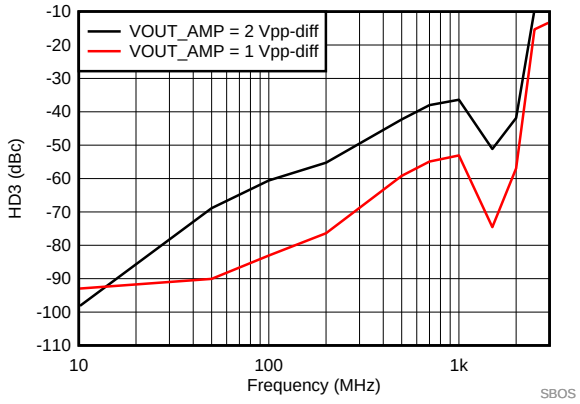
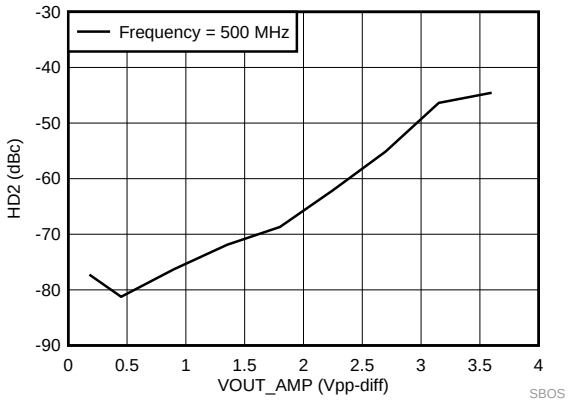
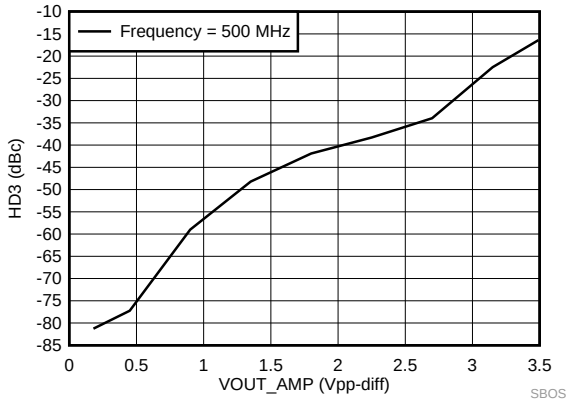


Figure 40. SE-DE 3rd Order Harmonic Distortion vs Frequency



Vout = pk-pk voltage swing per tone on 100-Ω effective load

Figure 41. SE-DE 2nd Order Harmonic Distortion vs Vout



Vout = pk-pk voltage swing per tone on 100-Ω effective load

Figure 42. SE-DE 3rd Order Harmonic Distortion vs Vout

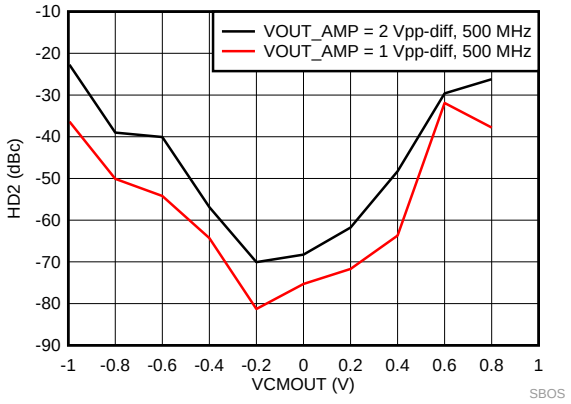


Figure 43. SE-DE 2nd Order Harmonic Distortion vs Output Common Mode Voltage

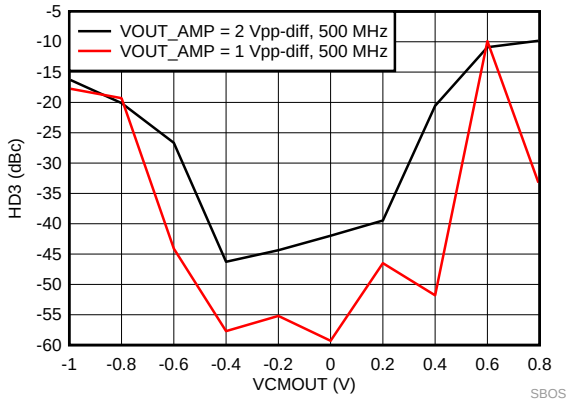


Figure 44. SE-DE 3rd Order Harmonic Distortion vs Output Common Mode Voltage

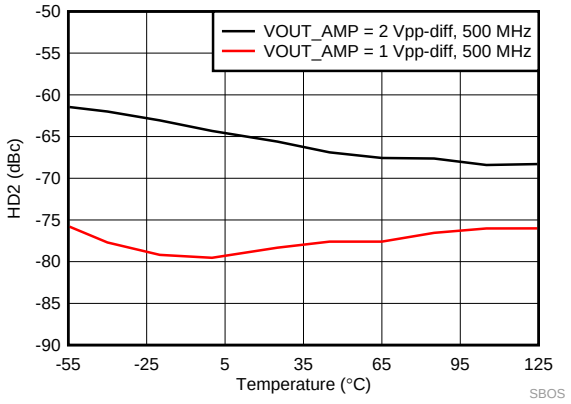


Figure 45. SE-DE 2nd Order Harmonic Distortion vs Temperature

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Typical Characteristics: 3.3 V (continued)

at T_A = 25°C, VS+ = 3.3 V; VS– = 0 V; V_{CM} = 1.65 V, RL_{total} = 200-Ω differential[0] (R_O = 40 Ω each), Gp = 8 dB (Gv = 17 dB), single-ended input and differential output, and input and output pins referenced to midsupply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 54 to Figure 57)

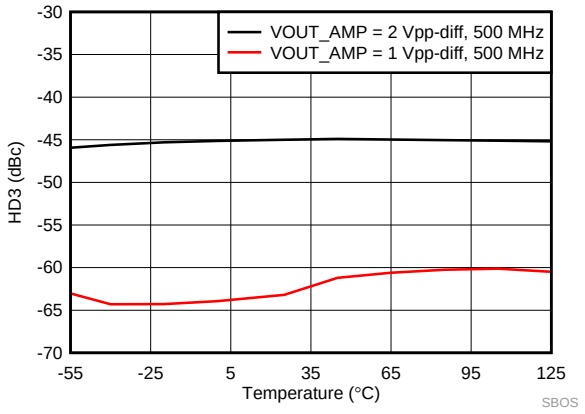

Figure 46. SE-DE 3rd Order Harmonic Distortion vs Temperature

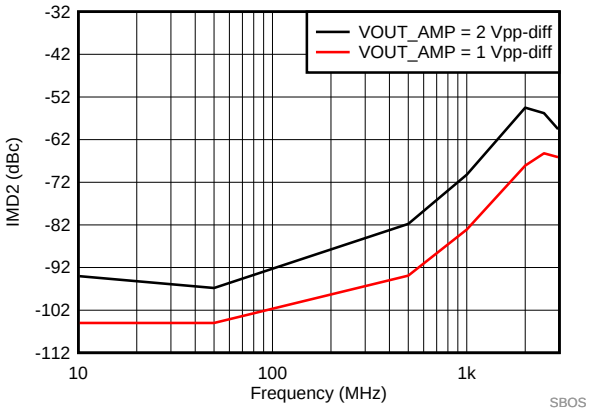

Figure 47. SE-DE 2nd Order Intermodulation Distortion vs Frequency

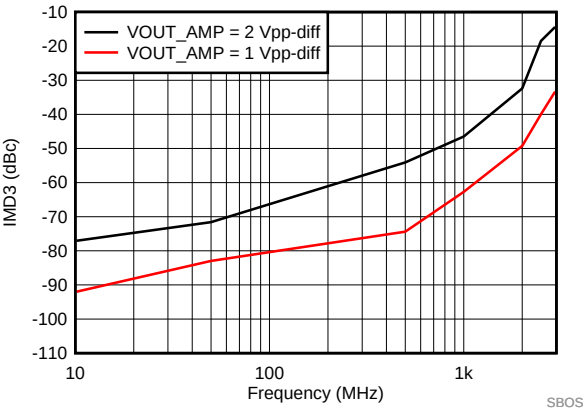

Figure 48. SE-DE 3rd Order Intermodulation Distortion vs Frequency

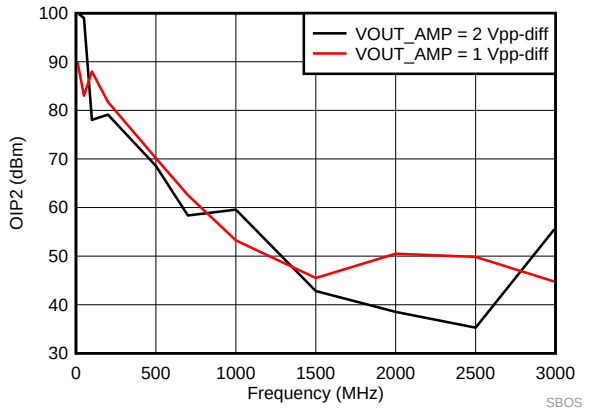

Figure 49. SE-DE Output 2nd Order Intercept Point

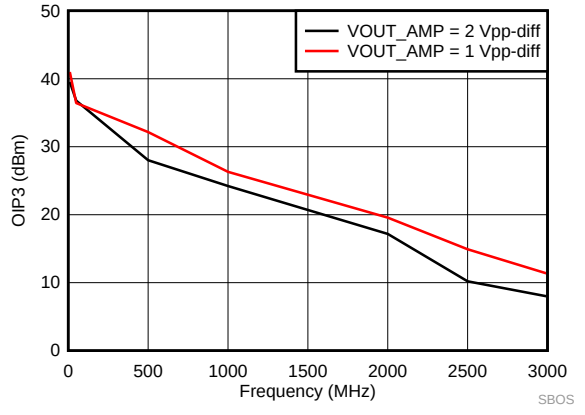

Figure 50. SE-DE Output 3rd Order Intercept Point

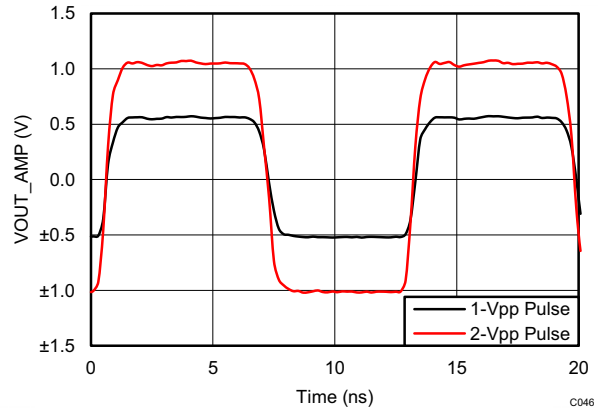

Figure 51. SE-DE Output Signal Pulse Response

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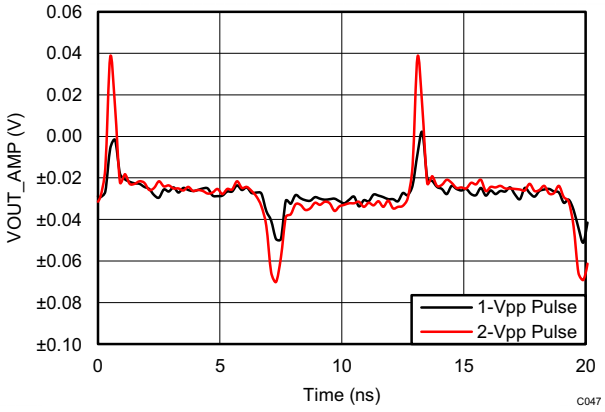
Typical Characteristics: 3.3 V (continued)

at T_A = 25°C, VS+ = 3.3 V; VS– = 0 V; V_{CM} = 1.65 V, RL_{total} = 200-Ω differential[0] (R_O = 40 Ω each), Gp = 8 dB (Gv = 17 dB), single-ended input and differential output, and input and output pins referenced to midsupply (unless otherwise noted); measured using an EVM as discussed in the *Parameter Measurement Information* section (see Figure 54 to Figure 57)



VCM @ AMPOUT Node; VCM = (Vo+ + Vo–) / 2

Figure 52. SE-DE Output Common Mode Pulse Response

8 Parameter Measurement Information

8.1 Output Reference Nodes and Gain Nomenclature

The LMH5401-SP is a decompensated, fully-differential amplifier (FDA) configurable with external resistors for noise gain greater than 4 V/V or 12 dB (GBP = 6.5 GHz). For most of this document, data are collected for Gv = 17 dB for both single-ended-to-differential (SE-DE) and differential-to-differential (DE-DE) conversions in the diagrams illustrated in the *Test Schematics* section. When matching the output to a 100-Ω load, the evaluation module (EVM) uses external 40-Ω resistors to complete the output matching, as the device has an internal series 10 Ω on each output. Having on-chip output resistors creates two potential reference points for measuring the output voltage. The amplifier output pins create one output reference point (OUT_AMP). The other output reference point is OUT_LOAD at the 100-Ω load impedance, RL. These points are illustrated in Figure 53; see also the *Test Schematics* section.

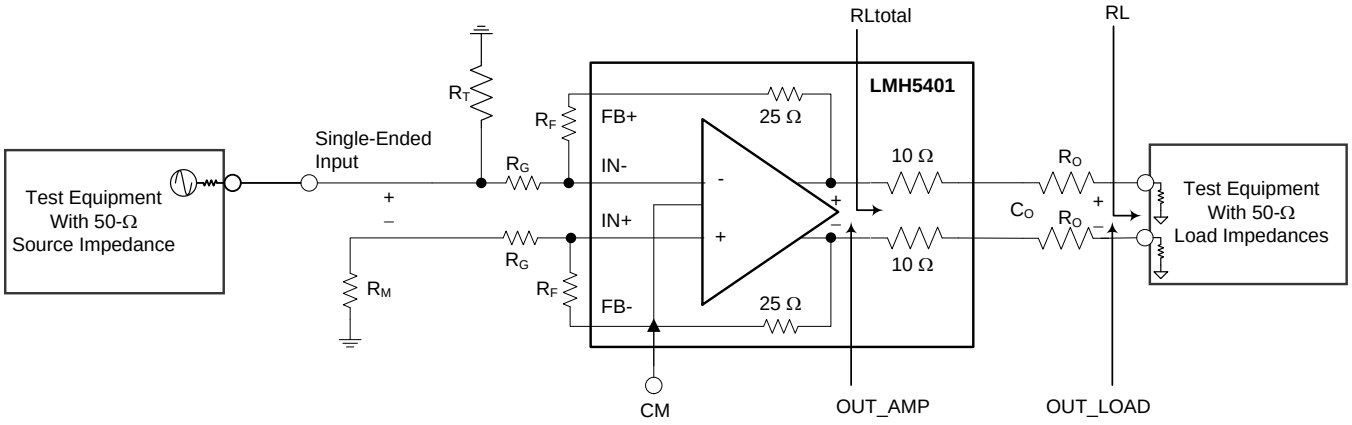


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Figure 53. Output Reference Nodes

Most measurements in the *Electrical Characteristics* tables and in the *Typical Characteristics* sections are measured with reference to the OUT_AMP reference point. Equation 1 shows that the conversion between reference points is a straightforward reduction of 3 dB for power and 6 dB for voltage in a matched condition when Ro is set such that 20 Ω + 2 × Ro = RL. With Ro set to 40 Ω and RL set to 100 Ω-differential, the total load impedance seen by the amplifier, RL_{total}, is 200 Ω. This is considered a matched load condition as 100-Ω is driving RL of 100 Ω. The device is also capable of driving lower impedances. By setting Ro to 0 Ω, RL_{total} becomes 120 Ω. This is considered an unmatched condition since 20 Ω is driving RL of 100 Ω. As explained in the *Application Curves* section, efficiency is improved (losses reduced) in a mismatched condition which is acceptable if transmission line reflections are avoided and proper termination practices are employed. As stated previously, most measurements in this document are referenced to OUT_AMP node. However, there are some typical characteristic plots that are measured with a fixed signal swing with respect to the OUT_LOAD reference point; specifically, IMD3 Figure 25 and Figure 27 are referenced to the voltage swing at node OUT_LOAD.

VOUT_LOAD = (VOUT_AMP – 6 dB) and POUT_LOAD = (POUT_AMP – 6 dB) (1)

This document makes references to both voltage gain, Gv, and power gain, Gp. Voltage gain is defined as the ratio of the differential output voltage at node OUT_AMP to the differential, or single-ended, input voltage at the node before Rg. Power gain, for the purposes of this document, is defined as the ratio of the power dissipated on RL (100 Ω-differential) to the power transferred from a source to the input impedance of the amplifier. Whereas voltage gain contains no input and load impedances in its calculation, power gain does depend on termination impedances.

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8.2 ATE Testing and DC Measurements

All production testing and ensured dc parameters are measured on automated test equipment capable of dc measurements only. Measurements such as output current sourcing and sinking are made in reference to the device output pins. Some measurements (such as voltage gain) are referenced to the output of the internal amplifier and do not include losses attributed to the on-chip output resistors. The *Electrical Characteristics* table conditions specify these conditions. When the measurement is referred to the amplifier output, then the output resistors are not included in the measurement. If the measurement is referred to the device pins, then the output resistor loss is included in the measurement.

8.3 Frequency Response

This test is run with both single-ended inputs and differential inputs.

For tests with single-ended inputs, the standard EVM is used with no changes; see Figure 54. In order to provide a matched input, the unused input requires a broadband 50-Ω termination to be connected. When using a four-port network analyzer, the unused input can either be terminated with a broadband load, or can be connected to the unused input on the four-port analyzer. The network analyzer provides proper termination. A network analyzer is connected to the input and output of the EVM with 50-Ω coaxial cables and is set to measure the forward transfer function (s21). The input signal frequency is swept with the signal level set for the desired output amplitude.

The LMH5401-SP is fully symmetrical, either input (IN+ or IN–) can be used for single-ended inputs. The unused input must be terminated. R_F, R_{G1}, and R_{G2} determine the gain. R_T and R_M enable matching to the source resistance. See the *Test Schematics* section for more information on setting these resistors per gain and source impedance requirements. Bandwidth is dependant on gain settings because this device is a voltage feedback amplifier. With a GBP of 6.5 GHz, the approximate bandwidth can be calculated for a specific application requirement, as shown in Equation 2. Figure 55 illustrates a test schematic for differential input and output.

$$\text{GBP (Hz)} = \text{BW (Hz)} \times \text{Noise Gain} \quad (2)$$

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Frequency Response (continued)

For tests with differential inputs, the same setup for single-ended inputs is used except all four connectors are connected to a network analyzer port. Measurements are made in either true differential mode on the Rohde & Schwarz® network analyzer or in calculated differential mode. In both cases, the differential inputs are each driven with a 50-Ω source. Table 2 and Table 3 list resistor values for various gain settings.

Table 2. Differential Input/Output

A_V (V/V)	R_{G1}, R_{G2} (Ω)	R_F (Total / External, Ω)	R_T (Ω)
2	100	199 / 174	100
4	49.9	199 / 174	N/A
6	49.9	300 / 274	N/A
8	49.9	400 / 375	N/A
10	49.9	500 / 475	N/A

Table 3. SE Input

A_V (V/V)	R_{G1} (Ω)	R_T (Ω)	R_{G2} (Ω)	R_F (Total / External, Ω)
2	90.9	76.8	121	200 / 175
4	22.6	357	66.5	152 / 127
8	12.1	1100	60.4	250 / 225
10	9.76	1580	57.6	300 / 275

8.4 S-Parameters

The standard EVM is used for all s-parameter measurements. All four ports are used or are terminated with 50 Ω; see the *Frequency Response* section.

8.5 Frequency Response with Capacitive Load

The standard EVM is used and the capacitive load is soldered to the inside pads of the 40-Ω matching resistors (on the DUT side). In this configuration, the on-chip, 10-Ω resistors isolate the capacitive load from the amplifier output pins. The test schematic for capacitive load measurements is illustrated in Figure 56.

8.6 Distortion

The standard EVM is used for measuring single-tone harmonic distortion and two-tone intermodulation distortion. All distortion is measured with single-ended input signals; see Figure 57. In order to interface with single-ended test equipment, external baluns are required between the EVM output ports and the test equipment. The *Typical Characteristics* plots are created with Marki™ baluns, model number BAL-0010. These baluns are used to combine two tones in the two-tone test plots. For distortion measurements the same termination must be used on both input pins. When a filter is used on the driven input port, the same filter and a broadband load are used to terminate the other input. When the signal source is a broadband controlled impedance, then only a broadband-controlled impedance is required to terminate the unused input.

8.7 Noise Figure

The standard EVM is used with a single-ended input matched to 50-Ω and the Marki balun on the output similar to the harmonic distortion test setup.

8.8 Pulse Response, Slew Rate, and Overdrive Recovery

The standard EVM is used for time-domain measurements. The input is single-ended with the differential outputs routed directly to the oscilloscope inputs. The differential signal response is calculated from the two separate oscilloscope inputs (Figure 28 to Figure 30). In addition, the common-mode response is also captured in this configuration.

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8.9 Power Down

The standard EVM is used with the shorting block on jumper JPD removed completely. A high-speed, 50-Ω pulse generator is used to drive the PD pin when the output signal is measured by viewing the output signal (such as a 250-MHz sine-wave input).

8.10 V_{CM} Frequency Response

The standard EVM is used with R_{CM+} and $R_{CM–}$ removed and a new resistor installed at R_{TCM} = 49.9 Ω. The 49.9-Ω resistor is placed at R14 on the EVM schematic. A network analyzer is connected to the V_{CM} input of the EVM and the EVM outputs are connected to the network analyzer with 50-Ω coaxial cables. Set the network analyzer analysis settings to single-ended input and differential output. Measure the output common-mode with respect to the single-ended input (Scs21). The input signal frequency is swept with the signal level set for 100 mV (–16 dBm). Note that the common-mode control circuit gain is one.

8.11 Test Schematics

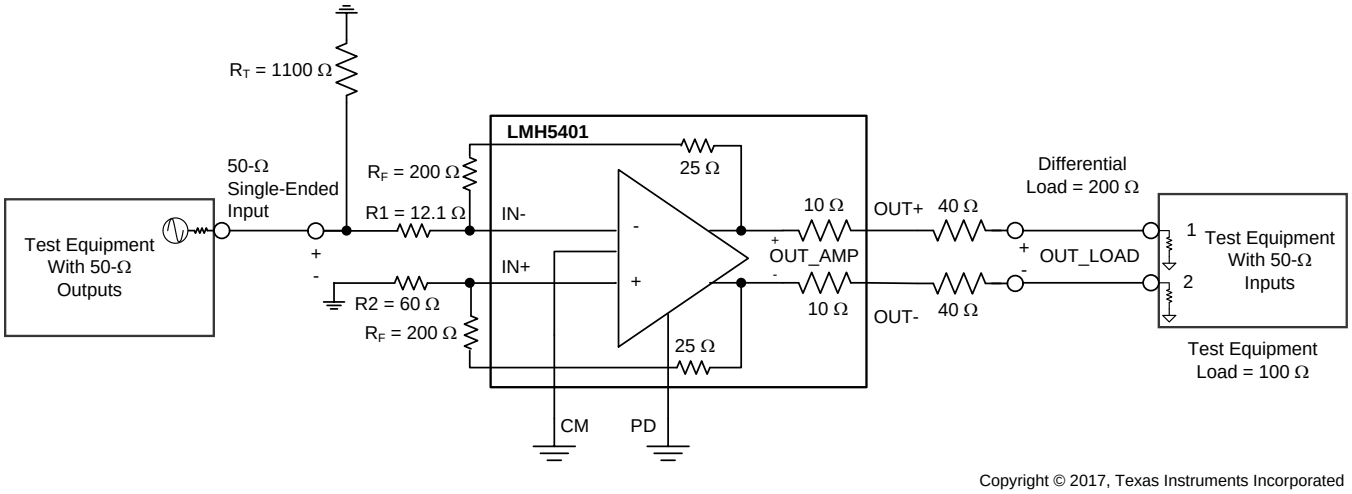

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Figure 54. Test Schematic: Single-Ended Input, Differential Output, G_V = 7 V/V

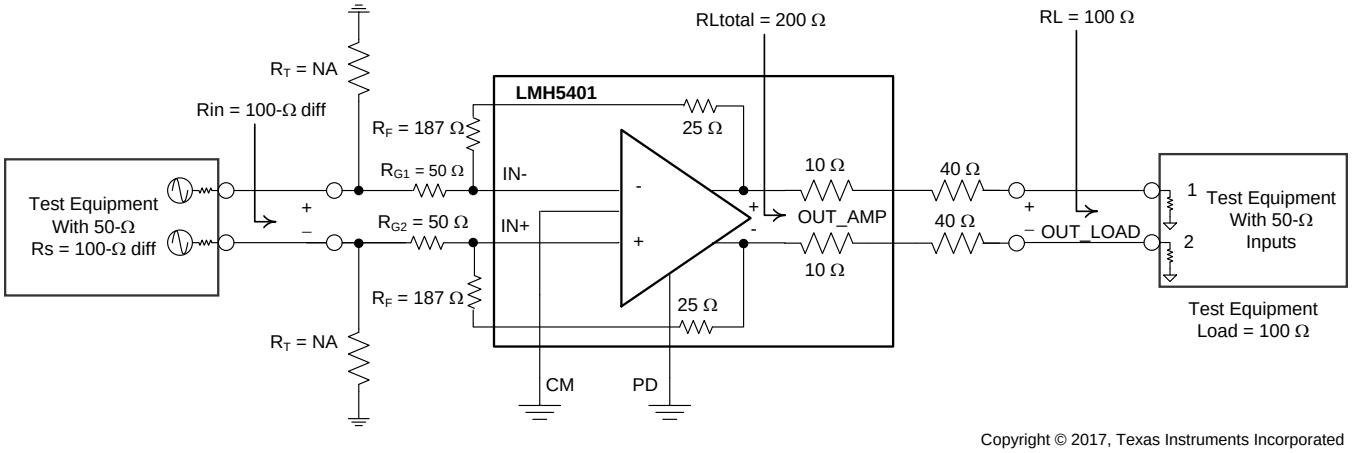

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Figure 55. Test Schematic: Differential Input, Differential Output, G_V = 4.25 V/V

Test Schematics (continued)

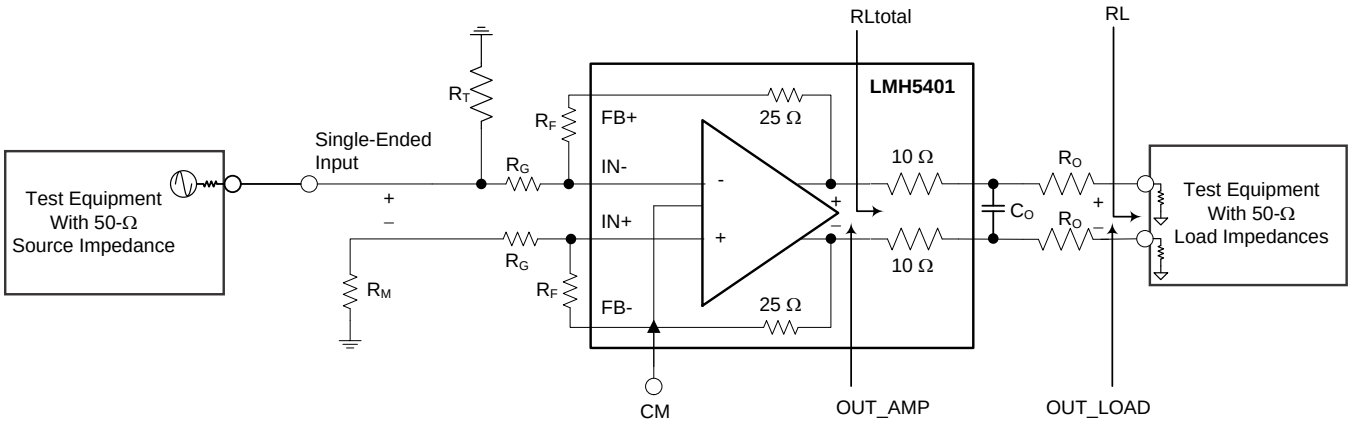

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Figure 56. Test Schematic: Capacitive Load, G_V = 7 V/V

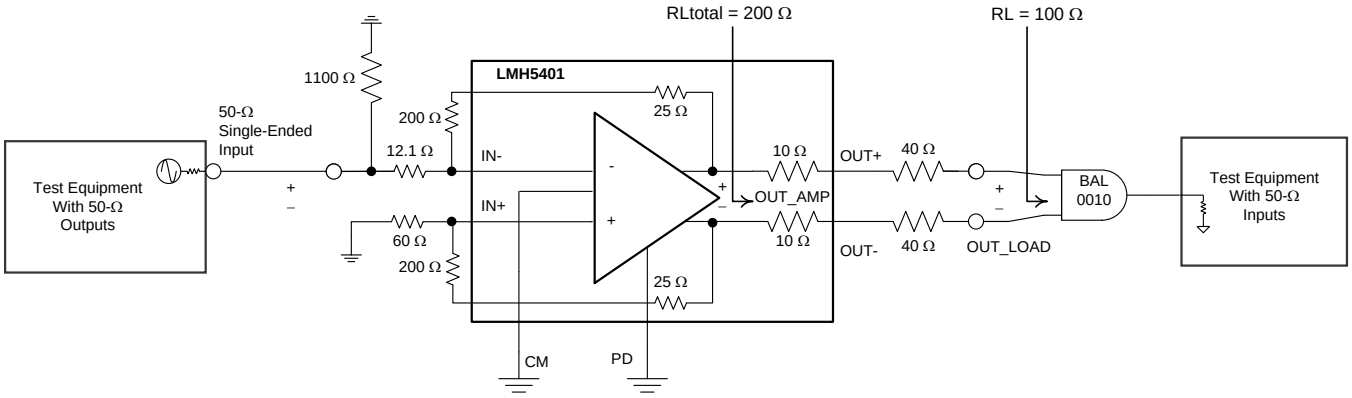

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Figure 57. Test Schematic for Noise Figure and Single-Ended Harmonic Distortion, G_V = 7 V/V

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9 Detailed Description

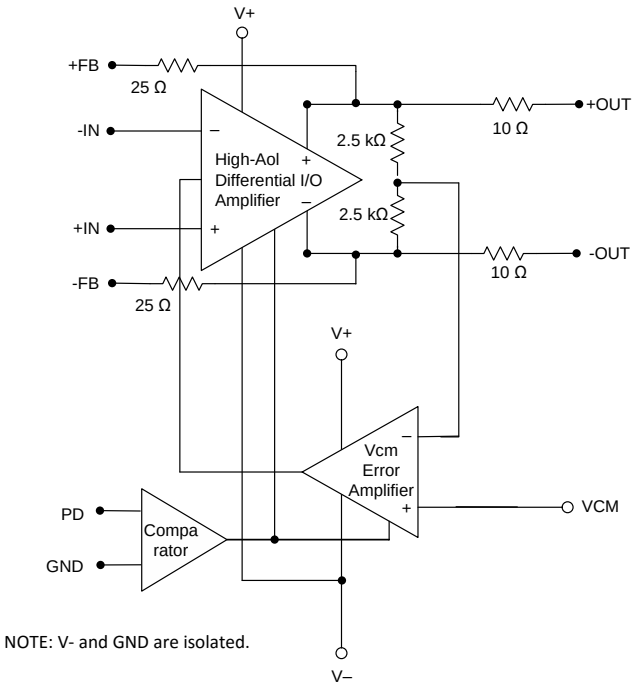
9.1 Overview

The LMH5401-SP is a very high-performance, differential amplifier optimized for radio frequency (RF) and intermediate frequency (IF) or high-speed, time-domain applications for wide bandwidth applications as the GBP is 6.5 GHz. The device is ideal for dc- or ac-coupled applications that may require a single-ended-to-differential (SE-DE) conversion when driving an analog-to-digital converter (ADC). The necessary external feedback (R_F) and gain set (R_G) resistors configure the gain of the device. For the EVM the standard gain is set to Gv = 17 dB (for both DE and SE conversions) with R_F = 200 Ω and R_G = 12.1 Ω.

A common-mode reference input pin is provided to align the amplifier output common-mode with the ADC input requirements. Power supplies between 3.3 V and 5 V can be selected and dual-supply operation is supported when required by the application. A power-down feature is also available for power savings.

The LMH5401-SP offers two on-chip termination resistors, one for each output with values of 10 Ω each. For most load conditions the 10-Ω resistors are only a partial termination. Consequently, external termination resistors are required in most applications. See Table 4 for some common load values and the matching resistors.

9.2 Functional Block Diagram



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NOTE: V– and GND are isolated.

9.3 Feature Description

The LMH5401-SP includes the following features:

- Fully-differential amplifier
- Flexible gain configurations using external resistors
- Output common-mode control
- Single- or split-supply operation
- Gain bandwidth product (GBP) of 6.5 GHz
- Linear bandwidth of 2 GHz (Gv = 17 dB)
- Power down

Feature Description (continued)

9.3.1 Fully-Differential Amplifier

The LMH5401-SP is a voltage feedback (VFA)-based fully-differential amplifier (FDA) offering a GBP of 6.5 GHz with flexible gain options using external resistors. The core differential amplifier is a slightly decompensated voltage feedback design with a high slew rate and best-in-class linearity up to 2 GHz for Gv = 17 dB (SE-DE, DE-DE).

As with all FDA devices, the output average voltage (common-mode) is controlled by a separate common-mode loop. The target for this output average is set by the V_{CM} input pin. The V_{OCM} range extends from 1.1 V below the midsupply voltage to 1.1 V above the midsupply voltage when using a 5-V supply. Note that on a 3.3-V supply the output common-mode range is quite small. For applications using a 3.3-V supply voltage, the output common-mode must remain very close to the midsupply voltage.

The input common-mode voltage offers more flexibility than the output common-mode voltage. The input common-mode range extends from the negative rail to approximately 1 V above the midsupply voltage when powered with a 5-V supply.

A power-down pin is included. This pin is referenced to the GND pins with a threshold voltage of approximately 1 V. Setting the PD pin voltage to more than the specified minimum voltage turns the device off, placing the LMH5401-SP into a very low quiescent current state. Note that, when disabled, the signal path is still present through the passive external resistors. Input signals applied to a disabled LMH5401-SP device still appear at the outputs at some level through this passive resistor path, as with any disabled FDA device. The power-down pin is biased to the logic low state with a 50-kΩ internal resistor.

9.3.2 Operations for Single-Ended to Differential Signals

One of the most useful features supported by the FDA device is the active balun configuration which provides an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. Although the output side is relatively straightforward, the device input pins move in a common-mode sense with the input signal. This feature acts to increase the apparent input impedance to be greater than the R_G value. However, this feature can cause input clipping if this common-mode signal moves beyond the input range. This input active impedance issue applies to both ac- and dc-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as described in this section.

9.3.2.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversion

When the signal path is ac coupled, the dc biasing for the LMH5401-SP becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The ac-coupling issue can be separated for the input and output sides of an FDA design. The input can be ac coupled and the output dc coupled, or the output can be ac coupled and the input dc coupled, or they can both be ac coupled. One situation where the output can be dc coupled (for an ac-coupled input), is when driving directly into an ADC where the V_{OCM} control voltage uses the ADC common-mode reference to directly bias the FDA output common-mode to the required ADC input common-mode. The feedback path must always be dc-coupled. In any case, the design starts by setting the desired V_{OCM}. When an ac-coupled path follows the output pins, the best linearity is achieved by operating V_{OCM} at mid supply. The V_{OCM} voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications. If the output path is also ac coupled, simply letting the V_{OCM} control pin float is usually preferred in order to obtain a midsupply default V_{OCM} bias with no external elements. To limit noise, place a 0.1-µF decoupling capacitor on the V_{OCM} pin to ground. After V_{OCM} is defined, check the target output voltage swing to ensure that the V_{OCM} positive or negative output swing on each side does not clip into the supplies. If the desired output differential swing is defined as V_{OPP}, divide by 4 to obtain the $\pm V_P$ swing around V_{OCM} at each of the two output pins (each pin operates 180° out of phase with the other). Check that $V_{OCM} \pm V_P$ does not exceed the output swing of this device. Going to the device input pins side, because both the source and balancing resistor on the non-signal input side are dc blocked (see Figure 59), no common-mode current flows from the output common-mode voltage, thus setting the input common-mode equal to the output common-mode voltage. This input headroom also sets a limit for higher V_{OCM} voltages. The minimum headroom for the input pins to the positive supply overrides the headroom limit for the output V_{OCM} because the input V_{ICM} is the output V_{OCM} for ac-coupled sources. Also, the input signal moves this input V_{ICM} around the dc bias point, as described in the *Resistor Design Equations for Single-to-Differential Applications* subsection of the *Fully-Differential Amplifier* section.

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Feature Description (continued)

9.3.2.2 DC-Coupled Input Signal Path Considerations for SE-DE Conversions

The output considerations remain the same as for the ac-coupled design. Again, the input can be dc coupled when the output is ac coupled. A dc-coupled input with an ac-coupled output can have some advantages to move the input V_{ICM} down if the source is ground referenced. When the source is dc coupled into the LMH5401-SP (as shown in Figure 58), both sides of the input circuit must be dc coupled to retain differential balance. Normally, the non-signal input side has an R_G element biased to whatever the source midrange is expected to be. Providing this mid-scale reference gives a balanced differential swing around V_{OCM} at the outputs. Often, R_{G2} is simply grounded for dc-coupled, bipolar-input applications. This configuration gives a balanced differential output if the source swings around ground. If the source swings from ground to some positive voltage, grounding R_{G2} gives a unipolar output differential swing from both outputs at V_{OCM} (when the input is at ground) to one polarity of swing. Biasing R_{G2} to an expected midpoint for the input signal creates a differential output swing around V_{OCM}. One significant consideration for a dc-coupled input is that V_{OCM} sets up a common-mode bias current from the output back through R_F and R_G to the source on both sides of the feedback. Without input-balancing networks, the source must sink or source this dc current. After the input signal range and biasing on the other R_G element is set, check that the voltage divider from V_{OCM} to V_I through R_F and R_G (and possibly R_S) establishes an input V_{ICM} at the device input pins that is in range.

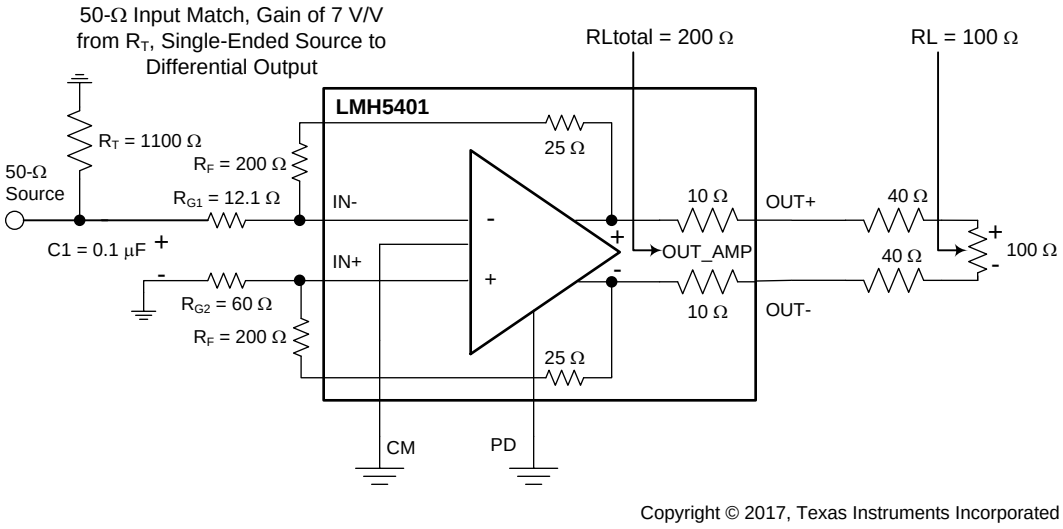

Figure 58. DC-Coupled, Single-Ended-to-Differential, Gv = 7 V/V

9.3.2.3 Resistor Design Equations for Single-to-Differential Applications

Being familiar with the FDA resistor selection criteria is still important because the LMH5401-SP gain is configured through external resistors. The design equations for setting the resistors around an FDA to convert from a single-ended input signal to a differential output can be approached in several ways. In this section, several critical assumptions are made to simplify the results:

- The feedback resistors are selected first and are set to be equal on the two sides of the device.
- The dc and ac impedances from the summing junctions back to the signal source and ground (or a bias voltage on the non-signal input side) are set equal to retain the feedback divider balance on each side of the FDA.

Both of these assumptions are typical and are aimed to deliver the best dynamic range through the FDA signal path.

After the feedback resistor values are chosen, the aim is to solve for R_T (a termination resistor to ground on the signal input side), R_{G1} (the input gain resistor for the signal path), and R_{G2} (the matching gain resistor on the non-signal input side); see Figure 59. This example uses the LMH5401-SP, an external resistor FDA. The same resistor solutions can be applied to either ac- or dc-coupled paths. Adding blocking capacitors in the input-signal chain is a simple option. Adding these blocking capacitors after the R_T element (see Figure 59) has the advantage of removing any dc currents in the feedback path from the output V_{OCM} to ground.

Feature Description (continued)

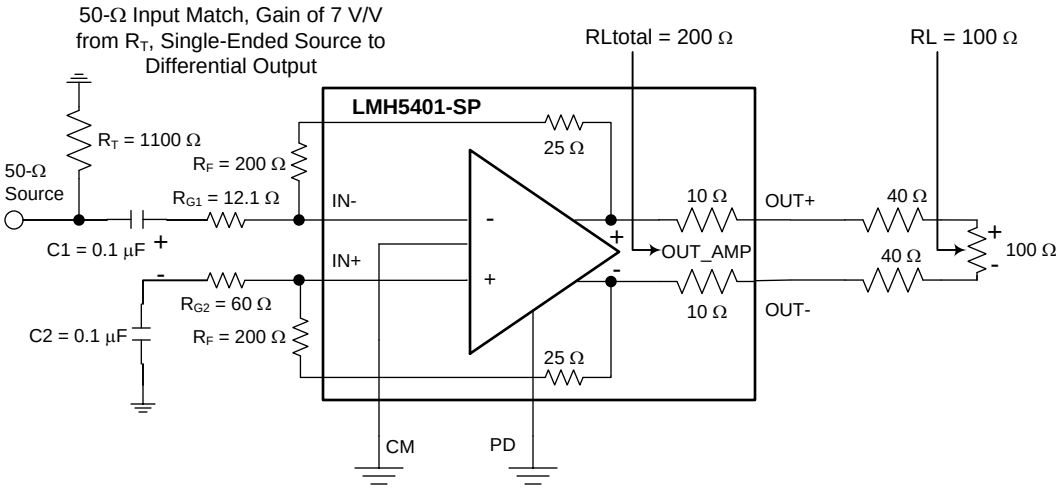

Figure 59. AC-Coupled, Single-Ended Source to a Differential Gain of a 7-V/V

Most FDA amplifiers use external resistors and have complete flexibility in the selected R_F, however the LMH5401-SP has small on-chip feedback resistors that are fixed at 25 Ω. The equations used in this section apply with an additional 25 Ω to be added to the external R_F resistors.

After the feedback resistor values are chosen, the aim is to solve for R_T (a termination resistor to ground on the signal input side), R_{G1} (the input gain resistor for the signal path), and R_{G2} (the matching gain resistor on the non-signal input side). The same resistor solutions can be applied to either ac- or dc-coupled paths. Adding blocking capacitors in the input-signal chain is a simple option. Adding these blocking capacitors after the R_T element has the advantage of removing any dc currents in the feedback path from the output V_{OCM} to ground.

Earlier approaches to the solutions for R_T and R_{G1} (when the input must be matched to a source impedance, R_S) follow an iterative approach. This complexity arises from the active input impedance at the R_{G1} input. When the FDA is used to convert a single-ended signal to differential, the common-mode input voltage at the FDA inputs must move with the input signal to generate the inverted output signal as a current in the R_{G2} element. A more recent solution is shown as Equation 3, where a quadratic in R_T can be solved for an exact required value. This quadratic emerges from the simultaneous solution for a matched input impedance and target gain. The only inputs required are:

1. The selected R_F value.
2. The target voltage gain (A_V) from the input of R_T to the differential output voltage.
3. The desired input impedance at the junction of R_T and R_{G1} to match R_S.

Solving this quadratic for R_T starts the solution sequence, as shown in Equation 3:

$$R_T^2 - R_T \frac{2R_S\left(2R_F + \frac{R_S}{2}A_V^2\right)}{2R_F\left(2 + A_V\right) - R_S A_V(4 + A_V)} - \frac{2R_F R_S^2 A_V}{2R_F\left(2 + A_V\right) - R_S A_V\left(4 + A_V\right)} = 0 \quad (3)$$

Being a quadratic, there are limits to the range of solutions. Specifically, after R_F and R_S are chosen, there is physically a maximum gain beyond which Equation 3 starts to solve for negative R_T values (if input matching is a requirement). With R_F selected, use Equation 4 to verify that the maximum gain is greater than the desired gain.

$$Av_{max} = \left(\frac{R_F}{R_S} - 2\right) \bullet \left[1 + \sqrt{1 + \frac{4\frac{R_F}{R_S}}{\left(\frac{R_F}{R_S} - 2\right)^2}}\right] \quad (4)$$

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Feature Description (continued)

If the achievable A_{Vmax} is less than desired, increase the R_F value. After R_T is derived from Equation 3, the R_{G1} element is given by Equation 5:

$$R_{G1} = \frac{2\frac{R_F}{A_V} - R_S}{1 + \frac{R_S}{R_T}} \tag{5}$$

Then, the simplest approach is to use a single $R_{G2} = R_T \parallel R_S + R_{G1}$ on the non-signal input side. Often, this approach is shown as the separate R_{G1} and R_S elements. This approach can provide a better divider match on the two feedback paths, but a single R_{G2} is often acceptable. A direct solution for R_{G2} is given as Equation 6:

$$R_{G2} = \frac{2\frac{R_F}{A_V}}{1 + \frac{R_S}{R_T}} \tag{6}$$

This design proceeds from a target input impedance matched to R_S, signal gain A_V, and a selected R_F value. The nominal R_F value chosen for the LMH5401-SP characterization is 225 Ω ($R_{FExternal}$ + $R_{FInternal}$, where $R_{FInternal}$ is always 25 Ω). As discussed previously, this resistance is on-chip and cannot be changed. Refer to Table 2 and Table 3 in the *Frequency Response* section, which list the value of resistors used for characterization in this document.

9.3.2.4 Input Impedance Calculations

The designs so far have included a source impedance, R_S, that must be matched by R_T and R_{G1}. The total impedance with respect to the input at R_{G1} for the circuit of Figure 58 is the parallel combination of R_T to ground and ZA (active impedance) presented by the amplifier input at R_{G1}. That expression, assuming R_{G2} is set to obtain a differential divider balance, is given by Equation 7:

$$ZA = R_{G1}\frac{\left(1 + \frac{R_{G1}}{R_{G2}}\right)\left(1 + \frac{R_F}{R_{G1}}\right)}{2 + \frac{R_F}{R_{G2}}} \tag{7}$$

For designs that do not need impedance matching (but instead come from the low-impedance output of another amplifier, for instance), $R_{G1} = R_{G2}$ is the single-to-differential design used without R_T to ground. Setting $R_{G1} = R_{G2} = R_G$ in Equation 7 gives the input impedance of a simple input FDA driving from a low-impedance, single-ended source to a differential output.

9.3.3 Differential-to-Differential Signals

The LMH5401-SP can also be used to amplify differential input signals to differential output signals. In many ways, this method is a much simpler way to operate the FDA from a design equations perspective. Again, assuming the two sides of the circuit are balanced with equal R_F and R_G elements, the differential input impedance is now just the sum of the two R_G elements to a differential inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal, but must be dc biased in the allowable range for the input pins with consideration given to the voltage headroom required to each supply. Slightly different considerations apply to ac- or dc-coupled, differential-in to differential-out designs, as described in this section.

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Feature Description (continued)

9.3.3.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

When using the LMH5401-SP with an ac-coupled differential source, the input can be coupled in through two blocking capacitors. An optional input differential termination resistor (R_M) can be included to allow the input R_G resistors to be scaled up while still delivering lower differential input impedance to the source. In Figure 60, the R_G elements sum to show a 200-Ω differential impedance and the R_M element combines in parallel to give a net 100-Ω, ac, differential impedance to the source. Again, the design proceeds ideally by selecting the R_F element values, then the R_G to set the differential gain, then an R_M element (if needed) to achieve a target input impedance. Alternatively, the R_M element can be eliminated, the R_G elements set to the desired input impedance, and R_F set to the get the differential gain (= R_F / R_G). The dc biasing in Figure 60 is very simple. The output V_{OCM} is set by the input control voltage and, because there is no dc current path for the output common-mode voltage, that dc bias also sets the input pins common-mode operating points.

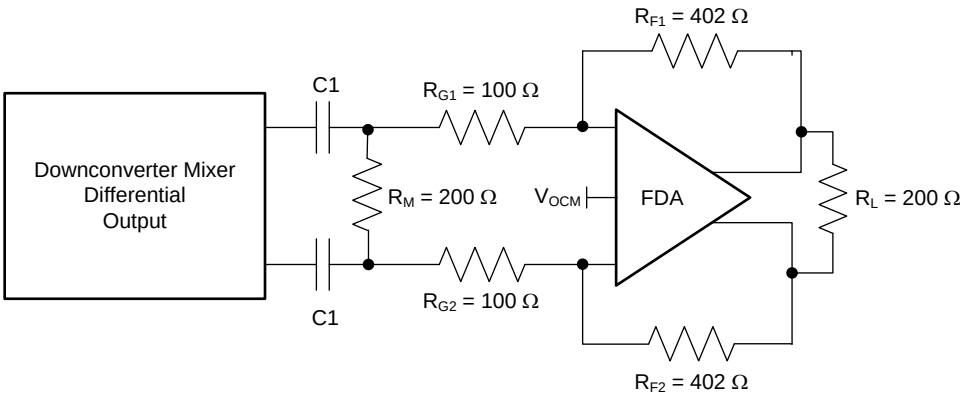

Figure 60. Downconverting Mixer AC-Coupled to the LMH5401-SP (G_V = 4 V/V)

9.3.3.2 DC-Coupled, Differential-Input to Differential-Output Design Issues

Operating the LMH5401-SP with a dc-coupled input source simply requires that the input pins stay in range of the dc common-mode operating voltage. Only R_G values that are equal to the differential input impedance and that set the correct R_F values for the gain desired are required.

9.3.4 Output Common-Mode Voltage

The CM input controls the output common-mode voltage. CM has no internal biasing network and must be driven by an external source or resistor divider network to the positive power supply. The CM input impedance is very high and bias current is not critical. Also, the CM input has no internal reference and must be driven from an external source. Using a bypass capacitor is also necessary. A capacitor value of 0.01 µF is recommended. For best harmonic distortion, maintain the CM input within ±1 V of the midsupply voltage using a 5-V supply and within ±0.5 V when using a 3.3-V supply. The CM input voltage can be operated outside this range if lower output swing is used or distortion degradation is allowed. For more information, see Figure 24 and Figure 25.

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9.4 Device Functional Modes

9.4.1 Operation With a Split Supply

The LMH5401-SP can be operated using split supplies. One of the most common supply configurations is ±2.5 V. In this case, VS+ is connected to 2.5 V, VS– is connected to –2.5 V, and the GND pins are connected to the system ground. As with any device, the LMH5401-SP is impervious to what the levels are named in the system. In essence, using split supplies is simply a level shift of the power pins by –2.5 V. If everything else is level-shifted by the same amount, the device does not detect any difference. With a ±2.5-V power supply, the CM range is 0 V ±1 V; the input has a slightly larger range of –2.5 V to 1 V. This design has certain advantages in systems where signals are referenced to ground, and as noted in the *ADC Input Common-Mode Voltage Considerations—DC-Coupled Input* section, for driving ADCs with low input common-mode voltage requirements in dc-coupled applications. With the GND pin connected to the system ground, the power-down threshold is 1.2 V, which is compatible with most logic levels from 1.5-V CMOS to 2.5-V CMOS.

As noted previously, the absolute supply voltage values are not critical. For example, using a 4-V VS+ and a –1-V VS– still results in a 5-V supply condition. As long as the input and output common-mode voltages remain in the optimum range, the amplifier can operate on any supply voltages from 3.3 V to 5.25 V. When considering using supply voltages near the 3.3-V total supply, be very careful to make sure that the amplifier performance is adequate. Setting appropriate common-mode voltages for large-signal swing conditions becomes difficult when the supply voltage is below 4 V.

9.4.2 Operation With a Single Supply

As with split supplies, the LMH5410-SP can be operated from single-supply voltages from 3.3 V to 5.25 V. Single-supply operation is most appropriate when the signal path is ac coupled and the input and output common-mode voltages are set to mid supply by the CM pin and are preserved by coupling capacitors on the input and output.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Stability, Noise Gain, and Signal Gain

Two types of gain are associated with amplifiers: noise gain (NG) and signal gain. Noise gain determines the stability of an amplifier. The noise gain is the inverse of the voltage divider from the outputs back to the differential inputs. This gain is calculated by NG = (R_F / R_{IN}) + 1. For the LMH5401-SP, NG > 4 creates a stable circuit independent on how the signal gain is set. In Figure 61, for optimal performance choose R_F within the values noted in this document (see the *Parameter Measurement Information* section for further information). Using too large of a resistance in the feedback path adds noise and can possibly have a negative affect on bandwidth, depending on the parasitic capacitance of the board; too low of a resistance can load the output, thus affecting distortion performance. When low signal gain stability is needed, the noise gain can be altered with the addition of a resistor, R_{comp}. By manipulating the noise gain with this addition, the amplifier can be stabilized at lower signal gains. In Figure 61, R_S and R_{comp} in parallel combination also affects the noise gain of the amplifier. R_G and R_F are the main gain-setting resistors and the addition of R_{comp} adjusts the noise gain for stability. Much of this stability can be simulated using the LMH5401-SP TINA model, depending on the amplifier configuration. The example in Figure 61 uses the LMH5401-SP, a signal gain of 2.8 V/V, and a noise gain of 4.75 V/V resulting in the frequency response shown in Figure 62.

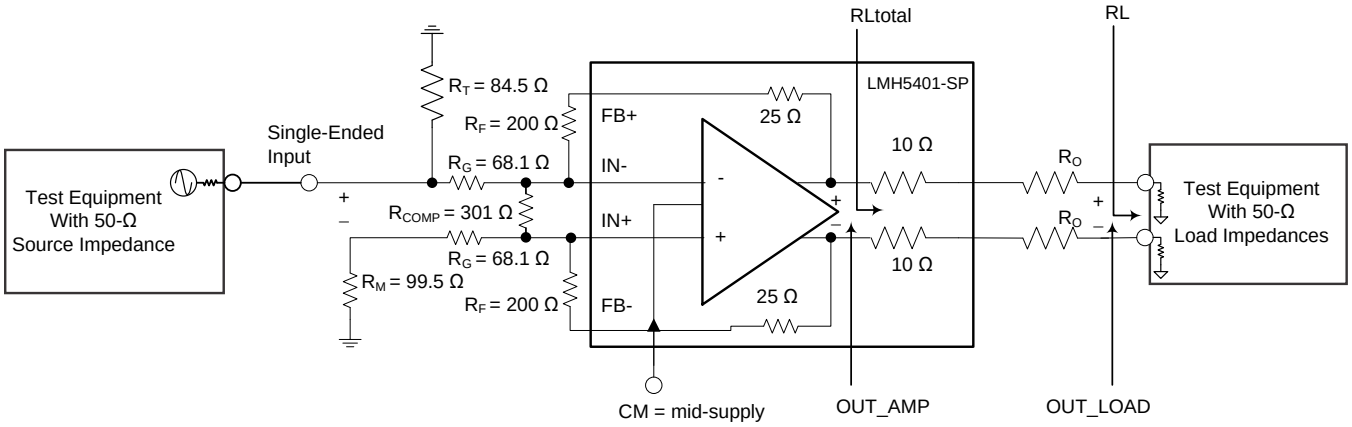

Figure 61. Noise Gain Compensation for Stability at Gp = 0 dB

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Application Information (continued)

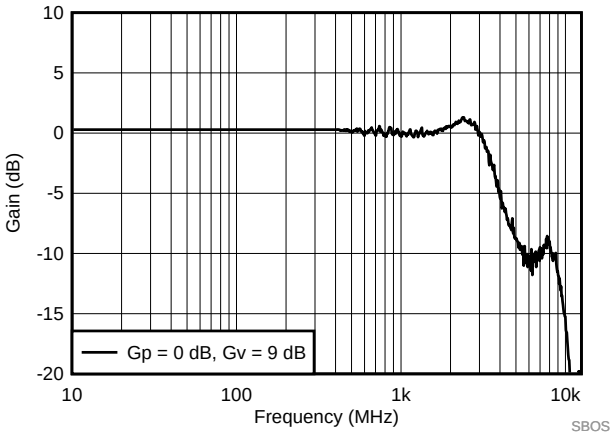

Figure 62. SE-DE Small Signal Frequency Response for Low Gain

10.1.2 Input and Output Headroom Considerations

The starting point for most designs is to assign an output common-mode voltage. For ac-coupled signal paths, this starting point is often the default midsupply voltage to retain the most available output swing around the output operating point, which is centered with V_{CM} equal to the midsupply point. For dc-coupled designs, set this voltage considering the required minimum headroom to the supplies listed in the *Electrical Characteristics* tables for V_{CM} control. From that target output, V_{CM}, the next step is to verify that the desired output differential V_{PP} stays within the supplies. For any desired differential output voltage (V_{OPP}) check the maximum possible signal swing for each output pin. Make sure that each pin can swing to the voltage required by the application.

For instance, when driving the ADC12D1800RF with a 1.25-V common-mode and 0.8-V_{PP} input swing, the maximum output swing is set by the negative-going signal from 1.25 V to 0.2 V. The negative swing of the signal is right at the edge of the output swing capability of the LMH5401-SP. In order to set the output common-mode to an acceptable range, a negative power supply of at least –1 V is recommended. The ideal negative supply voltage is the ADC V_{CM} – 2.5 V for the negative supply and the ADC V_{CM} + 2.5 V for the input swing. In order to use the existing supply rails, deviating from the ideal voltage may be necessary.

With the output headroom confirmed, the input junctions must also stay within their operating range. Because the input range extends nearly to the negative supply voltage, input range limitations only appear when approaching the positive supply where a maximum 1.5-V headroom is required.

The input pins operate at voltages set by the external circuit design, the required output V_{OCM}, and the input signal characteristics. The operating voltage of the input pins depends on the external circuit design. With a differential input, the input pins operate at a fixed input V_{ICM}, and the differential input signal does not influence this common-mode operating voltage.

AC-coupled differential input designs have a V_{ICM} equal to the output V_{OCM}. DC-coupled differential input designs must check the voltage divider from the source V_{CM} to the LMH5401-SP CM setting. That result solves to an input V_{ICM} within the specified range. If the source V_{CM} can vary over some voltage range, the validation calculations must include this variation.

10.1.3 Noise Analysis

The first step in the output noise analysis is to reduce the application circuit to its simplest form with equal feedback and gain setting elements to ground (as shown in Figure 63) with the FDA and resistor noise terms to be considered.

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Application Information (continued)

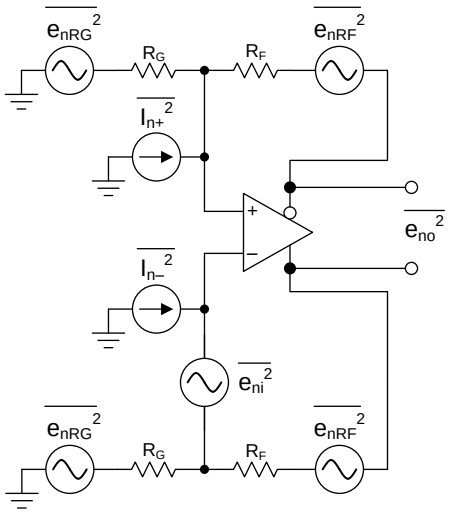

Figure 63. FDA Noise-Analysis Circuit

The noise powers are shown in Figure 63 for each term. When the R_F and R_G terms are matched on each side, the total differential output noise is the root sum of squares (RSS) of these separate terms. Using NG (noise gain) ≡ 1 + R_F / R_G, the total output noise is given by Equation 8. Each resistor noise term is a 4-k*T*R power.

$$e_{no} = \sqrt{\left(e_{ni}NG\right)^2 + 2\left(i_nR_F\right)^2 + 2\left(4kTR_FNG\right)} \tag{8}$$

The first term is simply the differential input spot noise times the noise gain. The second term is the input current noise terms times the feedback resistor (and because there are two terms, the power is two times one of the terms). The last term is the output noise resulting from both the R_F and R_G resistors, again times two, for the output noise power of each side added together. Using the exact values for a 50-Ω, matched, single-ended to differential gain, sweep with 2 Ω (plus an internal 25 Ω) and the intrinsic noise e_{ni} = 1.25 nV and i_n = 3.5 pA for the LMH5401-SP, which gives an output spot noise from Equation 8. Then, dividing by the signal gain set through internal resistors (A_V), gives the input-referred, spot-noise voltage (e_i) of 1.35 nV/√Hz. Note that for the LMH5401-SP the current noise is an insignificant noise contributor because of the low value of R_F.

10.1.4 Noise Figure

Noise figure (NF) is a helpful measurement in an RF system design. The basis of this calculation is to define how much thermal noise the system (or even on the component) adds to this input signal. All systems are assumed to have a starting thermal noise power of –174 dBm/√Hz at room temperature calculated from $P_{(dBW)}$ = 10 × log (kTB), where T is temperature in Kelvin (290k), B is bandwidth in Hertz (1 Hz), and k is Boltzmann's constant 1.38 × 10^{-23} (J / K). Whenever an element is placed in a system, additional noise is added beyond the thermal noise floor. The noise factor (F) helps calculate the noise figure and is the ratio between the input SNR and the output SNR. Input SNR includes the noise contribution from the resistive part of the source impedance, Z_S. NF is relative to the source impedance used in the measurement or calculation because ideal capacitors and inductors are known to be noiseless. NF can be calculated by Equation 9:

$$NF = 10 \log \left(e_{no}^2 / en_{Zs}\right)$$

where

- $e_{n(Zs)}$ is the thermal noise of the source resistance and equal to 4 kTR_S $(GD_T)^2$,
- G is the voltage gain of the amplifier. (9)

From Equation 10, NF is roughly equal to 10 dB which is the just above the actual value of 9.6 dB measured on the bench at 200 MHz when referenced to 50 Ω and as illustrated in Figure 29.

$$D_T = \frac{R_T}{R_S + R_T} \tag{10}$$

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Application Information (continued)

For thermal noise calculations with different source resistance, Equation 11 can be used to calculate the NF change with a new source resistance. For example, Equation 9 uses a source resistance of 50 Ω. By using a source of 100 Ω, the new noise figure calculation (Equation 11) yields an NF with a 3-dB improved. This is intuitive as the noise of source increases, the noise of the amplifier becomes less noticeable, and, hence, the NF improves.

$$e_{n(Zs)} = kTRs \quad (11)$$

10.1.5 Thermal Considerations

The LMH5401-SP is packaged in a space-saving LCCC package that has a thermal coefficient ($R_{\theta JC(bot)}$) of 63.8°C/W. Limit the total power dissipation in order to keep the device junction temperature below 150°C for instantaneous power and below 125°C for continuous power.

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10.2 Typical Application

The LMH5401-SP is designed as a single-ended-to-differential (SE-DE) and differential-to-differential (DE-DE) gain block configured with external resistors and gain-stable single-ended to differential for NG ≥ 2 V/V. The LMH5401-SP has no low-end frequency cutoff and has 6.5-GHz gain product bandwidth. The LMH5401-SP is a very attractive substitute for a balun transformer in many applications.

The resistors labeled R_O serve to match the filter impedance to the 20-Ω amplifier differential output impedance. If no filter is used, these resistors may not be required if the ADC is located very close to the LMH5401-SP. If there is a transmission line between the LMH5401-SP and the ADC then the R_O resistors must be sized to match the transmission line impedance. A typical application driving an ADC is shown in Figure 64.

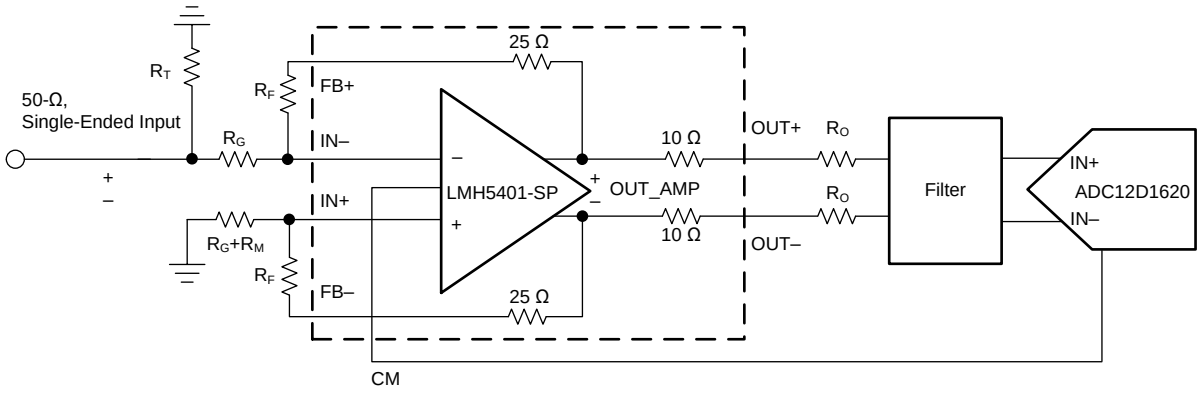

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Figure 64. Single-Ended Input ADC Driver

10.2.1 Design Requirements

The main design requirements are to keep the amplifier input and output common-mode voltages compatible with the ADC requirements and the amplifier requirements. Using split power supplies may be required.

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Typical Application (continued)

10.2.2 Detailed Design Procedure

10.2.2.1 Driving Matched Loads

The LMH5401-SP has on-chip output resistors, however, for most load conditions additional resistance must be added to the output to match a desired load. Table 4 lists the matching resistors for some common load conditions.

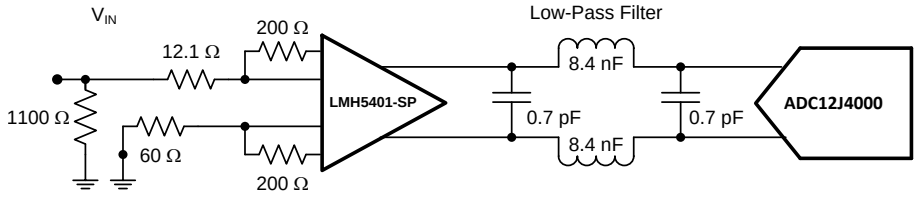
Table 4. Load Component Values(1)

LOAD (R_L)	R_{O+} AND R_{O-} FOR A MATCHED TERMINATION	TOTAL LOAD RESISTANCE AT AMPLIFIER OUTPUT (RL_{total})	TERMINATION LOSS
50 Ω	15 Ω	100 Ω	6 dB
100 Ω	40 Ω	200 Ω	6 dB
200 Ω	90 Ω	400 Ω	6 dB
400 Ω	190 Ω	800 Ω	6 dB
1 kΩ	490 Ω	2000 Ω	6 dB

(1) The total load includes termination resistors.

10.2.2.2 Driving Unmatched Loads For Lower Loss

When the LMH5401-SP and the load can be placed very close together, back-terminated transmission lines are not required. In this case, the 6-dB loss can be reduced significantly. One example is shown in Figure 65.



NOTE: Amplitude gain = 17 dB and net gain to ADC = 15.5 dB.

Figure 65. Low-Loss ADC

10.2.2.3 Driving Capacitive Loads

With high-speed signal paths, capacitive loading is highly detrimental to the signal path, as shown in Figure 66. Designers must make every effort to reduce parasitic loading on the amplifier output pins. The device on-chip resistors are included in order to isolate the parasitic capacitance associated with the package and the PCB pads that the device is soldered to. The LMH5401-SP is stable with most capacitive loads ≤ 10 pF; however, bandwidth suffers with capacitive loading on the output.

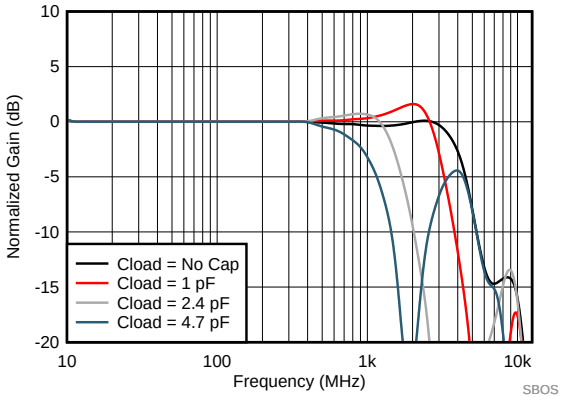


Figure 66. Frequency Response with Capacitive Load

10.2.2.4 Driving ADCs

The LMH5401-SP is designed and optimized for the highest performance to drive differential input ADCs. Figure 67 shows a generic block diagram of the LMH5401-SP driving an ADC. The primary interface circuit between the amplifier and the ADC is usually a filter of some type for antialias purposes, and provides a means to bias the signal to the input common-mode voltage required by the ADC. Filters range from single-order real RC poles to higher-order LC filters, depending on the requirements of the application. Output resistors (R_O) are shown on the amplifier outputs to isolate the amplifier from any capacitive loading presented by the filter.

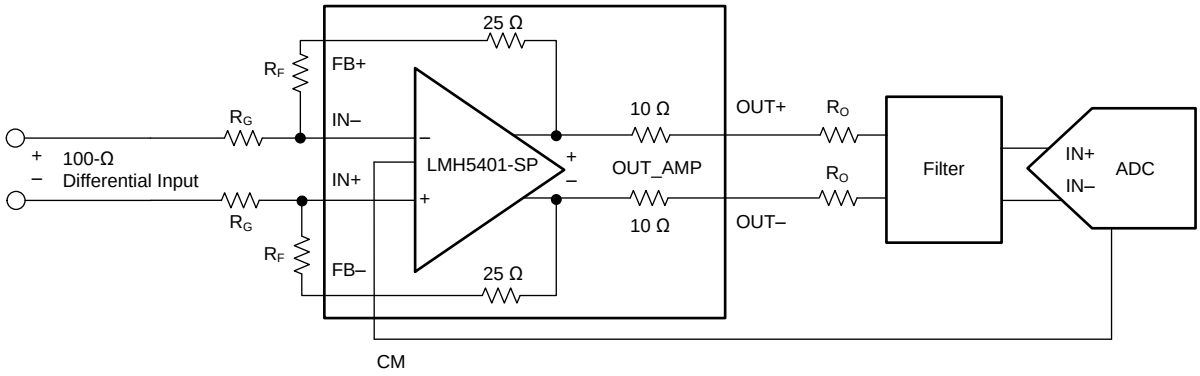


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Figure 67. Differential ADC Driver Block Diagram

The key points to consider for implementation are the SNR, SFDR, and ADC input considerations as described in this section.

10.2.2.4.1 SNR Considerations

The signal-to-noise ratio (SNR) of the amplifier and filter can be calculated from the amplitude of the signal and the bandwidth of the filter. The noise from the amplifier is band-limited by the filter with the equivalent brick-wall filter bandwidth. The amplifier and filter noise can be calculated using Equation 12:

$$SNR_{AMP+FILTER} = 10 \times \log\left(\frac{V^2_O}{e^2_{FILTEROUT}}\right) = 20 \times \log\left(\frac{V_O}{e_{FILTEROUT}}\right)$$

where:

- $e_{FILTEROUT} = e_{NAMPOUT} \times \sqrt{ENB}$,
- $e_{NAMPOUT}$ = the output noise density of the LMH5401-SP,
- ENB = the brick-wall equivalent noise bandwidth of the filter, and
- V_O = the amplifier output signal. (12)

For example, with a first-order (N = 1) band-pass or low-pass filter with a 30-MHz cutoff, the ENB is 1.57 × $f_{–3dB}$ = 1.57 × 30 MHz = 47.1 MHz. For second-order (N = 2) filters, the ENB is 1.22 × $f_{–3dB}$. When filter order increases, the ENB approaches $f_{–3dB}$ (N = 3 → ENB = 1.15 × $f_{–3dB}$; N = 4 → ENB = 1.13 × $f_{–3dB}$). Both V_O and $e_{FILTEROUT}$ are in RMS voltages. For example, with a 2-V_{PP} (0.707 V_{RMS}) output signal and a 30-MHz first-order filter, the SNR of the amplifier and filter is 70.7 dB with $e_{FILTEROUT}$ = 5.81 nV/√Hz × √47.1 MHz = 39.9 μV_{RMS}.

The SNR of the amplifier, filter, and ADC sum in RMS fashion is as shown in Equation 13 (SNR values in dB):

$$SNR_{SYSTEM} = -20 \times \log\left(\sqrt{10^{\frac{-SNR_{AMP+FILTER}}{10}} + 10^{\frac{-SNR_{ADC}}{10}}}\right) \quad (13)$$

This formula shows that if the SNR of the amplifier and filter equals the SNR of the ADC, the combined SNR is 3 dB lower (worse). Thus, for minimal degradation (< 1 dB) on the ADC SNR, the SNR of the amplifier and filter must be ≥ 10 dB greater than the ADC SNR. The combined SNR calculated in this manner is usually accurate to within ±1 dB of the actual implementation.

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10.2.2.4.2 SFDR Considerations

The SFDR of the amplifier is usually set by the second-order or third-order harmonic distortion for single-tone inputs, and by the second-order or third-order intermodulation distortion for two-tone inputs. Harmonics and second-order intermodulation distortion can be filtered to some degree, but third-order intermodulation spurs cannot be filtered. The ADC generates the same distortion products as the amplifier, but as a result of the sampling and clock feedthrough, additional spurs (not linearly related to the input signal) are included.

When the spurs from the amplifier and filter are known, each individual spur can be directly added to the same spur from the ADC, as shown in Equation 14, to estimate the combined spur (spur amplitudes in dBc):

$$HDx_{SYSTEM} = -20 \times \log\left(10^{\frac{-HDx_{AMP+FILTER}}{20}} + 10^{\frac{-HDx_{ADC}}{20}}\right) \quad (14)$$

This calculation assumes the spurs are in phase, but usually provides a good estimate of the final combined distortion.

For example, if the spur of the amplifier and filter equals the spur of the ADC, then the combined spur is 6 dB higher. To minimize the amplifier contribution (< 1 dB) to the overall system distortion, the spur from the amplifier and filter must be approximately 19 dB lower in amplitude than that of the converter. The combined spur calculated in this manner is usually accurate to within ±6 dB of the actual implementation; however, higher variations can be detected as a result of phase shift in the filter, especially in second-order harmonic performance.

This worst-case spur calculation assumes that the amplifier and filter spur of interest is in phase with the corresponding spur in the ADC, such that the two spur amplitudes can be added linearly. There are two phase-shift mechanisms that cause the measured distortion performance of the amplifier-ADC chain to deviate from the expected performance calculated using Equation 14: common-mode phase shift and differential phase shift.

Common-mode phase shift is the phase shift detected equally in both branches of the differential signal path including the filter. Common-mode phase shift nullifies the basic assumption that the amplifier, filter, and ADC spur sources are in phase. This phase shift can lead to better performance than predicted when the spurs become phase shifted, and there is the potential for cancellation when the phase shift reaches 180°. However, a significant challenge exists in designing an amplifier-ADC interface circuit to take advantage of a common-mode phase shift for cancellation: the phase characteristic of the ADC spur sources are unknown, thus the necessary phase shift in the filter and signal path for cancellation is also unknown.

Differential phase shift is the difference in the phase response between the two branches of the differential filter signal path. Differential phase shift in the filter as a result of mismatched components caused by nominal tolerance can severely degrade the even-order distortion of the amplifier-ADC chain. This effect has the same result as mismatched path lengths for the two differential traces, and causes more phase shift in one path than the other. Ideally, the phase response over frequency through the two sides of a differential signal path are identical, such that even-order harmonics remain optimally out of phase and cancel when the signal is taken differentially. However, if one side has more phase shift than the other, then the even-order harmonic cancellation is not as effective.

Single-order RC filters cause very little differential phase shift with nominal tolerances of 5% or less, but higher-order LC filters are very sensitive to component mismatch. For instance, a third-order Butterworth band-pass filter with a 100-MHz center frequency and a 20-MHz bandwidth creates as much as 20° of differential phase imbalance in a SPICE Monte Carlo analysis with 2% component tolerances. Therefore, although a prototype may work, production variance is unacceptable. In ac-coupled applications that require second- and higher-order filters between the LMH5401-SP and the ADC, a transformer or balun is recommended at the ADC input to restore the phase balance. For dc-coupled applications where a transformer or balun at the ADC input cannot be used, using first- or second-order filters is recommended to minimize the effect of differential phase shift because of the component tolerance.

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10.2.2.4.3 ADC Input Common-Mode Voltage Considerations—AC-Coupled Input

The input common-mode voltage range of the ADC must be respected for proper operation. In an ac-coupled application between the amplifier and the ADC, the input common-mode voltage bias of the ADC is accomplished in different ways depending on the ADC. Some ADCs use internal bias networks such that the analog inputs are automatically biased to the required input common-mode voltage if the inputs are ac-coupled with capacitors (or if the filter between the amplifier and ADC is a band-pass filter). Other ADCs supply their required input common-mode voltage from a reference voltage output pin (often called CM or V_{CM}). With these ADCs, the ac-coupled input signal can be re-biased to the input common-mode voltage by connecting resistors from each input to the CM output of the ADC, as Figure 68 shows. However, the signal is attenuated because of the voltage divider created by R_{CM} and R_O.

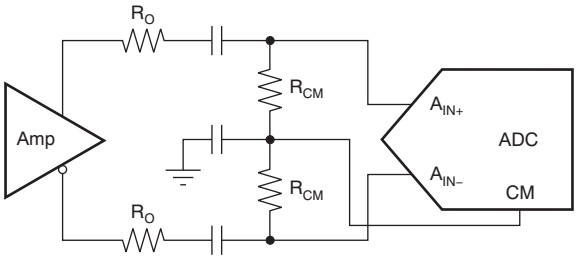

Figure 68. Biasing AC-Coupled ADC Inputs Using the ADC CM Output

The signal can be re-biased when ac coupling; thus, the output common-mode voltage of the amplifier is a *don't care* for the ADC.

10.2.2.4.4 ADC Input Common-Mode Voltage Considerations—DC-Coupled Input

DC-coupled applications vary in complexity and requirements, depending on the ADC. One typical requirement is resolving the mismatch between the common-mode voltage of the driving amplifier and the ADC. Devices such as the ADS5424 require a nominal 2.4-V input common-mode, whereas other devices such as the ADS5485 require a nominal 3.1-V input common-mode; still others such as the ADS6149 and the ADS4149 require 1.5 V and 0.95 V, respectively. As shown in Figure 69, a resistor network can be used to perform a common-mode level shift. This resistor network consists of the amplifier series output resistors and pull-up or pull-down resistors to a reference voltage. This resistor network introduces signal attenuation that may prevent the use of the full-scale input range of the ADC. ADCs with an input common-mode closer to the typical 2.5-V LMH5401-SP output common-mode are easier to dc-couple, and require little or no level shifting.

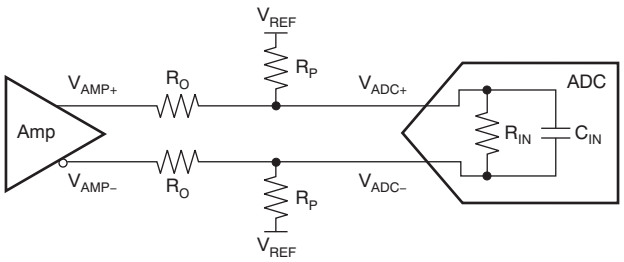

Figure 69. Resistor Network to DC Level-Shift Common-Mode Voltage

For common-mode analysis of the circuit in Figure 69, assume that $V_{AMP\pm} = V_{CM}$ and $V_{ADC\pm} = V_{CM}$ (the specification for the ADC input common-mode voltage). V_{REF} is chosen to be a voltage within the system higher than V_{CM} (such as the ADC or amplifier analog supply) or ground, depending on whether the voltage must be pulled up or down, respectively; R_O is chosen to be a reasonable value, such as 24.9 Ω. With these known values, R_P can be found by using Equation 15:

$$R_P = R_O \left(\frac{V_{ADC} - V_{REF}}{V_{AMP} - V_{ADC}} \right) \quad (15)$$

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Shifting the common-mode voltage with the resistor network comes at the expense of signal attenuation. Modeling the ADC input as the parallel combination of a resistance (R_{IN}) and capacitance (C_{IN}) using values taken from the ADC data sheet, the approximate differential input impedance (Z_{IN}) for the ADC can be calculated at the signal frequency. The effect of C_{IN} on the overall calculation of gain is typically minimal and can be ignored for simplicity (that is, $Z_{IN} = R_{IN}$). The ADC input impedance creates a divider with the resistor network; the gain (attenuation) for this divider can be calculated by Equation 16:

$$GAIN = \left(\frac{2R_P \parallel Z_{IN}}{2R_O + 2R_P \parallel Z_{IN}} \right) \quad (16)$$

With ADCs that have internal resistors that bias the ADC input to the ADC input common-mode voltage, the effective R_{IN} is equal to twice the value of the bias resistor. For example, the ADS5485 has a 1-kΩ resistor tying each input to the ADC V_{CM}; therefore, the effective differential R_{IN} is 2 kΩ.

The introduction of the R_P resistors also modifies the effective load that must be driven by the amplifier. Equation 17 shows the effective load created when using the R_P resistors.

$$R_L = 2R_O + 2R_P \parallel Z_{IN} \quad (17)$$

The R_P resistors function in parallel to the ADC input such that the effective load (output current) at the amplifier output is increased. Higher current loads limit the LMH5401-SP differential output swing.

By using the gain and knowing the full-scale input of the ADC ($V_{ADC\ FS}$), the required amplitude to drive the ADC with the network can be calculated using Equation 18:

$$V_{AMP\ PP} = \frac{V_{ADC\ FS}}{GAIN} \quad (18)$$

As with any design, testing is recommended to validate whether the specific design goals are met.

10.2.2.5 GSPS ADC Driver

The LMH5401-SP can drive the full Nyquist bandwidth of ADCs with sampling rates up to 4 GSPS, as shown in Figure 70. If the front-end bandwidth of the ADC is more than 2 GHz, use a simple noise filter to improve SNR. Otherwise, the ADC can be connected directly to the amplifier output pins. Matching resistors may not be required, however allow space for matching resistors on the preliminary design.

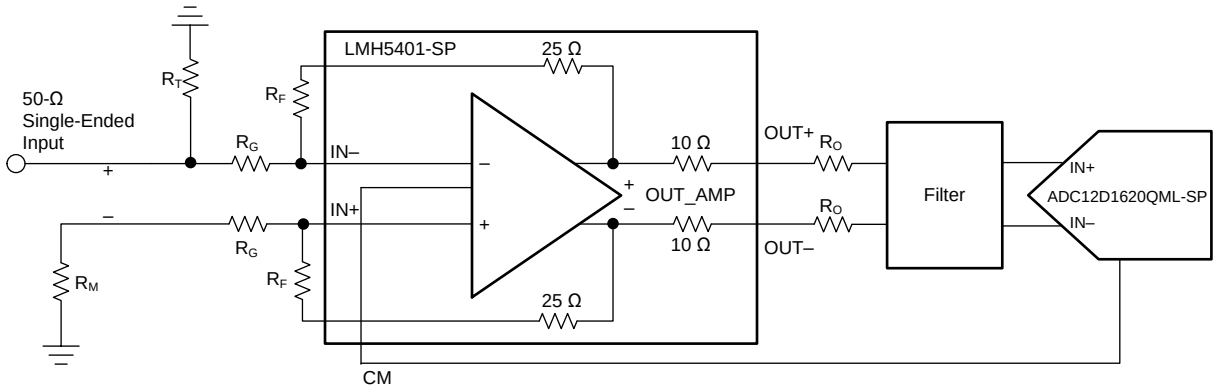

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Figure 70. GSPS ADC Driver

10.2.2.6 Common-Mode Voltage Correction

The LMH5401-SP can set the output common-mode voltage to within a typical value of ±30 mV. If greater accuracy is desired, a simple circuit can improve this accuracy by an order of magnitude. A precision, low-power operational amplifier is used to sense the error in the output common-mode of the LMH5401-SP and corrects the error by adjusting the voltage at the CM pin. In Figure 71, the precision of the op amp replaces the less accurate precision of the LMH5401-SP common-mode control circuit while still using the LMH5401-SP common-mode control circuit speed. The op amp in this circuit must have better than a 1-mV input-referred offset voltage and low noise. Otherwise the specifications are not very critical because the LMH5401-SP is responsible for the entire differential signal path.

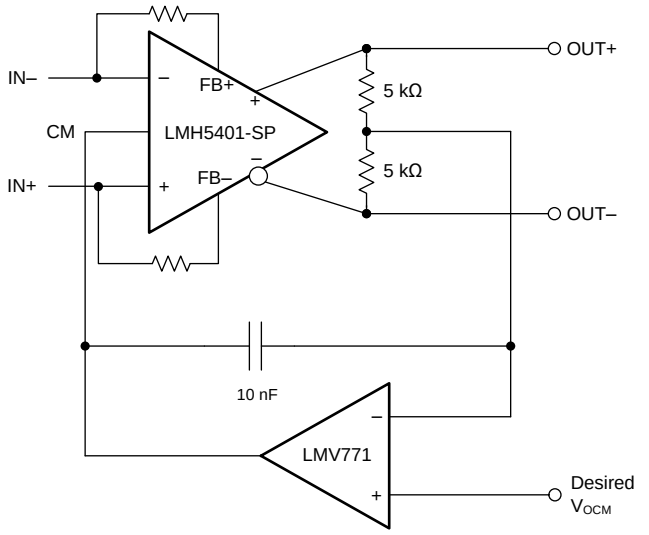

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Figure 71. Common-Mode Correction Circuit

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10.2.2.7 Active Balun

The LMH5401-SP is designed to convert single-ended signals to a differential output with very high bandwidth and linearity, as shown in Figure 72. The LMH5401-SP can support dc coupling as well as ac coupling. The LMH5401-SP is smaller than any balun with low-frequency response and has excellent amplitude and phase balance over a wide frequency range. As shown in Figure 73, the LMH5401-SP amplitude imbalance is near 0 dB up to 1 GHz when used with a 5-V supply. Figure 75 plots all S-parameters showing superior wideband input and output return loss compared to many baluns.

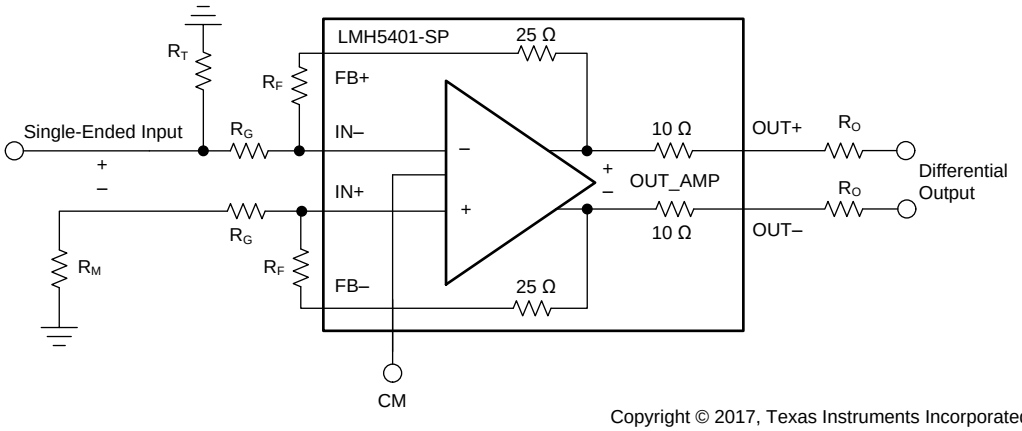

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Figure 72. Active Balun

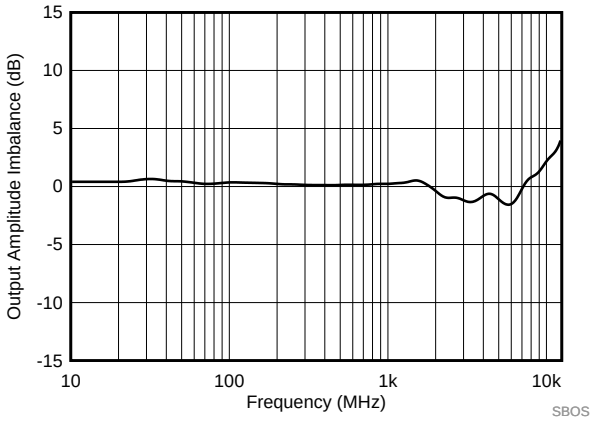

Figure 73. SE-DE Amplitude Imbalance

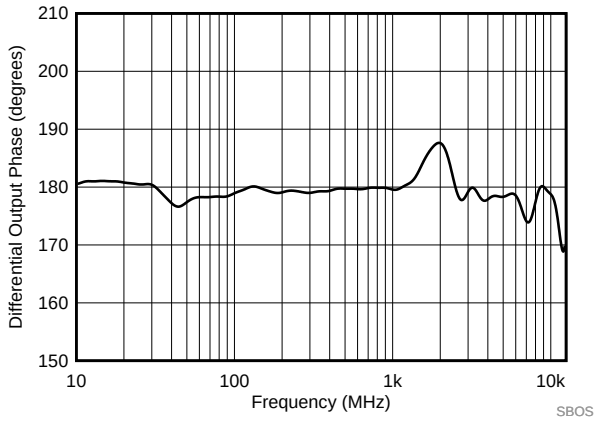

Figure 74. SE-DE Phase Imbalance

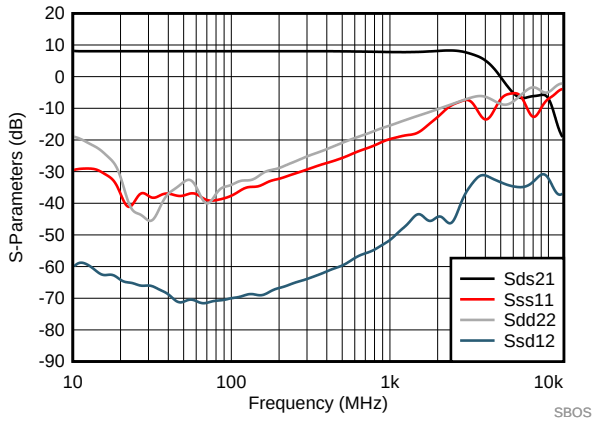

Figure 75. SE-DE Small Signal S-Parameters

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10.2.3 Application Curves

The LMH5401-SP has on-chip series output resistors to isolate the output of the amplifier. These resistors provide the LMH5401-SP extra phase margin in most applications. When the amplifier is used to drive a terminated transmission line or a controlled impedance filter, additional external resistance is required to match the transmission line of the filter. In these matched applications, there is a 6-dB loss of gain. When the LMH5401-SP is used to drive loads that are not back-terminated or matched, there is a loss in gain resulting from the on-chip resistors. Figure 76 shows that loss for different load conditions. In most cases the loads are between 50 Ω and 200 Ω, where the on-chip resistor losses are 1.6 dB and 0.42 dB, respectively. As an example, if the LMH5401-SP were to drive an ADC with a differential input impedance of 100 Ω without any matching components the signal loss would be 0.83 dB compared to 6 dB in a matched configuration. Of course, this is only feasible if the LMH5401-SP and the ADC are placed in close proximity (< 1/4 wavelength of the frequency of interest) so as to avoid standing waves from reflections due to the mismatch in impedances). Figure 77 shows the net gain realized by the amplifier for a large range of load resistances when the LMH5401-SP is configured for 16-dB gain.

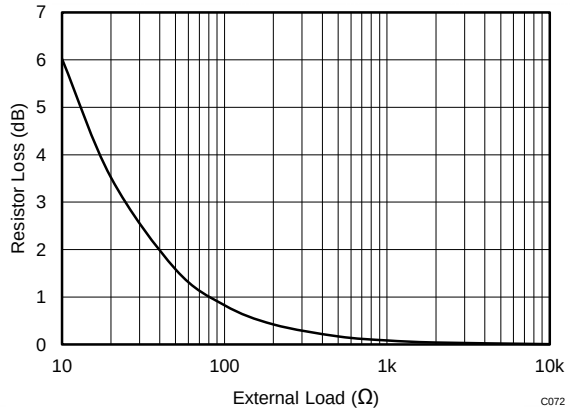

Figure 76. Gain Loss Resulting from On-Chip Output Resistors

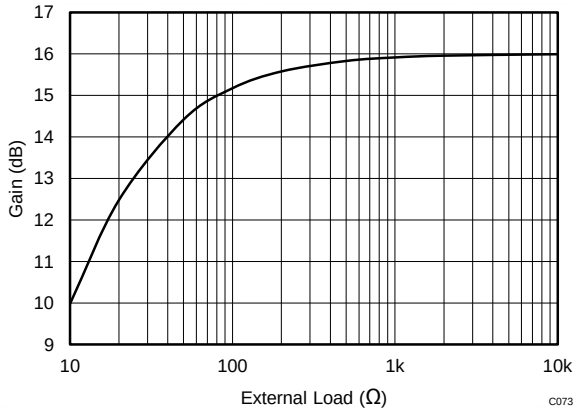

Figure 77. Net Gain versus Load Resistance

10.3 Do's and Don'ts

10.3.1 Do:

- Include a thermal design at the beginning of the project.
- Use well-terminated transmission lines for all signals.
- Use solid metal layers for the power supplies.
- Keep signal lines as straight as possible.
- Use split supplies where required.

10.3.2 Don't:

- Use a lower supply voltage than necessary.
- Use thin metal traces to supply power.
- Forget about the common-mode response of filters and transmission lines.

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11 Power Supply Recommendations

The LMH5401-SP can be used with either split or single-ended power supplies. The ideal supply voltage is a 5-V total supply, split around the desired common-mode of the output signal swing. For example, if the LMH5401-SP is used to drive an ADC with a 1-V input common mode, then the ideal supply voltages are 3.5 V and –1.5 V. The GND pin can then be connected to the system ground and the PD pin is ground referenced.

11.1 Supply Voltage

Using a 5-V power supply gives the best balance of performance and power dissipation. If power dissipation is a critical design criteria, a power supply as low as 3.3 V (±1.65) can be used. When using a lower power supply, the input common-mode and output swing capabilities are drastically reduced. Make sure to study the common-mode voltages required before deciding on a lower-voltage power supply. In most cases the extra performance achieved with 5-V supplies is worth the power.

11.2 Single Supply

Single-supply voltages from 3.3 V to 5 V are supported. When using a single supply check both the input and output common-mode voltages that are required by the system.

11.3 Split Supply

In general, split supplies allow the most flexibility in system design. To operate as split supply, apply the positive supply voltage to VS+, the negative supply voltage to VS–, and the ground reference to GND. Note that supply voltages do not need to be symmetrical. Provided the total supply voltage is between 3.3 V and 5.25 V, any combination of positive and negative supply voltages is acceptable. This feature is often used when the output common-mode voltage must be set to a particular value. For best performance, the power-supply voltages are symmetrical around the desired output common-mode voltage. The input common-mode voltage range is much more flexible than the output.

11.4 Supply Decoupling

Power-supply decoupling is critical to high-frequency performance. Onboard bypass capacitors are used on the LMH5401-SPEVM; however, the most important component of the supply bypassing is provided by the PCB. As illustrated in Figure 78, there are multiple vias connecting the LMH5401-SP power planes to the power-supply traces. These vias connect the internal power planes to the LMH5401-SP. Both VS+ and VS– must be connected to the internal power planes with several square centimeters of continuous plane in the immediate vicinity of the amplifier. The capacitance between these power planes provides the bulk of the high-frequency bypassing for the LMH5401-SP.

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12 Layout

12.1 Layout Guidelines

With a GBP of 6.5 GHz, layout for the LMH5401-SP is critical and nothing can be neglected. In order to simplify board design, the LMH5401-SP has on-chip resistors that reduce the affect of off-chip capacitance. For this reason, TI recommends that the ground layer below the LMH5401-SP not be cut. The recommendation not to cut the ground plane under the amplifier input and output pins is different than many other high-speed amplifiers, but the reason is that parasitic inductance is more harmful to the LMH5401-SP performance than parasitic capacitance. By leaving the ground layer under the device intact, parasitic inductance of the output and power traces is minimized. The DUT portion of the evaluation board layout is illustrated in Figure 78.

The EVM uses long-edge capacitors for the decoupling capacitors, which reduces series resistance and increases the resonant frequency. Vias are also placed to the power planes before the bypass capacitors. Although not evident in the top layer, two vias are used at the capacitor in addition to the two vias underneath the device.

The output matching resistors are 0402 size and are placed very close to the amplifier output pins, which reduces both parasitic inductance and capacitance. The use of 0603 output matching resistors produces a measurable decrease in bandwidth.

When the signal is on a 50-Ω controlled impedance transmission line, the layout then becomes much less critical. The transition from the 50-Ω transmission line to the amplifier pins is the most critical area.

The CM pin also requires a bypass capacitor. Place this capacitor near the device. Refer to the user guide *LMH5401EVM-CVAL evaluation module*, (SLOU478) for more details on board layout and design.

12.2 Layout Example

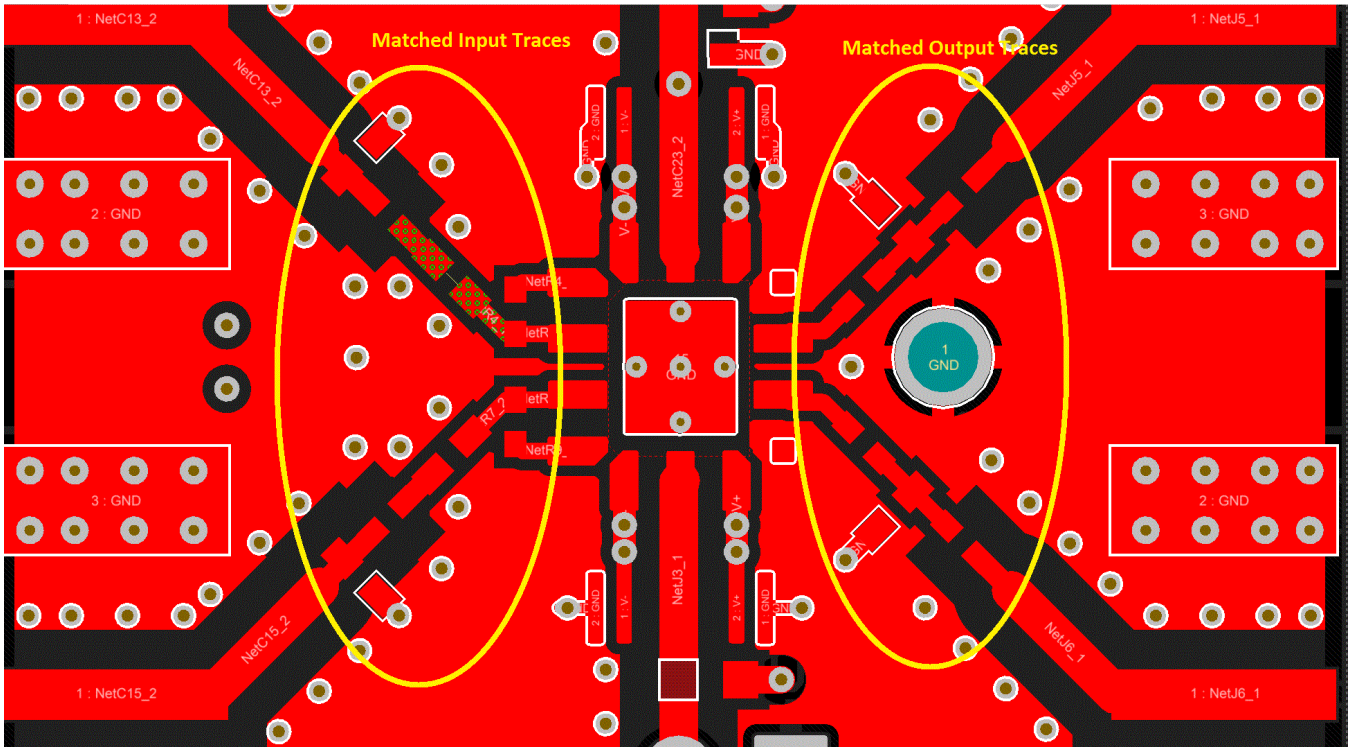

Figure 78. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Device Nomenclature

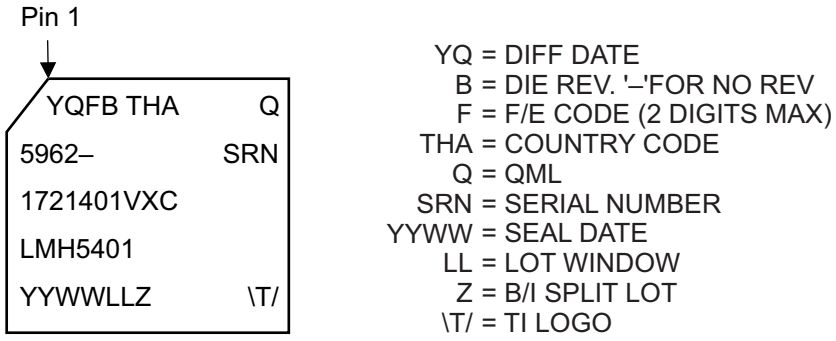

Figure 79. Device Marking Information

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *ADC12D1x00 12-Bit, 2.0/3.2 GSPS ultra high-speed ADC*, SNAS480
- *ADC12D1620QMP-SP 12-bit, single or dual, 3200- or 1600-MSPS RF sampling ADC*, SNAS717
- *Rad-tolerant class V, wideband, fully differential amplifier*, SLOS538
- *Rad-tolerant class V, wideband, fully differential amplifier*, SLOS539
- *LMH5401-SP TINA models*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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13.5 Trademarks

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Rohde & Schwarz is a registered trademark of Rohde & Schwarz.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-1721401VXC	Active	Production	LCCC (FFK) | 14	25 | TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-1721401VXC LMH5401
5962-1721401VXC.A	Active	Production	LCCC (FFK) | 14	25 | TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962-1721401VXC LMH5401
5962R1721401VXC	Active	Production	LCCC (FFK) | 14	25 | TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962R 1721401VXC LMH5401
5962R1721401VXC.A	Active	Production	LCCC (FFK) | 14	25 | TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	5962R 1721401VXC LMH5401
LMH5401FFK/EM	Active	Production	LCCC (FFK) | 14	25 | TUBE	No	Call TI	N/A for Pkg Type	25 to 25	LMH5401FFK /EM
LMH5401FFK/EM.A	Active	Production	LCCC (FFK) | 14	25 | TUBE	No	Call TI	N/A for Pkg Type	25 to 25	LMH5401FFK /EM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

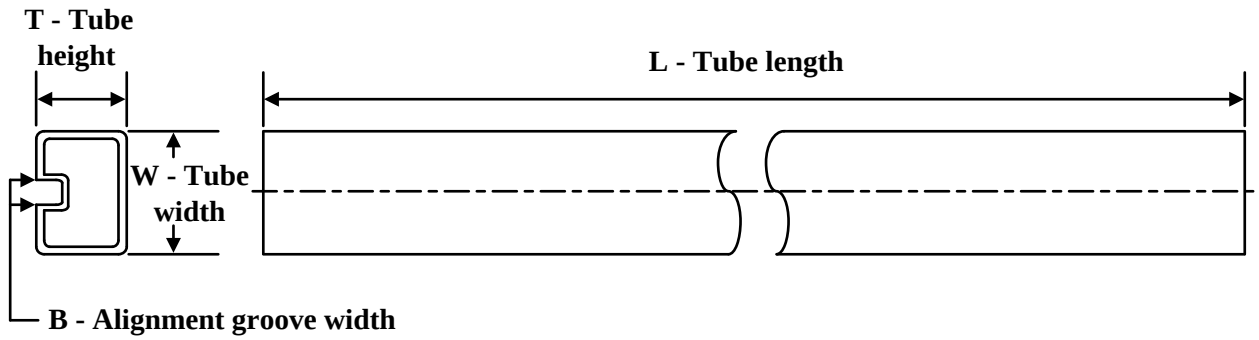
OTHER QUALIFIED VERSIONS OF LMH5401-SP :

- Catalog : LMH5401

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TUBE



*All dimensions are nominal

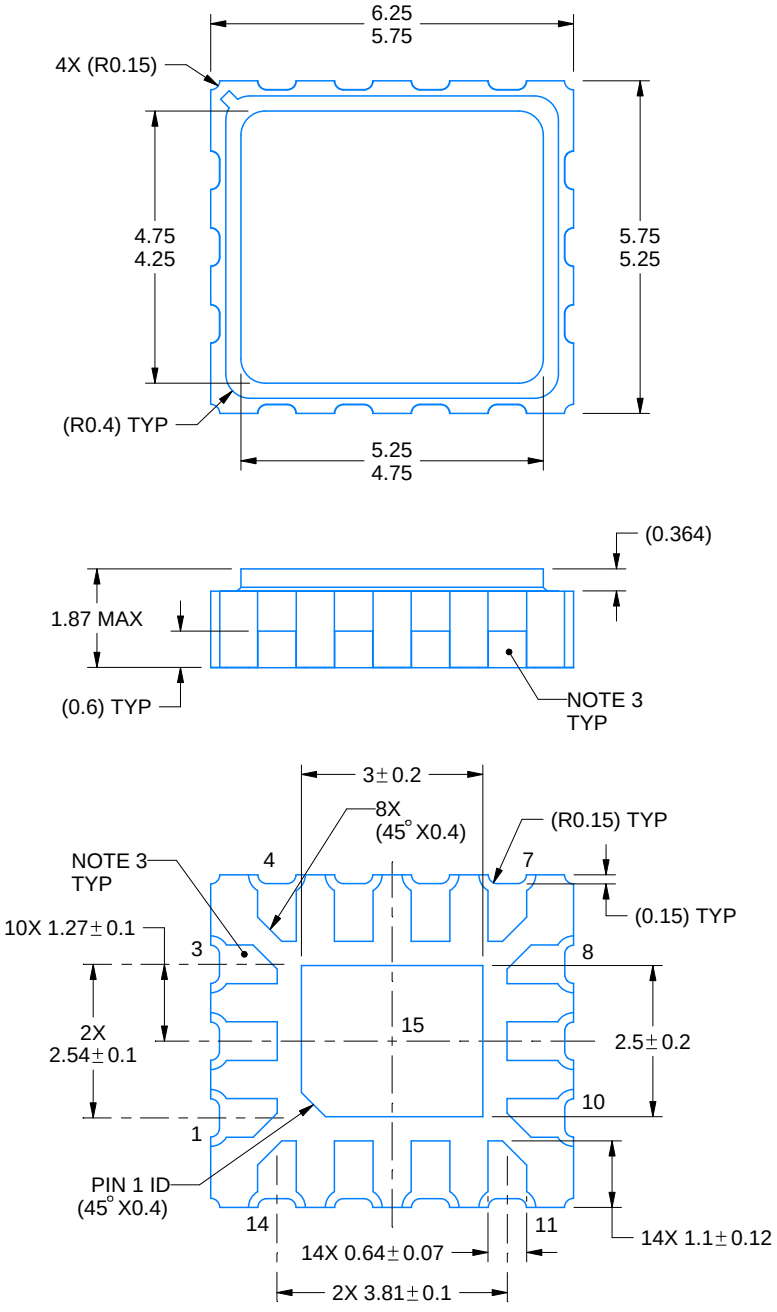
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1721401VXC	FFK	LCCC	14	25	506.98	26.16	6220	NA
5962-1721401VXC.A	FFK	LCCC	14	25	506.98	26.16	6220	NA
5962R1721401VXC	FFK	LCCC	14	25	506.98	26.16	6220	NA
5962R1721401VXC.A	FFK	LCCC	14	25	506.98	26.16	6220	NA
LMH5401FFK/EM	FFK	LCCC	14	25	506.98	26.16	6220	NA
LMH5401FFK/EM.A	FFK	LCCC	14	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

FFK0014A

LCCC - 1.87 mm max height

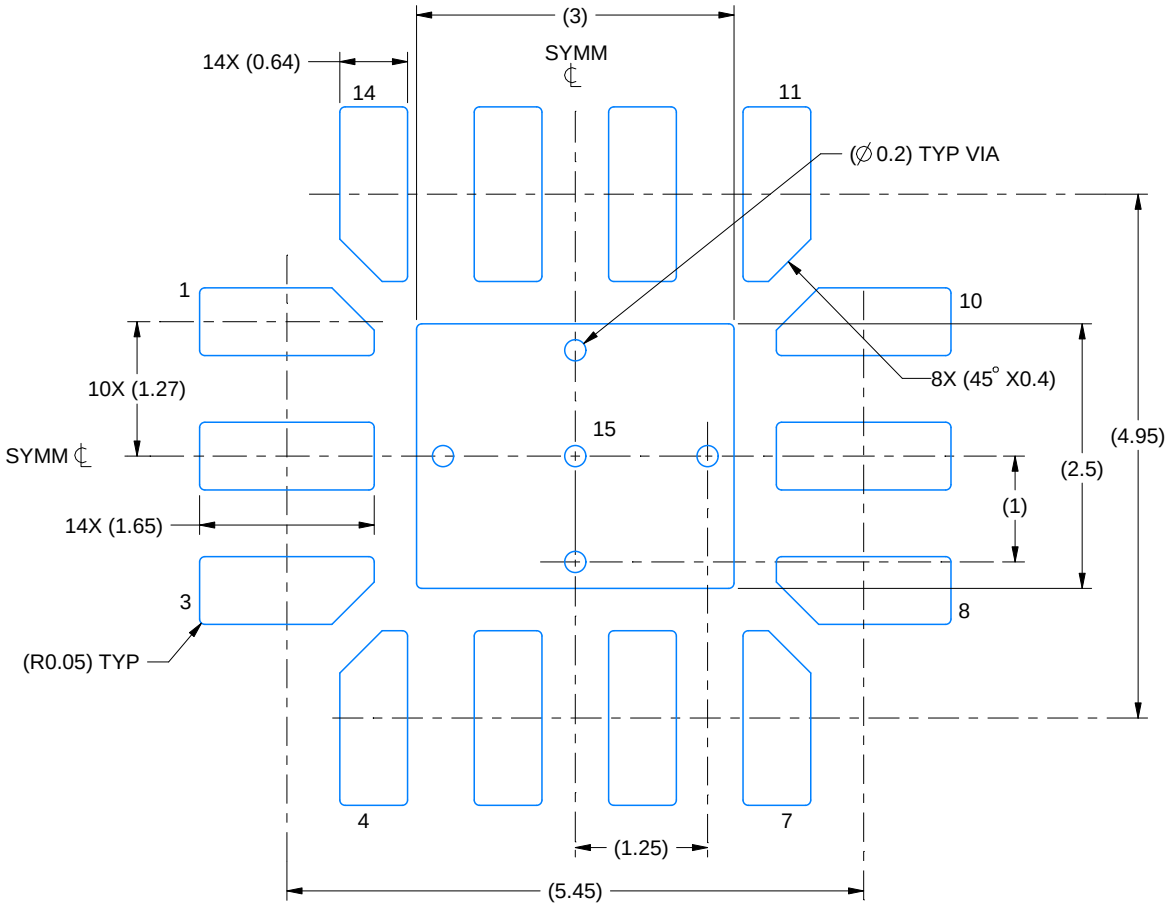
LEADLESS CERAMIC CHIP CARRIER



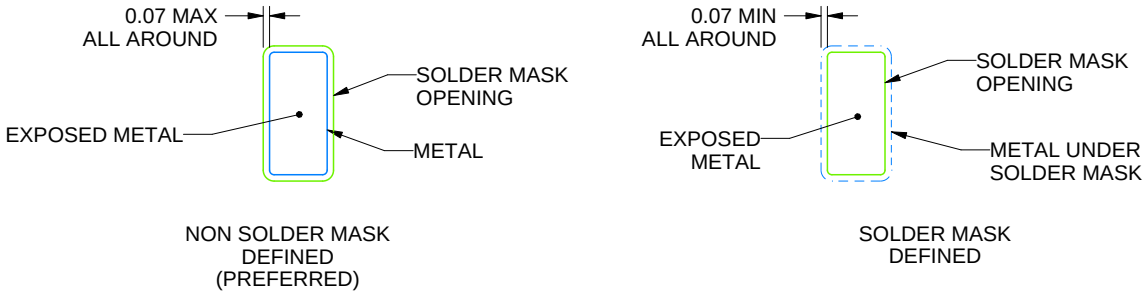
4223813/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The terminals are gold-plated.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 14X



SOLDER MASK DETAILS
NOT TO SCALE

4223813/B 04/2018

NOTES: (continued)

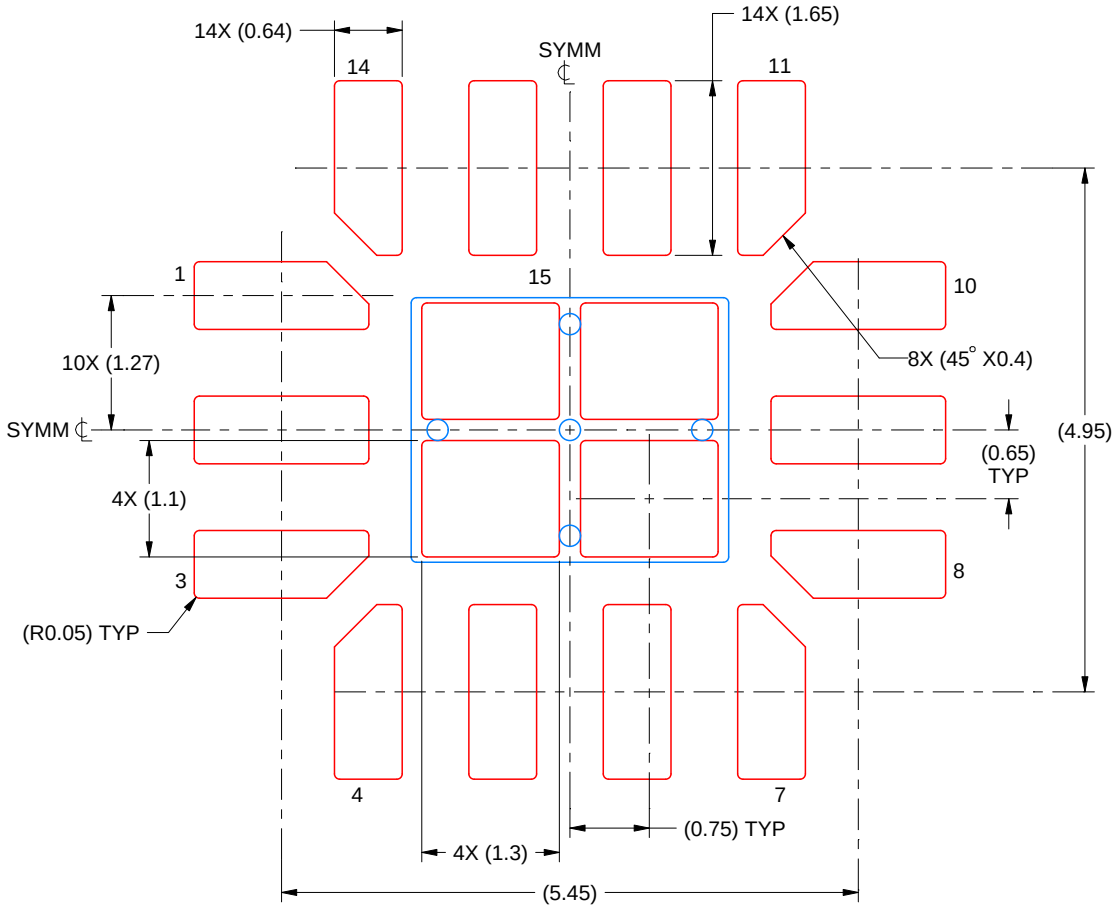
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

FFK0014A

LCCC - 1.87 mm max height

LEADLESS CERAMIC CHIP CARRIER



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15:
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 14X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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