*EVM User's Guide: PGA849EVM*

# *PGA849 Evaluation Module*

## Description

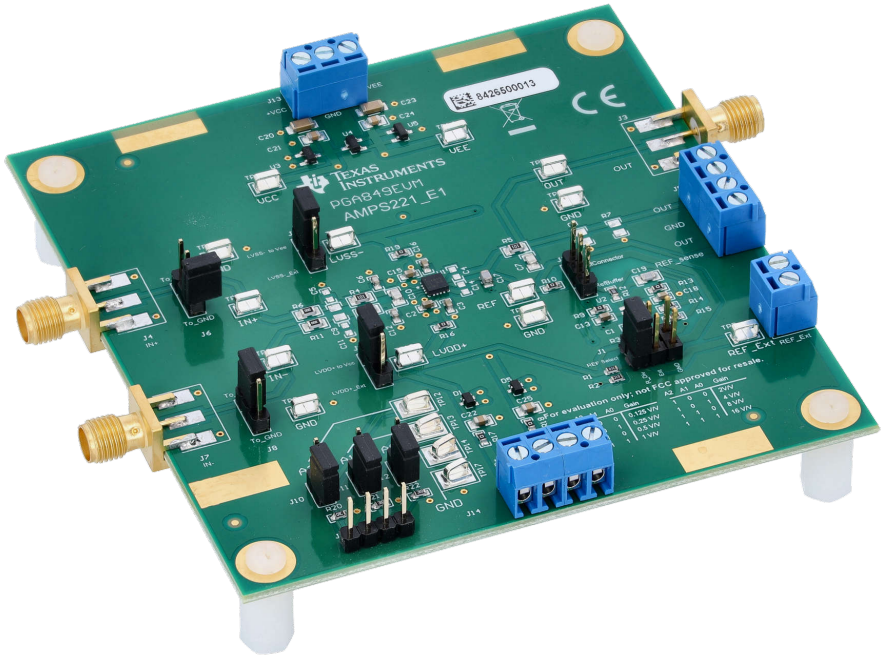
The PGA849 is a precision, wide-bandwidth programmable gain instrumentation amplifier (PGA) for differential to single ended conversion optimized to drive high-performance analog-to-digital converters (ADCs) with sampling rates up to 1 MSPS without the need for an additional ADC driver. The PGA849 is equipped with eight binary gain settings, from an attenuating gain of 0.125V/V to a maximum of 16V/V, using three digital gain-selection pins. The device features super-beta input transistors from Texas Instruments, which provide ultra-low input offset voltage, offset drift, low input bias current, input voltage noise, and current noise.

## Features

- Quick and simple evaluation of PGA849; provides access to features and measures performance
- PGA can be configured with binary gain settings from 0.125V/V to 16V/V
- Provides three shunt jumpers to set the PGA849 gain-control selection pins
- Sub-miniature version A (SMA) connectors and test points allow for quick tests
- Evaluation board incorporates an optional REF pin op-amp buffer for flexibility
- Independent input and output power supply connections to allow for ADC input overdrive protection

## Applications

- Factory automation and control
- Analog input module
- Data acquisition
- Test and measurement
- Semiconductor test



# 1 Evaluation Module Overview

## 1.1 Introduction

This user's guide contains information and support documentation for the PGA849 evaluation module (EVM). Included are the circuit description, jumper settings, required connections, printed circuit board (PCB) layout, schematic, and bill of materials of the PGA849EVM. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the PGA849EVM.

## 1.2 Kit Contents

**Table 1-1. PGA849EVM Kit Contents**

| Item | Description | Quantity |
|---|---|---|
| PGA849EVM | PCB | 1 |

## 1.3 Specification

For a full list of the electrical characteristics for the PGA849, see the PGA849 *Low-Noise, Wide-Bandwidth, Precision Programmable-Gain Instrumentation Amplifier* data sheet.

## 1.4 Device Information

The EVM is built with the PGA849RGT device in the 16-pin VQFN package with the thermal pad.

This EVM provides access to the features and measures the performance of the PGA849 device. The PGA849 is equipped with eight binary gain settings, from an attenuating gain of 0.125V/V to a maximum of 16V/V, using three digital gain selection pins. By default, the PGA849EVM programmable gain amplifier is configured to a gain of 0.125V/V. The evaluation board provides shunt jumpers J10, J11, and J12 to set the PGA849 gain.

# 2 Hardware

## 2.1 EVM Circuit Description

The device uses two sets of voltage supplies: input stage and output stage. The output-stage power supplies are decoupled from the input stage to limit the PGA849 output-swing voltage level protecting the ADC or downstream device against overdrive damage. The input-stage supplies, VS+ and VS–, are accessible using connector J13. The output-stage supplies, LVDD+ and LVSS–, are accessible using connector J14. Selectable jumpers J9 and J16 set the output-stage supply voltage level equal to the input-stage supplies (default), or to external voltages using connector J14.

The PGA849 incorporates features that simplify interfacing to a single-ended or pseudo-differential input ADC. The REF pin sets the reference point for the output voltage of the PGA849. The REF pin must be driven with a low-impedance source, and the evaluation board provides an optional buffer (U2) to drive the REF pin. Selectable jumper J1 provides options to set the REF pin voltage externally through connector J2, connects the REF to GND, or sets the REF to the PGA849 output-stage supplies (LVDD+ and LVSS–) mid-voltage value. The PGA849EVM allows access to the DA_IN– and DA_IN+ pins with optional capacitors C4 and C14. These capacitors are in parallel with the PGA849 output-stage difference amplifier internal resistors to implement noise filtering. Figure 2-1 displays a simplified block diagram of the PGA849EVM. For a full schematic of the PGA849EVM, see Figure 3-1.

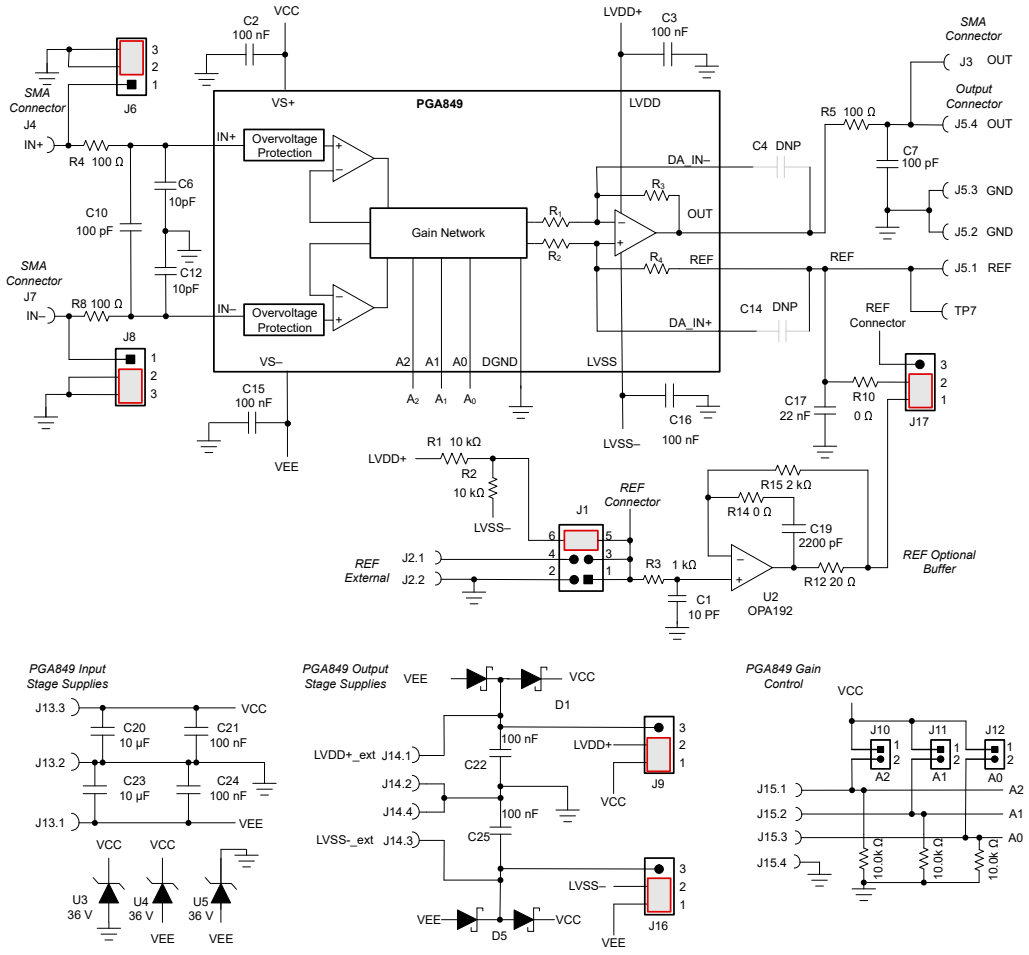



**Figure 2-1. PGA849EVM Simplified Schematic**

## 2.2 Jumper Settings

Figure 2-2 details the default jumper settings of the PGA849EVM. Table 2-1 explains the configuration for these jumpers.

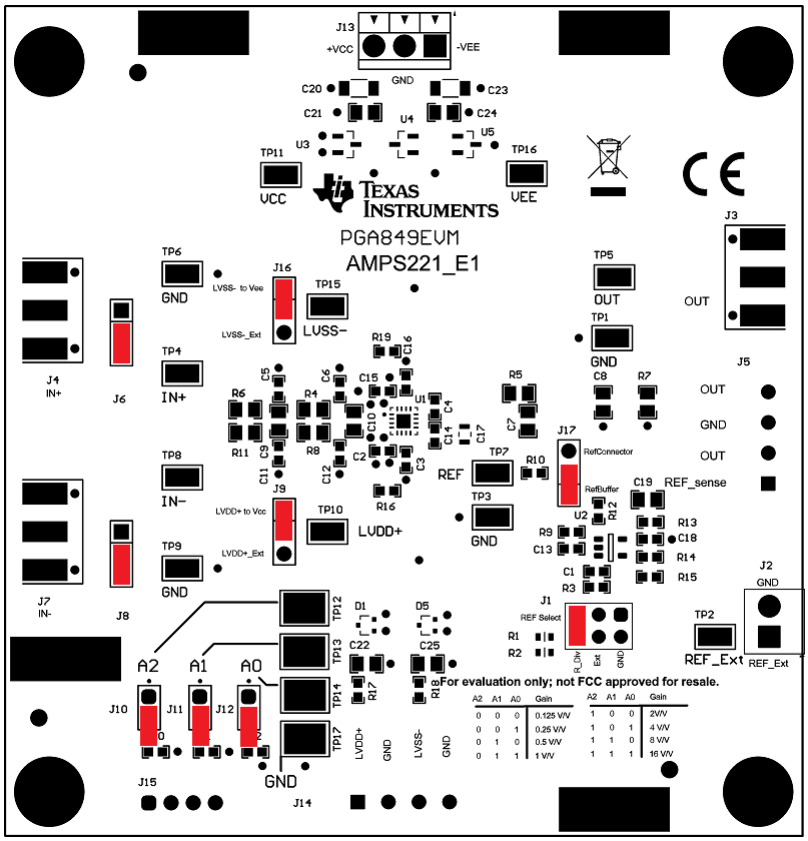



**Figure 2-2. PGA849EVM Default Jumper Settings**

**Table 2-1. Default Jumper Configuration**

| Jumper | Function | Default Position | Description |
|---|---|---|---|
| J1 | REF Select | Shunt 5-6 | Shunt 5-6: Sets REF to mid output stage supply<br>Shunt 3-4: Sets REF to Ext. REF connector J2<br>Shunt 1-2: Sets REF to GND |
| J17 | REF Buffer/Connector | Shunt 1-2 | Shunt 1-2: REF pin to REF buffer output<br>Shunt 2-3: REF pin to REF connector |
| J6 | Positive (noninverting) input, IN+ | Shunt 2-3 | Shunt 2-3: Input signal to SMA connector J3<br>Shunt 1-2: connects IN+ to GND |
| J8 | Negative (inverting) input, IN– | Shunt 2-3 | Shunt 2-3: Input signal to SMA connector J6<br>Shunt 1-2 connects IN– to GND |
| J9 | LVDD+ connection | Shunt 1-2 | Shunt 1-2: Sets output stage supply LVDD+ to +VCC supply<br>Shunt 2-3 connects LVDD+ to external connector J14 pin 1 |
| J16 | LVSS– connection | Shunt 1-2 | Shunt 1-2: Sets output stage supply LVDD- to –VEE supply<br>Shunt 2-3 connects LVDD– to external connector J14 pin 3 |
| J10 | PGA gain CTRL A2 | Open | Open: Sets A2 to GND or 0<br>Shunt 1-2: Sets A2 to VCC or 1 |
| J11 | PGA gain CTRL A1 | Open | Open: Sets A1 to GND or 0<br>Shunt 1-2: Sets A1 to VCC or 1 |
| J12 | PGA gain CTRL A0 | Open | Open: Sets A0 to GND or 0<br>Shunt 1-2: Sets A0 to VCC or 1 |

## 2.3 Power-Supply Connections

The PGA849EVM uses two sets of voltage supplies: input stage and output stage. The device operates using input-stage power supplies from ±4V (8V) to ±18V (36V) and output-stage power supplies from ±2.25V (4.5V) to ±18V (36V). The output-stage supply voltage must not exceed the input-stage supply voltage.

The input-stage power-supply connections for the PGA849EVM are provided through connector J13 at the top of the EVM. The input-stage positive power-supply connection is labeled +VCC, the negative power-supply connection is labeled –VEE, and the ground connection is labeled GND. To connect power to the PGA849EVM, insert wires into each terminal of J13 and then tighten the screws to make the connection. Table 2-2 summarizes the pin definition for supply connector J1 and the allowed voltage range for each supply connection.

**Table 2-2. PGA849EVM Supply-Range Specifications**

| Connector Pin Number | Supply Connection | Voltage Range |
|---|---|---|
| J13.3 | Input-stage positive supply (+VCC) | Single supply, $V_S$ = +VCC: 8V to 36V<br>Dual supply, $V_S$ = (+VCC) – (–VEE): 4V to 18V |
| J13.2 | Ground | 0V |
| J13.1 | Negative supply (–VEE) | Single supply, $V_S$ = +VCC: 0V (GND)<br>Dual supply, $V_S$ = (+VCC) – (–VEE): –4 V to –18 V |
| J14.1 | LVDD+_ext | Single supply, LVDD+_ext: 4.5V to 36V<br>Dual supply, output stage supply (LVSS+) – (LVSS–): 2.25V to 18V |
| J14.2 | Ground | 0V |
| J14.3 | LVSS–_ext | Single supply, LVSS–_ext: 0V (GND)<br>Dual supply, output stage supply (LVSS+) – (LVSS–): –2.25V to –18V |
| J14.4 | Ground | 0V |

By default, the output-stage supply-voltage levels (+LVDD and –LVSS) are set to the PGA849 positive (+VCC) and negative (–VEE) supplies, respectively. The +LVDD pin is connected to +VCC through jumper J9 1-2, and the –LVSS pin is connected to –VEE through J16 1-2. Screw terminal connector J14 provides access to the output-stage supply pins. To set the voltage level of LVDD and LVSS with an external supply, shunt jumper J9 2-3 to access the +LVDD using connector J14.1. In a similar fashion, shunt jumper J16 2-3 to access the –LVSS pin using connector J14.3.

Figure 2-3 shows the PGA849EVM voltage supply connections.

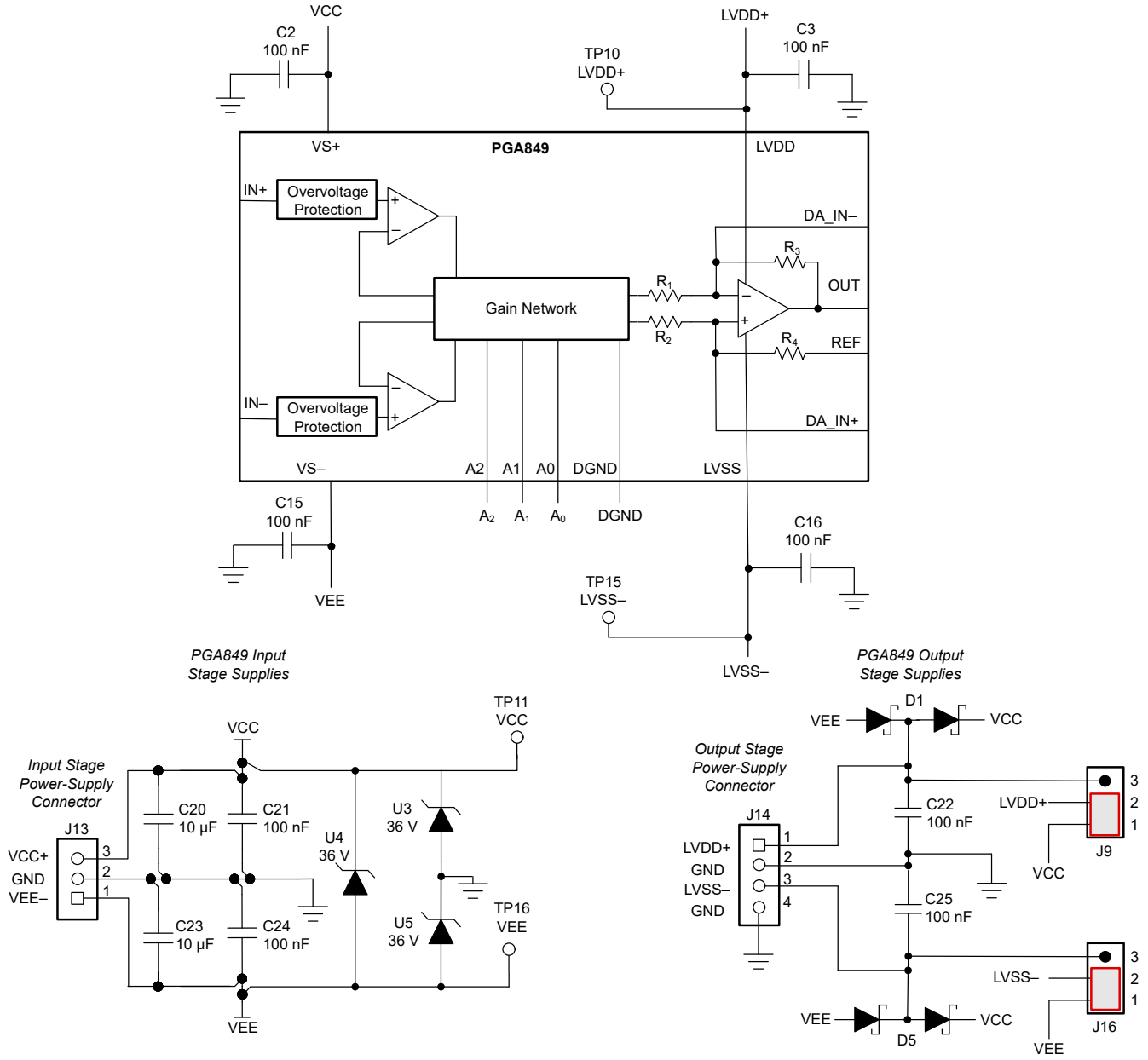



**Figure 2-3. PGA849EVM Voltage Supply Connections**

## 2.4 Analog Input and Output Connections

The programmable amplifier input signal connections for the PGA849EVM are provided through the use of SMA connectors J4, J7, and test points TP4, TP8, located at the left of the EVM. The REF external input is provided through screw-terminal connector J2, located at the right of the board. The PGA849EVM also provides direct access to the REF pin through screw-terminal connector J5.1, and test point TP7 located at the right of the board.

The PGA849 output amplifier connection is provided through screw-terminal connector J5.4, SMA connector J3, and test point TP5, located at the right side of the EVM. Figure 2-4 displays a simplified diagram of the PGA849EVM input and output connections.

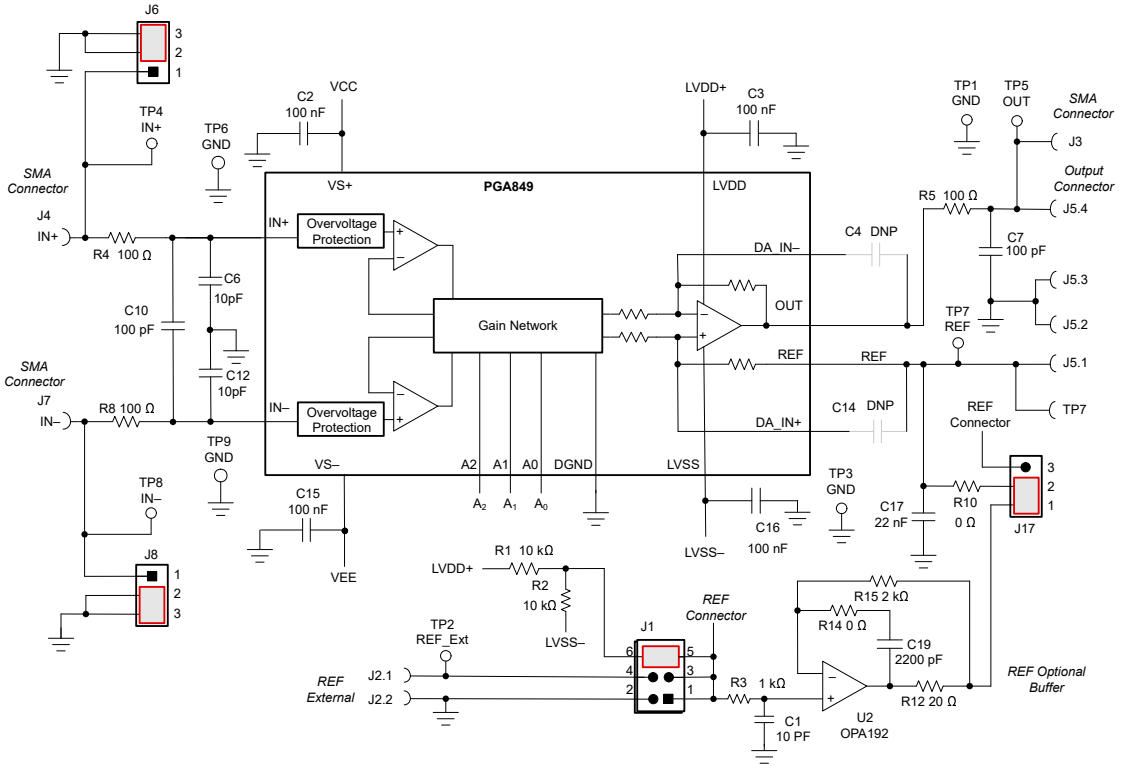



**Figure 2-4. PGA849EVM Analog Input and Output Connections**

Table 2-3 summarizes the input and output connectors and corresponding test points.

**Table 2-3. PGA849EVM Analog Input and Output Connections**

| Connector Designator | Signal | Comment | Test Point |
|---|---|---|---|
| J4 | IN+ | SMA | TP4 |
| J7 | IN– | SMA | TP8 |
| J3 | OUT | SMA | TP3 |
| J5.4 | OUT | Screw terminal | TP3 |
| J5.3 | GND | Screw terminal | TP2 |
| J5.2 | GND | Screw terminal | TP9 |
| J5.1 | REF pin / REF_sense | Screw terminal | TP7 |
| J2.1 | REF_Ext | Screw terminal | TP2 |
| J2.2 | GND | Screw terminal | N/A |

## 2.5 Reference Input

The output voltage of the PGA849 is developed with respect to the voltage on reference pin REF. Use the REF pin to offset the output signal to a precise voltage level. Typically, this offset is set to the mid-voltage level of the output-stage supplies. To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the PGA849 drives a single-supply ADC. For bipolar voltage output-stage supply operation, the REF pin is typically connected to the low-impedance system ground.

The voltage source applied to the reference pin must provide a low output impedance. Any resistance at the reference pin is in series with an internal 5kΩ resistor that creates an imbalance in the four resistors of the internal difference amplifier. The PGA849EVM provides an optional reference buffer through the OPA192 op-amp (U2). This buffer provides a low-impedance path when driving the REF pin with external reference sources.

Connector J2.1 of the EVM provides access for external reference sources. For best performance, use a low-noise, low-drift, precision reference when driving the REF pin with an external source. To connect the buffer to the external reference source, insert wires into each terminal of J2 and then tighten the screws to make the connection.

To set the REF to the external reference, shunt jumper J1 4-3. In similar fashion, shunt jumper J1 1-2 to set REF to GND. Alternatively, shunt jumper J1 5-6 to set the REF to mid-supply level of the output-stage supplies through the R1-R2 voltage divider.

To bypass the buffer and access the REF pin directly, shunt jumper J17 2-3.

By default, the buffer drives the REF pin, and the reference is set to mid-supply level of the output stage supplies. Jumper J17 is set to shunt pins 1-2, and Jumper J1 is set to shunt pins 5-6. Figure 2-5 shows the REF input connections and optional REF buffer.

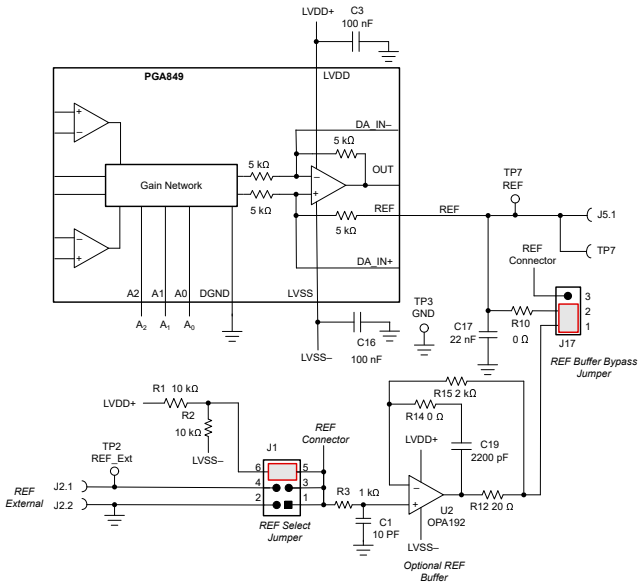



**Figure 2-5. PGA849EVM Reference Input and Optional Buffer**

**Note**

When using the optional REF buffer, the REF input signal must allow headroom above and below the op-amp supplies. Use a reference input voltage in the range of (LVSS-) + 300mV < REF_ext < (LVDD+) -300mV to remain within a good OPA192 output swing linear range. Exceeding the op-amp linear range results in degraded linearity performance of the PGA849 circuit.

## 2.6 Digital Input Pins and Gain Control

The PGA849 provides eight binary gain settings, from an attenuating gain of 0.125V/V to a maximum of 16V/V. The gain is controlled by three digital selection pins: A0, A1, and A2. By default, the PGA849 is configured to a gain of 0.125V/V.

The evaluation board provides shunt jumpers J10, J11, and J12 to set the PGA849 gain-control selection pins. Table 2-4 lists the gain-control options. To set the gain-control pin high, install the shunt on the corresponding jumper. To set the gain-control pin low, remove the shunt jumper.

**Table 2-4. PGA849EVM Gain Control**

| A2<br>Jumper J10<br>Connector J15.1 | A1<br>Jumper J11<br>Connector J15.2 | A0<br>Jumper J12<br>Connector J15.3 | PGA Gain (V/V) |
|---|---|---|---|
| Low (Open) | Low (Open) | Low (Open) | 0.125 |
| Low (Open) | Low (Open) | High (Shunt) | 0.25 |
| Low (Open) | High (Shunt) | Low (Open) | 0.5 |
| Low (Open) | High (Shunt) | High (Shunt) | 1 |
| High (Shunt) | Low (Open) | Low (Open) | 2 |
| High (Shunt) | Low (Open) | High (Shunt) | 4 |
| High (Shunt) | High (Shunt) | Low (Open) | 8 |
| High (Shunt) | High (Shunt) | High (Shunt) | 16 |

Alternatively, the A0, A1, and A2 digital pins can be driven externally through connector J15. Any pin that is not driven by an external source, or any shunt that is left open, is biased at DGND using pulldown resistors. Figure 2-6 shows the gain-setting block diagram.

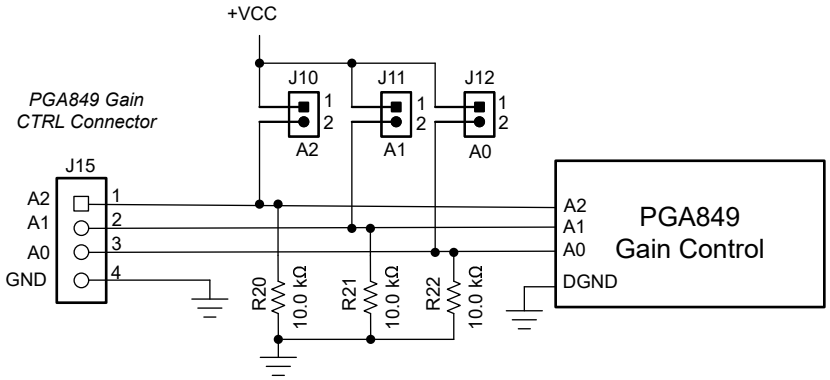



**Figure 2-6. PGA849EVM Gain Control**

## 2.7 Modifications

For flexibility, the EVM provides optional capacitors C4 and C14. These capacitors are in parallel with the PGA849 output-stage difference amplifier internal resistors to implement noise filtering. In addition, the evaluation board provides footprints R6, R11, C9, C5, and C11 for optional input low-pass filters, and footprints for load resistor R7. These additional component footprints in the layout allow the user to customize the evaluation circuit. For a full schematic of the PGA849EVM, see Figure 3-1.

## 2.8 Best Practices

### 2.8.1 Electrostatic Discharge Caution

**CAUTION**

Many of the components on the PGA849EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

### 2.8.2 Hot Surface Warning

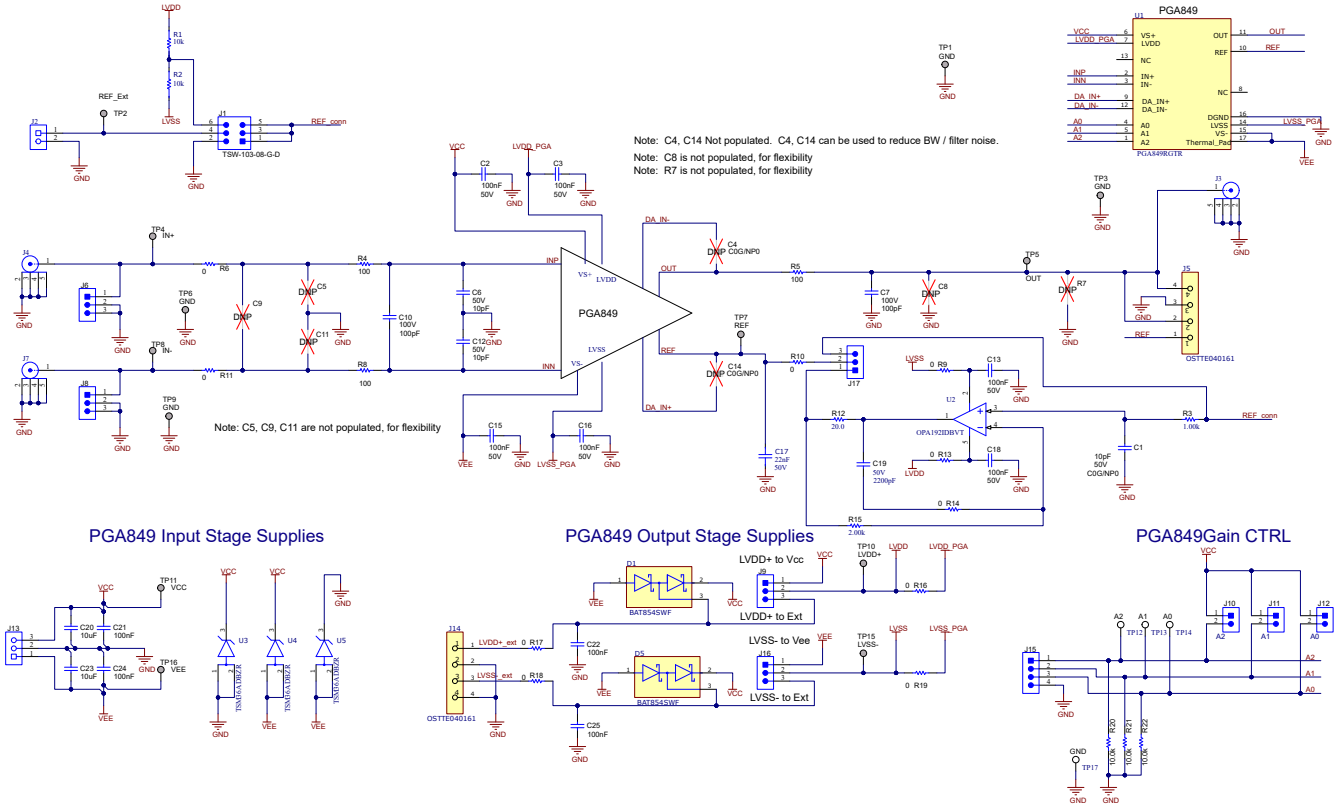
**WARNING**

Device can become hot under high-current conditions. Take care when handling the EVM.

# 3 Hardware Design Files

## 3.1 Schematic

Figure 3-1 illustrates the EVM schematic.




Note: DNP components are not populated.

**Figure 3-1. PGA849EVM Schematic**

## 3.2 PCB Layout

The PGA849EVM is a four-layer PCB design. Figure 3-2 to Figure 3-6 show the PCB layer illustrations. The top layer consists of all signal path traces, and is poured with a solid ground plane. A symmetrical board layout is used at the differential inputs to keep good performance matching and improve common-mode noise rejection. Route traces as symmetrically as possible for both positive and negative pathways. The optional differential input low-pass filter capacitor is placed in very close proximity to the PGA inputs to reduce extrinsic noise. Capacitor C17 is placed in close proximity to REF pin to avoid injecting noise. Decoupling capacitors C2, C15, C3 and C16 are positioned on the top layer as close as possible to the power-supply pins of the device. The second internal layer is a dedicated solid GND plane. The voltage source applied to the reference pin must have a low output impedance. Any resistance at the REF pin is in series with an internal 5kΩ resistor that creates an imbalance in the four resistors of the internal difference amplifier. Optional OPA192 buffer (U2) is placed in close proximity to the REF pin to minimize series resistance in the REF pin. Independent vias are placed at the ground connection of every component to provide a low-impedance path to ground. The third internal layer and bottom layer route the input stage power supplies and the output-stage supply connections.

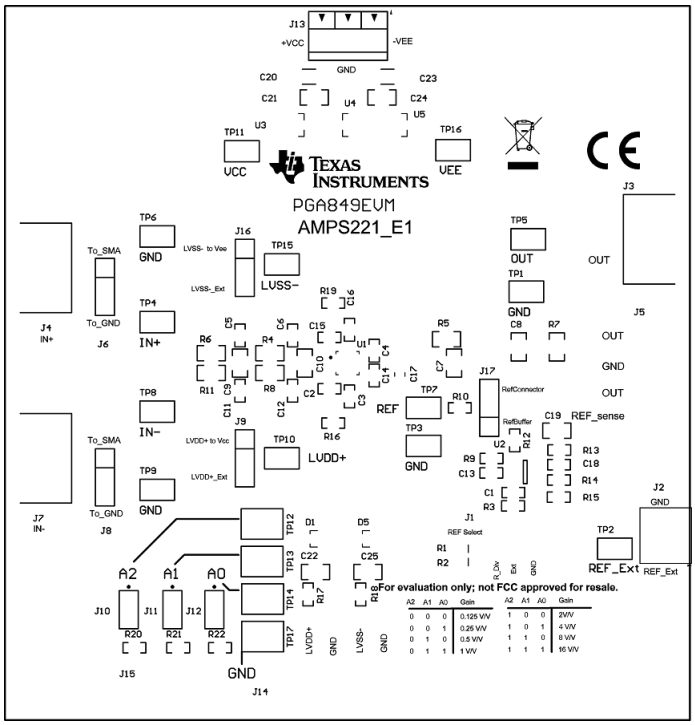



**Figure 3-2. Top Overlay PCB Layout**

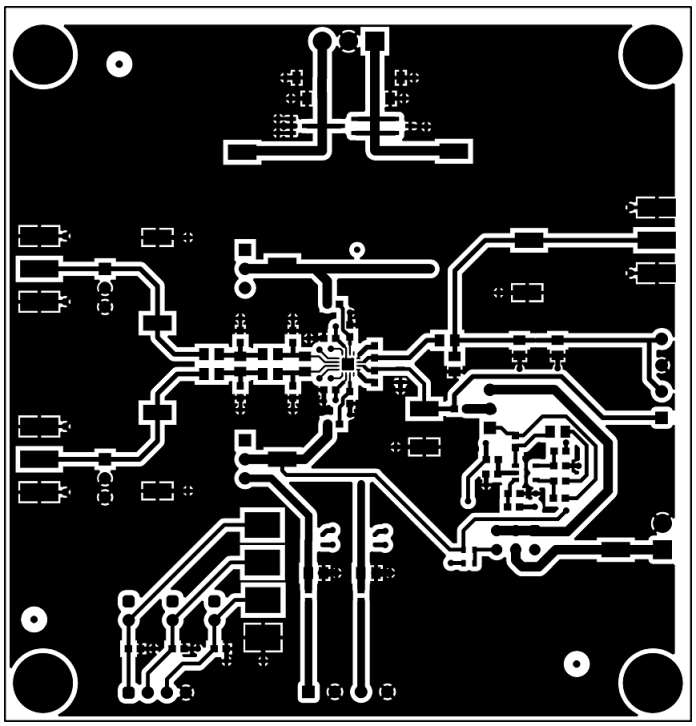


**Figure 3-3. Top Layer PCB Layout**

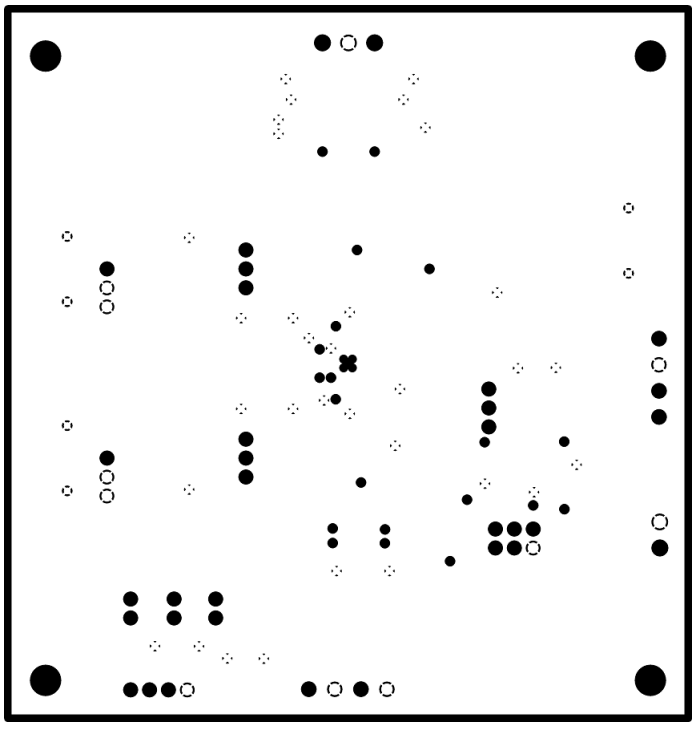


**Figure 3-4. Ground Layer PCB Layout**

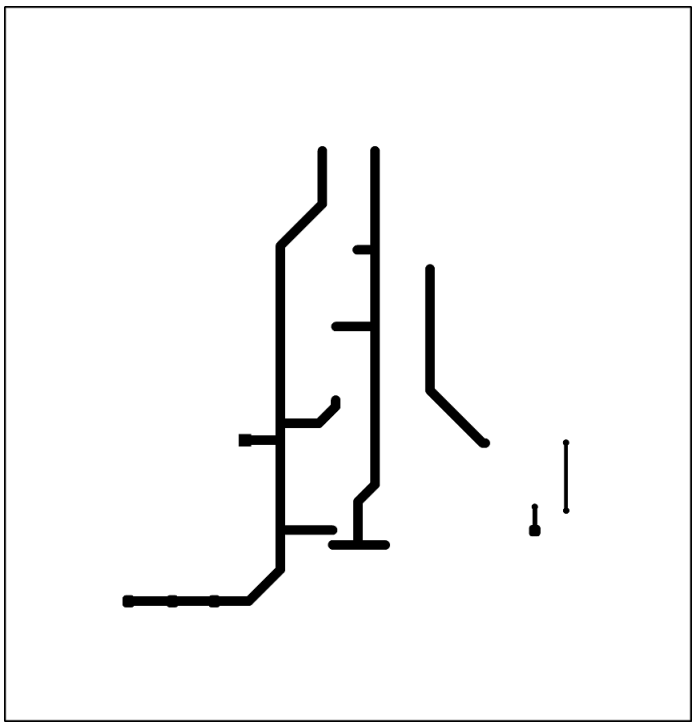


**Figure 3-5. Power Layer PCB Layout**

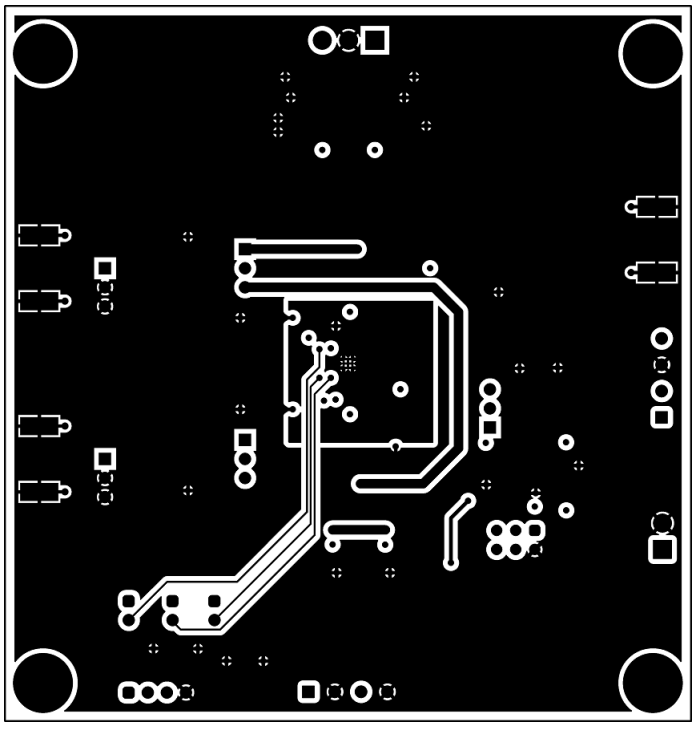


**Figure 3-6. Bottom Layer PCB Layout**

## 3.3 Bill of Materials

Table 3-1 lists the PGA849EVM bill of materials (BOM).

**Table 3-1. PGA849EVM Bill of Materials**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| !PCB1 | 1 | | Printed Circuit Board | | AMPS221 | Any |
| C1, C6, C12 | 3 | 10pF | CAP, CERM, 10pF, 50V, +/- 1%, C0G/NP0, 0603 | 0603 | C0603C100F5GAC7867 | Kemet |
| C2, C3, C13, C15, C16, C18 | 6 | 0.1uF | CAP, CERM, 0.1uF, 50V, +/- 5%, X7R, 0603 | 0603 | C0603C104J5RACTU | Kemet |
| C7, C10 | 2 | 100pF | CAP, CERM, 100pF, 100V, +/- 5%, C0G/NP0, 0805 | 0805 | C0805C101J1GACTU | Kemet |
| C17 | 1 | 22nF | Cap Ceramic 22nF 50V C0G ±5% SMD 0805 +125°C Emboss T/R | 0805 | GRT21B5C1H223JA02L | Murata |
| C19 | 1 | 2200pF | CAP, CERM, 2200pF, 50V, +/- 5%, C0G/NP0, 0805 | 0805 | 08055A222JAT2A | AVX |
| C20, C23 | 2 | 10uF | CAP, CERM, 10uF, 35V, +/- 10%, X7R, 1206 | 1206 | C3216X7R1V106K160AC | TDK |
| C21, C22, C24, C25 | 4 | 0.1uF | CAP, CERM, 0.1uF, 50V, +/- 10%, X7R, 0805 | 0805 | 08055C104KAT2A | AVX |
| D1, D5 | 2 | | Diode Array 1 Pair Series Connection Schottky 40V 200mA (DC) Surface Mount SC-70, SOT-323 | SOT-323 | BAT854SWF | Nexperia |
| H1, H2, H3, H4 | 4 | | Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead | Screw | NY PMS 440 0025 PH | B&F Fastener Supply |
| H5, H6, H7, H8 | 4 | | Standoff, Hex, 0.5"L #4-40 Nylon | Standoff | 1902C | Keystone |
| J1 | 1 | | Header, 2.54mm, 3x2, Gold, TH | Header, 2.54mm, 3x2, TH | TSW-103-08-G-D | Samtec |
| J2 | 1 | | Terminal Block, 3.5mm Pitch, 2x1, TH | 7.0x8.2x6.5mm | ED555/2DS | On-Shore Technology |
| J3, J4, J7 | 3 | | Connector, End launch SMA, 50 ohm, SMT | End Launch SMA | 142-0701-801 | Cinch Connectivity |
| J5, J14 | 2 | | TERM BLOCK 3.5MM VERT 4POS PCB | HDR4 | OSTTE040161 | On Shore Technology |
| J6, J8, J9, J16, J17 | 5 | | Header, 100mil, 3x1, Gold, TH | PBC03SAAN | PBC03SAAN | Sullins Connector Solutions |
| J10, J11, J12 | 3 | | Header, 100mil, 2x1, Gold, TH | 2x1 Header | TSW-102-07-G-S | Samtec |
| J13 | 1 | | Terminal Block, 3.5mm Pitch, 3x1, TH | 10.5x8.2x6.5mm | ED555/3DS | On-Shore Technology |
| J15 | 1 | | Header, 100mil, 4x1, Gold, TH | 10.5x8.2x6.5mm | TSW-104-07-G-S | Samtec |
| R1, R2 | 2 | 10k | Res Thin Film 0603 10K Ohm 0.1% 1/10W ±10ppm/°C Molded SMD Punched Carrier T/R | 0603 | ERA-3ARB103V | Panasonic |
| R3 | 1 | 1.00k | RES, 1.00 k, 0.1%, 0.1 W, 0603 | 0603 | RT0603BRD071KL | Yageo America |
| R4, R5, R8 | 3 | 100 | RES, 100, 0.1%, 0.125 W, 0805 | 0805 | RT0805BRD07100RL | Yageo America |
| R6, R11 | 2 | 0 | RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805 | 0805 | ERJ-6GEY0R00V | Panasonic |

**Table 3-1. PGA849EVM Bill of Materials (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| R9, R10, R13, R14, R16, R17, R18, R19 | 8 | 0 | RES, 0, 5%, 0.1 W, 0603 | 0603 | RC0603JR-070RL | Yageo |
| R12 | 1 | 20 | RES, 20.0, 0.1%, 0.1 W, 0603 | 0603 | RT0603BRD0720RL | Yageo America |
| R15 | 1 | 2.00k | RES, 2.00 k, 0.1%, 0.1 W, 0603 | 0603 | RT0603BRD072KL | Yageo America |
| R20, R21, R22 | 3 | 10.0k | RES, 10.0 k, 1%, 0.1 W, 0603 | 0603 | RCG060310K0FKEA | Vishay Draloric |
| SH-J0, SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8 | 9 | 1x2 | Shunt, 100mil, Flash Gold, Black | Closed Top 100mil Shunt | SPC02SYAN | Sullins Connector Solutions |
| TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP15, TP16 | 13 | | Test Point, Miniature, SMT | Test Point, Miniature, SMT | 5019 | Keystone |
| U1 | 1 | | Low-Noise, Wide-Bandwidth, Precision Programmable Gain Instrumentation Amplifier | VQFN16 | PGA849RGTR | Texas Instruments |
| U2 | 1 | | Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with E-trim, 4.5V to 36V, -40℃ to 125℃, 8-Pin SOT-23 (DBV), Green (RoHS & no Sb/Br), Tape and Reel | DBV0005A | OPA192IDBVT | Texas Instruments |
| U3, U4, U5 | 3 | | Surge Protection Device in SOT-23 Package | SOT23-3 | TSM36ADBZR | Texas Instruments |

# 4 Additional Information

## 4.1 Trademarks

All trademarks are the property of their respective owners.

# 5 Related Documentation

The following document provides information regarding Texas Instruments integrated circuits used in the assembly of the PGA849EVM. This user's guide is available from the TI website under literature number SBOU315. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions are available from the TI website at https://www.ti.com/, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

**Table 5-1. Related Documentation**

| Device | Literature Number |
|---|---|
| PGA849 | SBOSAG3 |

## STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

**WARNING**

**Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.**

**User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.**

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

**CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

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8. *Limitations on Damages and Liability:*

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

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