Application Report
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Recommendation for Register-Related SPD Settings on DDR3 RDIMM

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ABSTRACT

DDR3 memory modules can be populated with EEPROMs that use the Serial Presence Detect memory technology. The SPD EEPROM contains information for the memory controller about the memory module. On Registered DIMM (RDIMM), the SPD bytes 65-76 are reserved for register specific content.

This application report gives DIMM manufacturers who are using TI registers on their modules, a recommendation for the correct SPD settings of bytes 65-76. Only the JEDEC standard board layouts (Raw Cards or R/C) are covered by this report, namely R/C A-H, J-N, and V.

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1 Description of SPD Bytes 65–76

The DDR3 register is a complex buffer that which allows various kinds of configuration. The memory controller performs the configuration by writing Register Control commands to the register.

As different DIMM designs have different requirements, it is necessary to write the correct settings in the SPD EEPROM on the memory module. The memory controller can read this information at system start and program the register accordingly. Table 1 gives a short description for the register-related bytes in the SPD.

Table 1. Description of SPD Bytes 65-76

SPD Byte	Short Description	Description
65	Vendor ID1	Bytes 65 and 66 are reserved for the register vendor ID. TI's ID is 0x8097
66	Vendor ID2	
67	Revision ID	Information about the revision of the register. See Table 2 for version overview.
68	Register Type	Reserved
69	RC0+RC1	Global feature and clock driver enable control word
70	RC2+RC3	Timing and CA signal driver characteristics control word
71	RC4+RC5	Control signal driver characteristics control word
72	RC6+RC7	Reserved
73	RC8+RC9	Input bus termination and static system settings control word
74	RC10+RC11	Maximum DIMM speed and voltage range control word
75	RC12+RC13	Reserved
76	RC14+RC15	Reserved

Table 2. TI DDR3 Register Revision ID Overview

Part Number	Top Marking	Architecture	Revision ID (SPD Byte 67)
SN74SSQE32882	TE32882E	V3.1	0x1D
SN74SSQEA32882	EA32882B	V4.2	0x28
SN74SSQEB32882	EB32882A	V5.0	0x33
SN74SSQEC32882	EC32882S	V5.1	0X3D

2 Recommendation for Standard RDIMM

Table 3 shows TI's recommendation for the register-related SPD bytes on DDR3 standard height RDIMM. Different DRAM vendors have different input loads. Therefore, bytes 70 and 71 might be different for individual DIMM/DRAM vendors, as those bytes define the driver strength of the register. It is up to the DIMM vendors to verify this with simulations and measurements on their own DIMM design.

Table 3. Recommended DDR3 RDIMM SPD Programming for Bytes 65–76

SPD Byte	Description	R/C A 1Rx8 Planar	R/C B 2Rx8 Planar	R/C C 1Rx4 Planar	R/C D 2Rx4 Stacked	R/C E 2Rx4 Planar	R/C F 4Rx4 Stacked	R/C G 4Rx8 Stacked	R/C H 4Rx8 Planar	R/C J 2Rx4 Planar	R/C W 4Rx4 Stacked	R/C Y 4Rx8 Planar	R/C AB 4Rx4 Stacked
65	TI Vendor ID	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80
66	TI Vendor ID	0x97	0x97	0x97	0x97	0x97	0x97	0x97	0x97	0x97	0x97	0x97	0x97
67	Rev. ID	See Table 2	See Table 2	See Table 2	See Table 2	See Table 2	See Table 2	See Table 2	See Table 2	See Table 2	See Table 2	See Table 2	See Table 2
68	Register Type	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
69	RC1 + RC0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
70	RC 3 + RC2	**0x00**	**0x50**	**0x50**	**0xA0**	**0x50**	**0x50**	**0x50**	**0x50**	**0x50**	**0x50**	**0x50**	**0x50**
71	RC 5 + RC4	**0x00**	**0x00**	**0x55**	**0xA5**	**0x55**	**0x50**	**0x55**	**0x55**	**0x55**	**0x50**	**0x55**	**0x50**
72	RC7+RC6	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
73	RC9+RC8	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
74	RC11+RC10	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
75	RC13+RC12	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
76	RC15+RC14	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00

3 Recommendation for Very Low Profile (VLP) RDIMM

Table 4 shows TI's recommendation for the register related SPD bytes on DDR3 VLP-RDIMM. Different DRAM vendors have different input loads. Therefore, bytes 70 and 71 might be different for individual DIMM/DRAM vendors, as those bytes define the driver strength of the register. It is up to the DIMM vendors to verify this with simulations and measurements on their own DIMM design.

Table 4. Recommended DDR3 VLP RDIMM SPD Programming for Bytes 65-76

SPD Byte	Description	R/C K	R/C L	R/C M	R/C N	R/C U	R/C V
		1Rx8 planar	2Rx8 planar	1Rx4 planar	2Rx4 stacked	4Rx4 stacked	4Rx8 stacked
65	TI Vendor ID	0x80	0x80	0x80	0x80	0x80	0x80
66	TI Vendor ID	0x97	0x97	0x97	0x97	0x97	0x97
67	Rev. ID	See Table 2	See Table 2	See Table 2	See Table 2	See Table 2	See Table 2
68	Register Type	0x00	0x00	0x00	0x00	0x00	0x00
69	RC1 + RC0	0x00	0x00	0x00	0x00	0x00	0x00
70	RC 3 + RC2	**0x00**	**0x50**	**0x50**	**0xA0**	**0xA0**	**0xA0**
71	RC 5 + RC4	**0x00**	**0x00**	**0x55**	**0x55**	**0x55**	**0xAA**
72	RC7+RC6	0x00	0x00	0x00	0x00	0x00	0x00
73	RC9+RC8	0x00	0x00	0x00	0x00	0x00	0x00
74	RC11+RC10	0x00	0x00	0x00	0x00	0x00	0x00
75	RC13+RC12	0x00	0x00	0x00	0x00	0x00	0x00
76	RC15+RC14	0x00	0x00	0x00	0x00	0x00	0x00

4 References

1. *SN74SSQEC32882, 28-Bit to 56-Bit Registered Buffer with Address Parity Test One Pair to Four Pair Differential Clock PLL Driver* data sheet SCAS920
2. *JEDEC Solid State Technology Association, Registered DIMM Design Specification (JESD21)*

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