# TMUX6236 36V, Low-RON, 2:1 (SPDT), 2-Channel Precision Switch With 1.8V Logic

## 1 Features

- Dual supply range: ±4.5V to ±18V
- Single supply range: 4.5V to 36V
- Low on-resistance: 2Ω
- High current support: 330mA (maximum) (WQFN)
- –40°C to +125°C operating temperature
- 1.8V logic compatible
- Integrated pull-down resistor on logic pins
- Fail-safe logic
- Rail-to-rail operation
- Bidirectional operation

## 2 Applications

- Factory automation and industrial controls
- Programmable logic controllers (PLC)
- Analog input modules
- ATE test equipment
- Battery monitoring systems
- Ultrasound scanners
- Patient monitoring and diagnostics
- Optical networking
- Optical test equipment
- Remote radio units
- Wired networking
- Data acquisition systems

## 3 Description

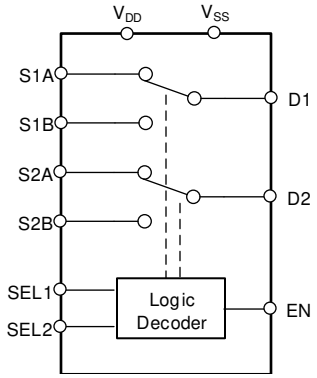
The TMUX6236 is a complementary metal-oxide semiconductor (CMOS) switch with two 2:1 switches. The device works well with dual supplies (±4.5V to ±18V), a single supply (4.5V to 36V), or asymmetric supplies (such as $V_{DD}$ = 12V, $V_{SS}$ = –5V). The TMUX6236 supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from $V_{SS}$ to $V_{DD}$.

All logic control inputs support logic levels from 1.8V to $V_{DD}$, allowing for both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TMUX6236 | RUM (WQFN, 16) | 4mm × 4mm |
| | PW (TSSOP, 16) | 5mm × 6.4mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Block Diagram**

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# 4 Pin Configuration and Functions

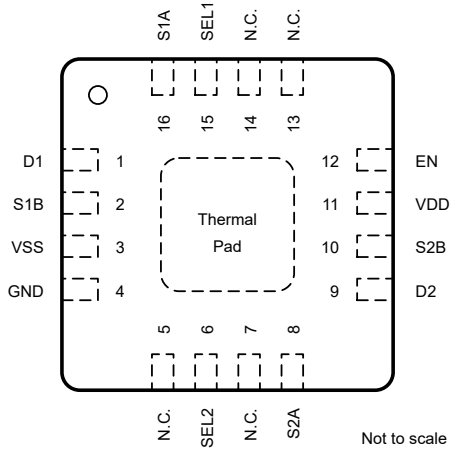



**Figure 4-1. RUM Package, 16-Pin WQFN (Top View)**

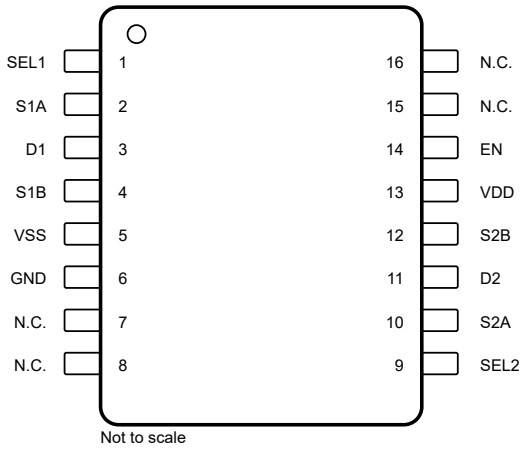



**Figure 4-2. PW Package, 16-Pin TSSOP (Top View)**

**Table 4-1. Pin Functions**

| PIN | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | TSSOP | WQFN | | |
| D1 | 3 | 1 | I/O | Drain pin. Can be an input or output. |
| D2 | 11 | 9 | I/O | Drain pin. Can be an input or output. |
| EN | 14 | 12 | I | Active high logic enable, has internal pull-up resistor. When this pin is low, all switches are turned off. When this pin is high, the SEL logic input determine which switch is turned on. |
| GND | 6 | 4 | P | Ground (0V) reference |
| NC | 7, 8, 15, 16 | 5, 7, 13, 14 | — | No internal connection. Can be shorted to GND or left floating. |
| S1A | 2 | 16 | I/O | Source pin 1A. Can be an input or output. |
| S1B | 4 | 2 | I/O | Source pin 1B. Can be an input or output. |
| S2A | 10 | 8 | I/O | Source pin 2A. Can be an input or output. |
| S2B | 12 | 10 | I/O | Source pin 2B. Can be an input or output. |
| SEL1 | 1 | 15 | I | Logic control input, has internal pull-down resistor. Table 7-1 lists how to control the switch connection. |
| SEL2 | 9 | 6 | I | Logic control input, has internal pull-down resistor. Table 7-1 lists how to control the switch connection. |
| $V_{DD}$ | 13 | 11 | P | Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between $V_{DD}$ and GND. |
| $V_{SS}$ | 5 | 3 | P | Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between $V_{SS}$ and GND. |
| Thermal Pad | | | — | The thermal pad is not connected internally. There is no requirement to electrically connect this pad. If connected, however, it is recommended that the pad be left floating or tied to GND. |

(1) I = input, O = output, P = power

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD} – V_{SS}$ | Supply voltage | | 38 | V |
| $V_{DD}$ | | –0.5 | 38 | V |
| $V_{SS}$ | | –38 | 0.5 | V |
| $V_{SEL}$ or $V_{EN}$ | Logic control input pin voltage (SELx) | –0.5 | 38 | V |
| $I_{SEL}$ or $I_{EN}$ | Logic control input pin current (SELx) | –30 | 30 | mA |
| $V_S$ or $V_D$ | Source or drain voltage (Sx, Dx) | $V_{SS}$–0.5 | $V_{DD}$+0.5 | V |
| $I_{IK}$ | Diode clamp current(3) | –30 | 30 | mA |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx, Dx) | | $I_{DC}$ + 10 %(4) | mA |
| $T_A$ | Ambient temperature | –55 | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |
| $T_J$ | Junction temperature | | 150 | °C |
| $P_{tot}$ | Total power dissipation (TSSOP)(5) | | 720 | mW |
| $P_{tot}$ | Total power dissipation (QFN)(6) | | 1650 | mW |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for $I_{DC}$ specifications.
(5) For QFN package: $P_{tot}$ derates linearly above $T_A$ = 70°C by 10.3mW/°C.
(6) For QFN package: $P_{tot}$ derates linearly above $T_A$ = 70°C by 24.2mW/°C.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±1000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Thermal Information

| THERMAL METRIC(1) | | TMUX6236 | | UNIT |
|---|---|---|---|---|
| | | RUM (WQFN) | PW (TSSOP) | |
| | | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 41.5 | 97.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 25.1 | 25.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 16.5 | 44.1 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | 1.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 16.4 | 43.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.9 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ – $V_{SS}$ (1) | Power supply voltage differential | 4.5 | | 36 | V |
| $V_{DD}$ | Positive power supply voltage | 4.5 | | 36 | V |
| $V_S$ or $V_D$ | Signal path input/output voltage (source or drain pin) (Sx, D) | $V_{SS}$ | | $V_{DD}$ | V |
| $V_{SEL}$ or $V_{EN}$ | Address or enable pin voltage | 0 | | 36 | V |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx, D) | | | $I_{DC}$ (2) | mA |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |

(1) $V_{DD}$ and $V_{SS}$ can be any value as long as 4.5V ≤ ($V_{DD}$ – $V_{SS}$) ≤ 36V, and the minimum $V_{DD}$ is met.
(2) Refer to *Source or Drain Continuous Current* table for $I_{DC}$ specifications.

## 5.5 Source or Drain Continuous Current

at supply voltage of $V_{DD}$ ± 10%, $V_{SS}$ ± 10 % (unless otherwise noted)

| CONTINUOUS CURRENT PER CHANNEL ($I_{DC}$) (2) | | $T_A$ = 25°C | $T_A$ = 85°C | $T_A$ = 125°C | UNIT |
|---|---|---|---|---|---|
| PACKAGE | TEST CONDITIONS | | | | |
| PW (TSSOP) | +36V Single Supply(1) | 455 | 300 | 165 | mA |
| | ±15V Dual Supply | 455 | 300 | 165 | mA |
| | +12V Single Supply | 355 | 240 | 145 | mA |
| | ±5V Dual Supply | 335 | 225 | 140 | mA |
| | +5V Single Supply | 240 | 170 | 110 | mA |
| RUM (WQFN) | +36V Single Supply(1) | 650 | 400 | 190 | mA |
| | ±15V Dual Supply | 640 | 380 | 180 | mA |
| | +12V Single Supply | 500 | 310 | 170 | mA |
| | ±5V Dual Supply | 460 | 275 | 160 | mA |
| | +5V Single Supply | 330 | 210 | 120 | mA |

(1) Specified for nominal supply voltage only.
(2) Refer to Total power dissipation ($P_{tot}$) limits in *Absolute Maximum Ratings* table that must be followed with max continuous current specification.

## 5.6 ±15V Dual Supply: Electrical Characteristics

$V_{DD}$ = +15V ± 10%, $V_{SS}$ = –15V ±10%, GND = 0V (unless otherwise noted)
Typical at $V_{DD}$ = +15V, $V_{SS}$ = –15V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = –10V to +10V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 2 | 2.7 | Ω |
| | | | –40°C to +85°C | | | 3.4 | Ω |
| | | | –40°C to +125°C | | | 4 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = –10V to +10V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 0.1 | 0.18 | Ω |
| | | | –40°C to +85°C | | | 0.19 | Ω |
| | | | –40°C to +125°C | | | 0.21 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = –10V to +10V<br>$I_S$ = –10mA<br>Refer to On-Resistance | 25°C | | 0.2 | 0.46 | Ω |
| | | | –40°C to +85°C | | | 0.65 | Ω |
| | | | –40°C to +125°C | | | 0.7 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 0V, $I_S$ = –10mA<br>Refer to On-Resistance | –40°C to +125°C | | 0.008 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 16.5V, $V_{SS}$ = –16.5V<br>Switch state is off<br>$V_S$ = +10V / –10V<br>$V_D$ = –10V / + 10V<br>Refer to Off-Leakage Current | 25°C | –0.35 | 0.05 | 0.35 | nA |
| | | | –40°C to +85°C | –3 | | 3 | nA |
| | | | –40°C to +125°C | –20 | | 20 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 16.5V, $V_{SS}$ = –16.5V<br>Switch state is off<br>$V_S$ = +10V / –10V<br>$V_D$ = –10V / + 10V<br>Refer to Off-Leakage Current | 25°C | –0.6 | 0.1 | 0.6 | nA |
| | | | –40°C to +85°C | –7 | | 7 | nA |
| | | | –40°C to +125°C | –45 | | 45 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 16.5V, $V_{SS}$ = –16.5V<br>Switch state is on<br>$V_S$ = $V_D$ = ±10V<br>Refer to On-Leakage Current | 25°C | –0.5 | 0.05 | 0.5 | nA |
| | | | –40°C to +85°C | –3.5 | | 3.5 | nA |
| | | | –40°C to +125°C | –25 | | 25 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | –40°C to +125°C | 1.3 | | 36 | V |
| $V_{IL}$ | Logic voltage low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | –40°C to +125°C | | 0.4 | 2 | µA |
| $I_{IL}$ | Input leakage current | | –40°C to +125°C | –1.5 | –0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | 3.5 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 16.5V, $V_{SS}$ = –16.5V<br>Logic inputs = 0V, 5V, or $V_{DD}$ | 25°C | | 45 | 60 | µA |
| | | | –40°C to +85°C | | | 70 | µA |
| | | | –40°C to +125°C | | | 85 | µA |
| $I_{SS}$ | $V_{SS}$ supply current | $V_{DD}$ = 16.5V, $V_{SS}$ = –16.5V<br>Logic inputs = 0V, 5V, or $V_{DD}$ | 25°C | | 7 | 24 | µA |
| | | | –40°C to +85°C | | | 30 | µA |
| | | | –40°C to +125°C | | | 38 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

## 5.7 ±15V Dual Supply: Switching Characteristics

$V_{DD}$ = +15V ± 10%, $V_{SS}$ = –15V ± 10%, GND = 0V (unless otherwise noted)
Typical at $V_{DD}$ = +15V, $V_{SS}$ = –15V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 10V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Transition Time | 25°C | | 110 | 130 | ns |
| | | | –40°C to +85°C | | | 160 | ns |
| | | | –40°C to +125°C | | | 180 | ns |
| $t_{ON}$ | Turn-on time from control input | $V_S$ = 10V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 95 | 120 | ns |
| | | | –40°C to +85°C | | | 135 | ns |
| | | | –40°C to +125°C | | | 145 | ns |
| $t_{OFF}$ | Turn-off time from control input | $V_S$ = 10V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 125 | 160 | ns |
| | | | –40°C to +85°C | | | 175 | ns |
| | | | –40°C to +125°C | | | 190 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 10V,<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Break-before-make Time | 25°C | | 27 | | ns |
| | | | –40°C to +85°C | 5 | | | ns |
| | | | –40°C to +125°C | 5 | | | ns |
| $t_{ON (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 1µs<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on (VDD) Time | 25°C | | 0.17 | | ms |
| | | | –40°C to +85°C | | 0.18 | | ms |
| | | | –40°C to +125°C | | 0.18 | | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50Ω , $C_L$ = 5pF<br>Refer to Propagation Delay | 25°C | | 720 | | ps |
| $Q_{INJ}$ | Charge injection | $V_S$ = 0V, $C_L$ = 100pF<br>Refer to Charge Injection | 25°C | | 30 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V, f = 100kHz<br>Refer to Off Isolation | 25°C | | –70 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V, f = 1MHz<br>Refer to Off Isolation | 25°C | | –50 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V, f = 100kHz<br>Refer to Crosstalk | 25°C | | –107 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V, f = 1MHz<br>Refer to Crosstalk | 25°C | | –93 | | dB |
| BW | –3dB Bandwidth | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V<br>Refer to Bandwidth | 25°C | | 40 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V, f = 1MHz | 25°C | | –0.15 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 50Ω , $C_L$ = 5pF,<br>f = 1MHz<br>Refer to ACPSRR | 25°C | | –68 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 15V, $V_{BIAS}$ = 0V<br>$R_L$ = 10kΩ , $C_L$ = 5pF,<br>f = 20Hz to 20kHz<br>Refer to THD + Noise | 25°C | | 0.0006 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 0V, f = 1MHz | 25°C | | 45 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 0V, f = 1MHz | 25°C | | 55 | | pF |
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 0V, f = 1MHz | 25°C | | 165 | | pF |

## 5.8 36V Single Supply: Electrical Characteristics

$V_{DD}$ = +36V ± 10%, $V_{SS}$ = 0V, GND = 0V (unless otherwise noted)
Typical at $V_{DD}$ = +36V, $V_{SS}$ = 0V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0V to 30V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 2.1 | 3.1 | Ω |
| | | | –40°C to +85°C | | | 3.5 | Ω |
| | | | –40°C to +125°C | | | 4.4 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = 0V to 30V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 0.1 | 0.18 | Ω |
| | | | –40°C to +85°C | | | 0.19 | Ω |
| | | | –40°C to +125°C | | | 0.21 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0V to 30V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 0.7 | 1.25 | Ω |
| | | | –40°C to +85°C | | | 1.3 | Ω |
| | | | –40°C to +125°C | | | 1.35 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 18V, $I_S$ = –10mA<br>Refer to On-Resistance | –40°C to +125°C | | 0.008 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 39.6V, $V_{SS}$ = 0V<br>Switch state is off<br>$V_S$ = 30V / 1V<br>$V_D$ = 1V / 30V<br>Refer to Off-Leakage Current | 25°C | –0.25 | 0.05 | 0.25 | nA |
| | | | –40°C to +85°C | –5 | | 5 | nA |
| | | | –40°C to +125°C | –39 | | 39 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 39.6V, $V_{SS}$ = 0V<br>Switch state is off<br>$V_S$ = 30V / 1V<br>$V_D$ = 1V / 30V<br>Refer to Off-Leakage Current | 25°C | –0.6 | 0.12 | 0.6 | nA |
| | | | –40°C to +85°C | –12 | | 12 | nA |
| | | | –40°C to +125°C | –80 | | 80 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 39.6V, $V_{SS}$ = 0V<br>Switch state is on<br>$V_S$ = $V_D$ = 30V or 1V<br>Refer to On-Leakage Current | 25°C | –0.25 | 0.05 | 0.25 | nA |
| | | | –40°C to +85°C | –5 | | 5 | nA |
| | | | –40°C to +125°C | –39 | | 39 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | –40°C to +125°C | 1.3 | | 44 | V |
| $V_{IL}$ | Logic voltage low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | –40°C to +125°C | | 1 | 2.75 | µA |
| $I_{IL}$ | Input leakage current | | –40°C to +125°C | –1.25 | –0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | 3.5 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 39.6V, $V_{SS}$ = 0V<br>Logic inputs = 0V, 5V, or $V_{DD}$ | 25°C | | 50 | 75 | µA |
| | | | –40°C to +85°C | | | 85 | µA |
| | | | –40°C to +125°C | | | 100 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

## 5.9 36V Single Supply: Switching Characteristics

$V_{DD}$ = +36V ± 10%, $V_{SS}$ = 0V, GND = 0V (unless otherwise noted)
Typical at $V_{DD}$ = +36V, $V_{SS}$ = 0V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 18V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Transition Time | 25°C | | 85 | 135 | ns |
| | | | –40°C to +85°C | | | 150 | ns |
| | | | –40°C to +125°C | | | 170 | ns |
| $t_{ON}$ | Turn-on time from control input | $V_S$ = 18V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 90 | 130 | ns |
| | | | –40°C to +85°C | | | 150 | ns |
| | | | –40°C to +125°C | | | 170 | ns |
| $t_{OFF}$ | Turn-off time from control input | $V_S$ = 18V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 120 | 165 | ns |
| | | | –40°C to +85°C | | | 180 | ns |
| | | | –40°C to +125°C | | | 195 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 18V,<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Break-before-make Time | 25°C | | 30 | | ns |
| | | | –40°C to +85°C | 8 | | | ns |
| | | | –40°C to +125°C | 8 | | | ns |
| $t_{ON (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 1µs<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on (VDD) Time | 25°C | | 0.16 | | ms |
| | | | –40°C to +85°C | | 0.17 | | ms |
| | | | –40°C to +125°C | | 0.17 | | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50Ω , $C_L$ = 5pF<br>Refer to Propagation Delay | 25°C | | 900 | | ps |
| $Q_{INJ}$ | Charge injection | $V_S$ = 18V, $C_L$ = 100pF<br>Refer to Charge Injection | 25°C | | 78 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V, f = 100kHz<br>Refer to Off Isolation | 25°C | | –70 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V, f = 1MHz<br>Refer to Off Isolation | 25°C | | –50 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V, f = 100kHz<br>Refer to Crosstalk | 25°C | | –112 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V, f = 1MHz<br>Refer to Crosstalk | 25°C | | –93 | | dB |
| BW | –3dB Bandwidth | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V<br>Refer to Bandwidth | 25°C | | 35 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V, f = 1MHz | 25°C | | –0.16 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 50Ω , $C_L$ = 5pF,<br>f = 1MHz<br>Refer to ACPSRR | 25°C | | –65 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 18V, $V_{BIAS}$ = 6V<br>$R_L$ = 10kΩ , $C_L$ = 5pF,<br>f = 20Hz to 20kHz<br>Refer to THD + Noise | 25°C | | 0.0006 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 6V, f = 1MHz | 25°C | | 45 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 6V, f = 1MHz | 25°C | | 60 | | pF |
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 6V, f = 1MHz | 25°C | | 165 | | pF |

## 5.10 12V Single Supply: Electrical Characteristics

$V_{DD}$ = +12V ± 10%, $V_{SS}$ = 0V, GND = 0V (unless otherwise noted)
Typical at $V_{DD}$ = +12V, $V_{SS}$ = 0V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0V to 10V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 2.8 | 5.4 | Ω |
| | | | –40°C to +85°C | | | 6.8 | Ω |
| | | | –40°C to +125°C | | | 7.4 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = 0V to 10V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 0.13 | 0.21 | Ω |
| | | | –40°C to +85°C | | | 0.23 | Ω |
| | | | –40°C to +125°C | | | 0.25 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0V to 10V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 0.8 | 1.7 | Ω |
| | | | –40°C to +85°C | | | 1.9 | Ω |
| | | | –40°C to +125°C | | | 2 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 0V, $I_S$ = –10mA<br>Refer to On-Resistance | –40°C to +125°C | | 0.015 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 13.2V, $V_{SS}$ = 0V<br>Switch state is off<br>$V_S$ = 10V / 1V<br>$V_D$ = 1V / 10V<br>Refer to Off-Leakage Current | 25°C | –0.25 | 0.01 | 0.25 | nA |
| | | | –40°C to +85°C | –2 | | 2 | nA |
| | | | –40°C to +125°C | –16 | | 16 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 13.2V, $V_{SS}$ = 0V<br>Switch state is off<br>$V_S$ = 10V / 1V<br>$V_D$ = 1V / 10V<br>Refer to Off-Leakage Current | 25°C | –0.6 | 0.12 | 0.6 | nA |
| | | | –40°C to +85°C | –5 | | 5 | nA |
| | | | –40°C to +125°C | –34 | | 34 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 13.2V, $V_{SS}$ = 0V<br>Switch state is on<br>$V_S$ = $V_D$ = 10V or 1V<br>Refer to On-Leakage Current | 25°C | –0.35 | 0.01 | 0.35 | nA |
| | | | –40°C to +85°C | –2 | | 2 | nA |
| | | | –40°C to +125°C | –16 | | 16 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | –40°C to +125°C | 1.3 | | 44 | V |
| $V_{IL}$ | Logic voltage low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | –40°C to +125°C | | 0.4 | 2.25 | µA |
| $I_{IL}$ | Input leakage current | | –40°C to +125°C | –1.25 | –0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | 3.5 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 13.2V, $V_{SS}$ = 0V<br>Logic inputs = 0V, 5V, or $V_{DD}$ | 25°C | | 30 | 44 | µA |
| | | | –40°C to +85°C | | | 52 | µA |
| | | | –40°C to +125°C | | | 62 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

## 5.11 12V Single Supply: Switching Characteristics

$V_{DD}$ = +12V ± 10%, $V_{SS}$ = 0V, GND = 0V (unless otherwise noted)
Typical at $V_{DD}$ = +12V, $V_{SS}$ = 0V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 8V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Transition Time | 25°C | | 100 | 180 | ns |
| | | | –40°C to +85°C | | | 220 | ns |
| | | | –40°C to +125°C | | | 245 | ns |
| $t_{ON}$ | Turn-on time from control input | $V_S$ = 8V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 190 | 235 | ns |
| | | | –40°C to +85°C | | | 260 | ns |
| | | | –40°C to +125°C | | | 280 | ns |
| $t_{OFF}$ | Turn-off time from control input | $V_S$ = 8V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 160 | 200 | ns |
| | | | –40°C to +85°C | | | 220 | ns |
| | | | –40°C to +125°C | | | 245 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 8V,<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Break-before-make Time | 25°C | | 30 | | ns |
| | | | –40°C to +85°C | 9 | | | ns |
| | | | –40°C to +125°C | 9 | | | ns |
| $t_{ON (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 1µs<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on (VDD) Time | 25°C | | 0.17 | | ms |
| | | | –40°C to +85°C | | 0.18 | | ms |
| | | | –40°C to +125°C | | 0.18 | | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50Ω , $C_L$ = 5pF<br>Refer to Propagation Delay | 25°C | | 770 | | ps |
| $Q_{INJ}$ | Charge injection | $V_S$ = 6V, $C_L$ = 100pF<br>Refer to Charge Injection | 25°C | | 12 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V, f = 100kHz<br>Refer to Off Isolation | 25°C | | –70 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V, f = 1MHz<br>Refer to Off Isolation | 25°C | | –50 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V, f = 100kHz<br>Refer to Crosstalk | 25°C | | –112 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V, f = 1MHz<br>Refer to Crosstalk | 25°C | | –93 | | dB |
| BW | –3dB Bandwidth | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V<br>Refer to Bandwidth | 25°C | | 50 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 6V, f = 1MHz | 25°C | | –0.25 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 50Ω , $C_L$ = 5pF,<br>f = 1MHz<br>Refer to ACPSRR | 25°C | | –70 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 6V, $V_{BIAS}$ = 6V<br>$R_L$ = 10kΩ , $C_L$ = 5pF,<br>f = 20Hz to 20kHz<br>Refer to THD + Noise | 25°C | | 0.001 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 6V, f = 1MHz | 25°C | | 52 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 6V, f = 1MHz | 25°C | | 68 | | pF |
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 6V, f = 1MHz | 25°C | | 170 | | pF |

## 5.12 ±5V Dual Supply: Electrical Characteristics

$V_{DD}$ = +5V ± 10%, $V_{SS}$ = –5V ±10%, GND = 0V (unless otherwise noted)
Typical at $V_{DD}$ = +5V, $V_{SS}$ = –5V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = –4.5V to +4.5V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 3.3 | 6.3 | Ω |
| | | | –40°C to +85°C | | | 7.6 | Ω |
| | | | –40°C to +125°C | | | 8.5 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = –4.5V to +4.5V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 0.07 | 0.22 | Ω |
| | | | –40°C to +85°C | | | 0.23 | Ω |
| | | | –40°C to +125°C | | | 0.25 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = –4.5V to +4.5V<br>$I_D$ = –10mA<br>Refer to On-Resistance | 25°C | | 1 | 2 | Ω |
| | | | –40°C to +85°C | | | 2.1 | Ω |
| | | | –40°C to +125°C | | | 2.2 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 0V, $I_S$ = –10mA<br>Refer to On-Resistance | –40°C to +125°C | | 0.015 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = +5.5V, $V_{SS}$ = –5.5V<br>Switch state is off<br>$V_S$ = +4.5V / –4.5V<br>$V_D$ = –4.5V / + 4.5V<br>Refer to Off-Leakage Current | 25°C | –0.4 | 0.05 | 0.4 | nA |
| | | | –40°C to +85°C | –2 | | 2 | nA |
| | | | –40°C to +125°C | –16 | | 16 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = +5.5V, $V_{SS}$ = –5.5V<br>Switch state is off<br>$V_S$ = +4.5V / –4.5V<br>$V_D$ = –4.5V / + 4.5V<br>Refer to Off-Leakage Current | 25°C | –1 | 0.12 | 1 | nA |
| | | | –40°C to +85°C | –5 | | 5 | nA |
| | | | –40°C to +125°C | –35 | | 35 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = +5.5V, $V_{SS}$ = –5.5V<br>Switch state is on<br>$V_S$ = $V_D$ = ±4.5V<br>Refer to On-Leakage Current | 25°C | –0.4 | 0.05 | 0.4 | nA |
| | | | –40°C to +85°C | –2 | | 2 | nA |
| | | | –40°C to +125°C | –16 | | 16 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | –40°C to +125°C | 1.3 | | 44 | V |
| $V_{IL}$ | Logic voltage low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | –40°C to +125°C | | 0.4 | 2 | µA |
| $I_{IL}$ | Input leakage current | | –40°C to +125°C | –1.2 | –0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | 3.5 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = +5.5V, $V_{SS}$ = –5.5V<br>Logic inputs = 0V, 5V, or $V_{DD}$ | 25°C | | 28 | 38 | µA |
| | | | –40°C to +85°C | | | 44 | µA |
| | | | –40°C to +125°C | | | 55 | µA |
| $I_{SS}$ | $V_{SS}$ supply current | $V_{DD}$ = +5.5V, $V_{SS}$ = –5.5V<br>Logic inputs = 0V, 5V, or $V_{DD}$ | 25°C | | 6 | 8.4 | µA |
| | | | –40°C to +85°C | | | 11 | µA |
| | | | –40°C to +125°C | | | 20 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

## 5.13 ±5V Dual Supply: Switching Characteristics

$V_{DD}$ = +5V ± 10%, $V_{SS}$ = –5V ±10%, GND = 0V (unless otherwise noted)
Typical at $V_{DD}$ = +5V, $V_{SS}$ = –5V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 3V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Transition Time | 25°C | | 135 | 210 | ns |
| | | | –40°C to +85°C | | | 250 | ns |
| | | | –40°C to +125°C | | | 285 | ns |
| $t_{ON}$ | Turn-on time from control input | $V_S$ = 3V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 140 | 290 | ns |
| | | | –40°C to +85°C | | | 315 | ns |
| | | | –40°C to +125°C | | | 340 | ns |
| $t_{OFF}$ | Turn-off time from control input | $V_S$ = 3V<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 170 | 250 | ns |
| | | | –40°C to +85°C | | | 270 | ns |
| | | | –40°C to +125°C | | | 295 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 3V,<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Break-before-make Time | 25°C | | 32 | | ns |
| | | | –40°C to +85°C | 7 | | | ns |
| | | | –40°C to +125°C | 7 | | | ns |
| $t_{ON (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 1µs<br>$R_L$ = 300Ω, $C_L$ = 35pF<br>Refer to Turn-on (VDD) Time | 25°C | | 0.17 | | ms |
| | | | –40°C to +85°C | | 0.18 | | ms |
| | | | –40°C to +125°C | | 0.18 | | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50Ω , $C_L$ = 5pF<br>Refer to Propagation Delay | 25°C | | 670 | | ps |
| $Q_{INJ}$ | Charge injection | $V_S$ = 0V, $C_L$ = 100pF<br>Refer to Charge Injection | 25°C | | 9 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V, f = 100kHz<br>Refer to Off Isolation | 25°C | | –70 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V, f = 1MHz<br>Refer to Off Isolation | 25°C | | –50 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V, f = 100kHz<br>Refer to Crosstalk | 25°C | | –117 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V, f = 1MHz<br>Refer to Crosstalk | 25°C | | –94 | | dB |
| BW | –3dB Bandwidth | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V<br>Refer to Bandwidth | 25°C | | 55 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = 0V, f = 1MHz | 25°C | | –0.28 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 50Ω , $C_L$ = 5pF,<br>f = 1MHz<br>Refer to ACPSRR | 25°C | | –70 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 5V, $V_{BIAS}$ = 0V<br>$R_L$ = 10kΩ , $C_L$ = 5pF,<br>f = 20Hz to 20kHz<br>Refer to THD + Noise | 25°C | | 0.001 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 0V, f = 1MHz | 25°C | | 54 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 0V, f = 1MHz | 25°C | | 72 | | pF |
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 0V, f = 1MHz | 25°C | | 170 | | pF |

## 5.14 Typical Characteristics

at $T_A$ = 25°C (unless otherwise noted)

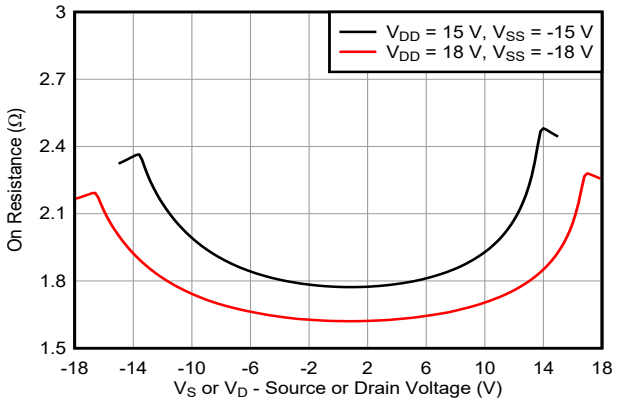



**Figure 5-1. On-Resistance vs Source or Drain Voltage – Dual Supply**

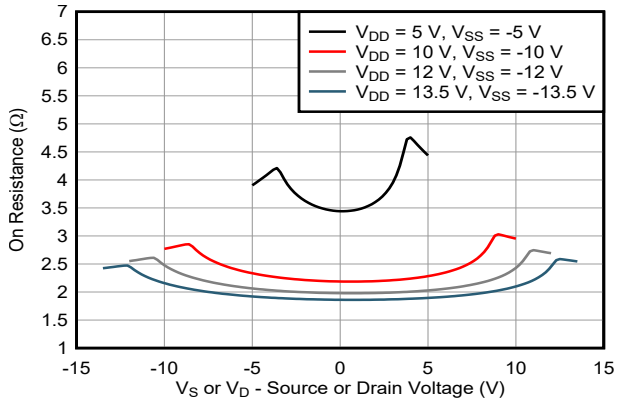



**Figure 5-2. On-Resistance vs Source or Drain Voltage – Dual Supply**

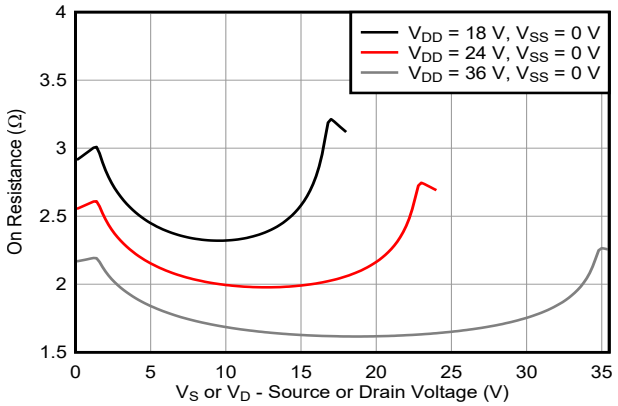



**Figure 5-3. On-Resistance vs Source or Drain Voltage – Single Supply**

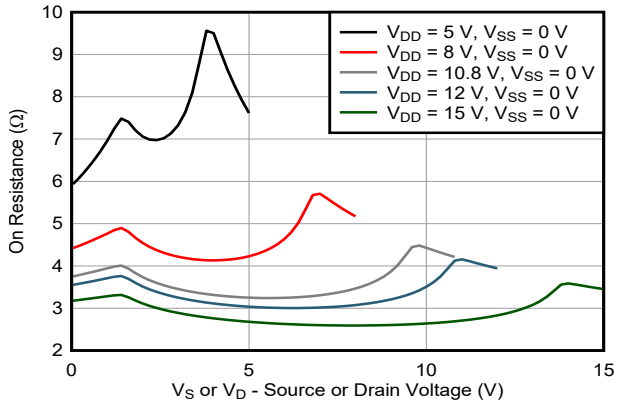



**Figure 5-4. On-Resistance vs Source or Drain Voltage – Single Supply**

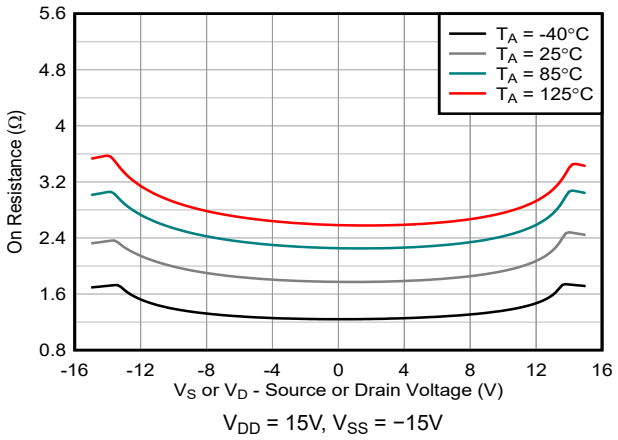



**Figure 5-5. On-Resistance vs Temperature**

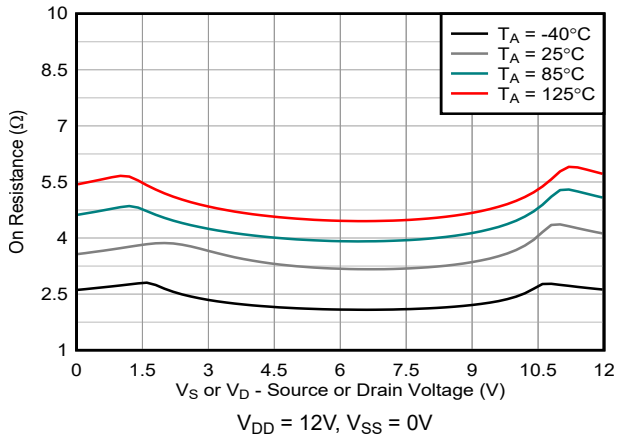
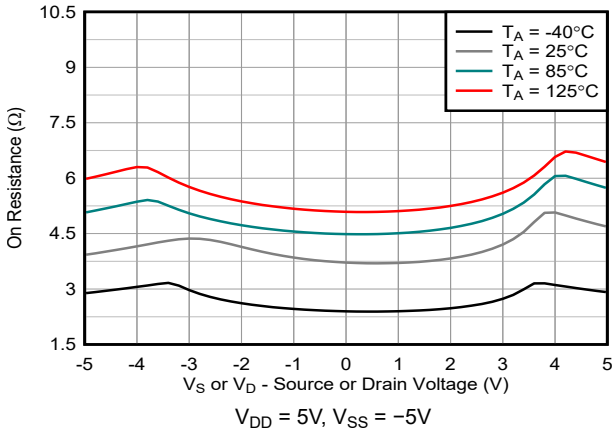



**Figure 5-6. On-Resistance vs Temperature**

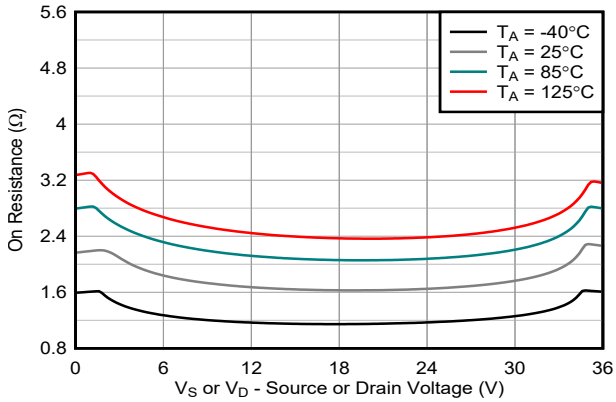
## 5.14 Typical Characteristics (continued)

at $T_A$ = 25°C (unless otherwise noted)



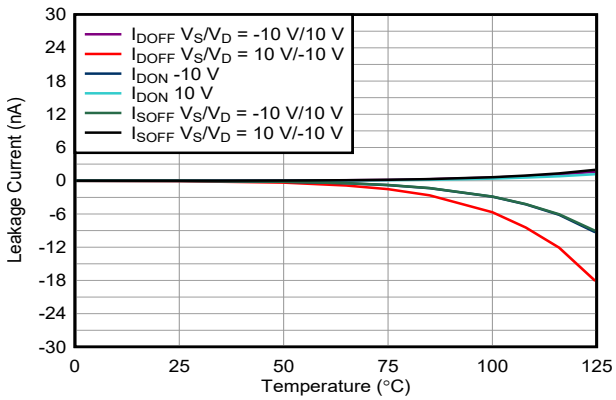

$V_{DD}$ = 5V, $V_{SS}$ = −5V

**Figure 5-7. On-Resistance vs Temperature**



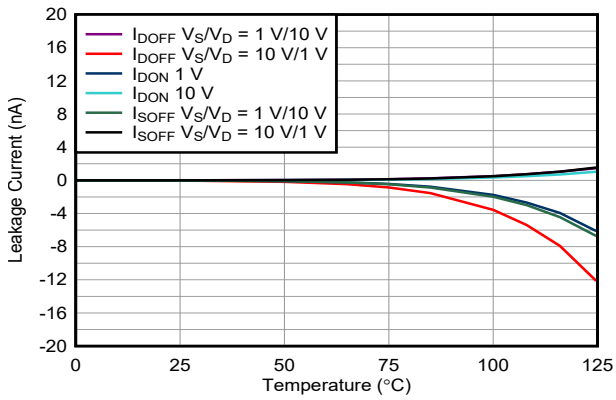

$V_{DD}$ = 36V, $V_{SS}$ = 0V

**Figure 5-8. On-Resistance vs Temperature**



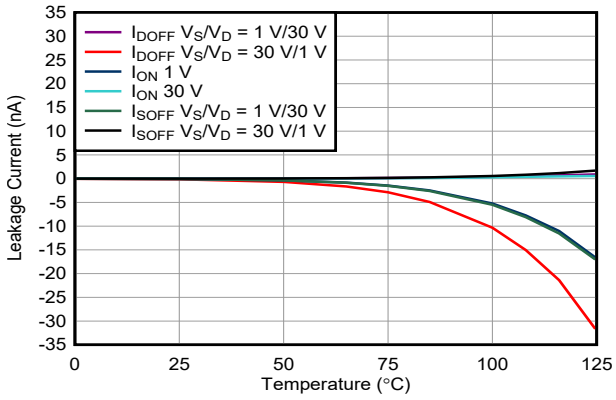

$V_{DD}$ = 15V, $V_{SS}$ = −15V

**Figure 5-9. On-Leakage vs Temperature**



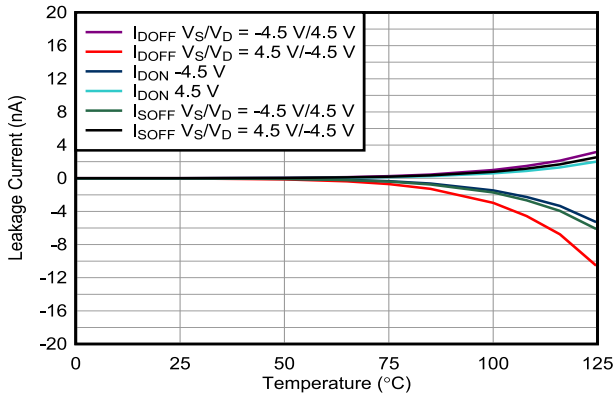

$V_{DD}$ = 12V, $V_{SS}$ = 0V

**Figure 5-10. On-Leakage vs Temperature**




$V_{DD}$ = 36V, $V_{SS}$ = 0V

**Figure 5-11. On-Leakage vs Temperature**




$V_{DD}$ = 5V, $V_{SS}$ = −5V

**Figure 5-12. On-Leakage vs Temperature**

## 5.14 Typical Characteristics (continued)

at $T_A$ = 25°C (unless otherwise noted)

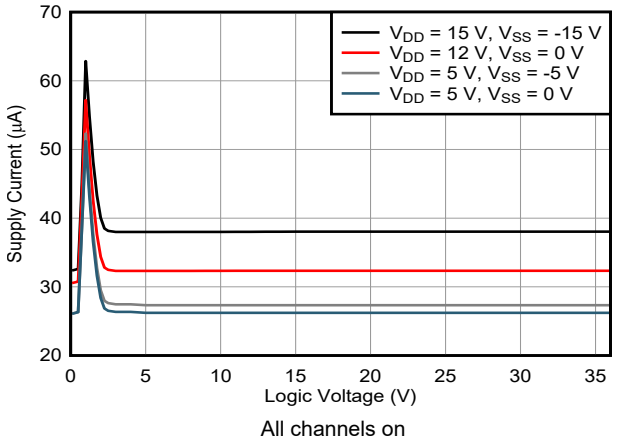



**Figure 5-13. Supply Current vs Logic Voltage**

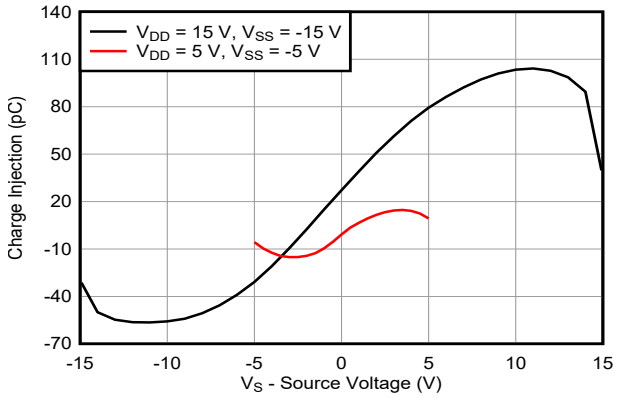



**Figure 5-14. Charge Injection vs Source Voltage – Dual Supply**

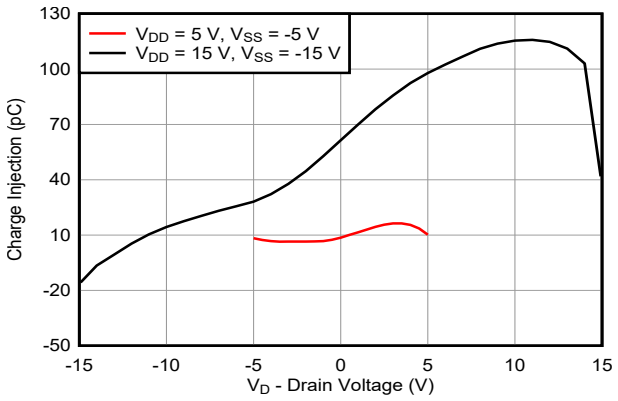



**Figure 5-15. Charge Injection vs Drain Voltage – Dual Supply**

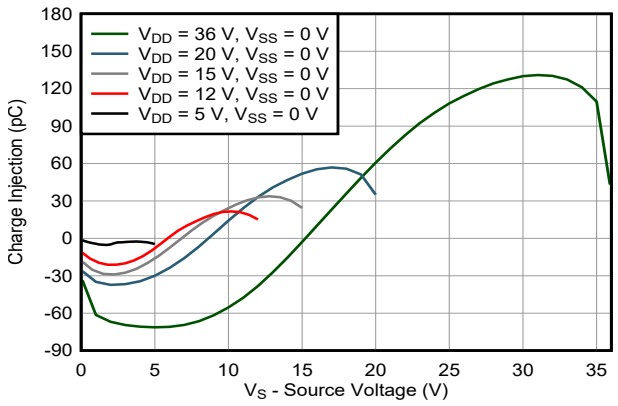



**Figure 5-16. Charge Injection vs Source Voltage – Single Supply**

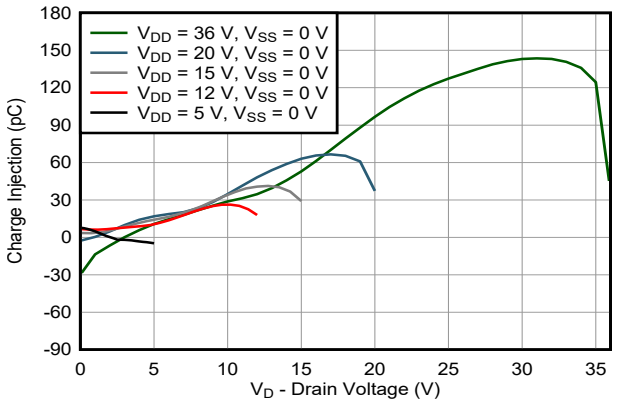



**Figure 5-17. Charge Injection vs Drain Voltage – Single Supply**

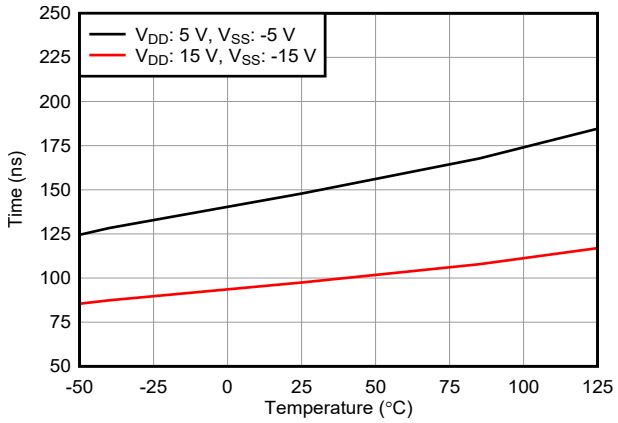



**Figure 5-18. $T_{TRANSITION}$ vs Temperature**

## 5.14 Typical Characteristics (continued)

at $T_A$ = 25°C (unless otherwise noted)

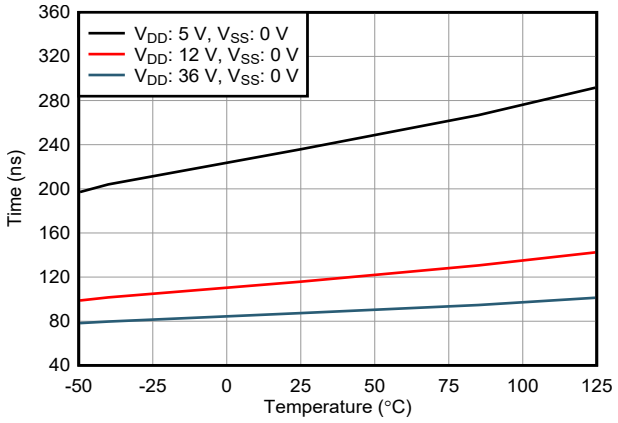
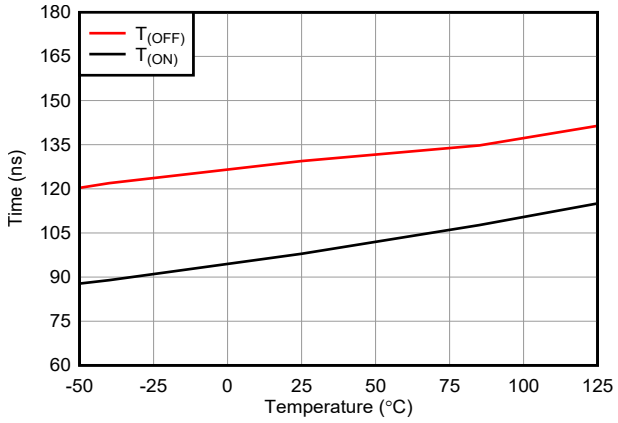
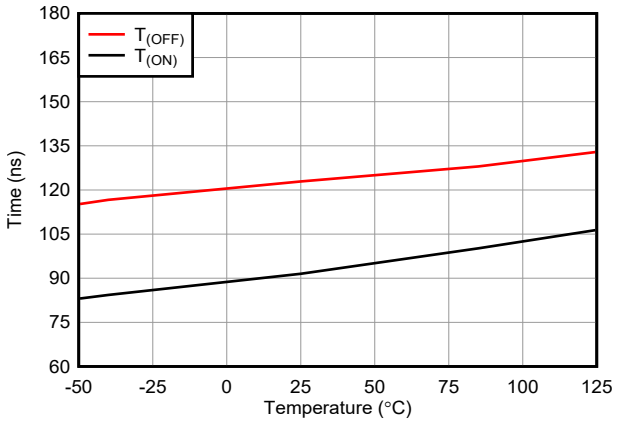



**Figure 5-19. $T_{TRANSITION}$ vs Temperature**



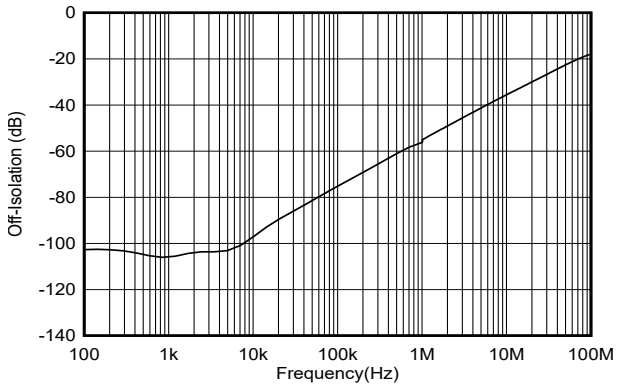

$V_{DD}$ = 15V, $V_{SS}$ = −15V

**Figure 5-20. $T_{ON\ (EN)}$ and $T_{OFF\ (EN)}$ vs Temperature**



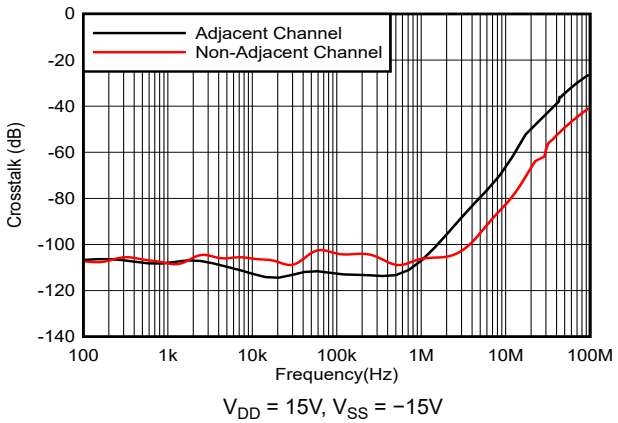

$V_{DD}$ = 36V, $V_{SS}$ = 0V

**Figure 5-21. $T_{ON\ (EN)}$ and $T_{OFF\ (EN)}$ vs Temperature**



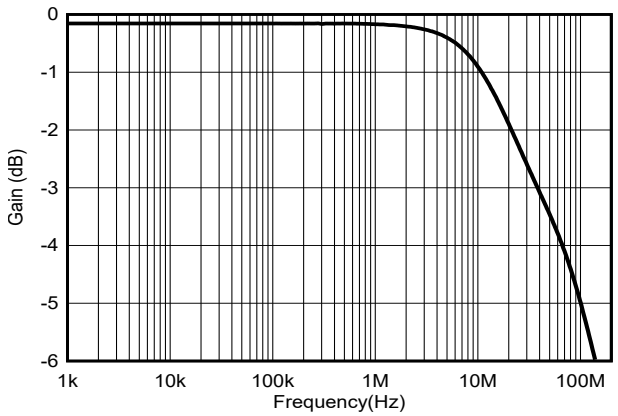

$V_{DD}$ = 15V, $V_{SS}$ = −15V

**Figure 5-22. Off-Isolation vs Frequency**




$V_{DD}$ = 15V, $V_{SS}$ = −15V

**Figure 5-23. Crosstalk vs Frequency**

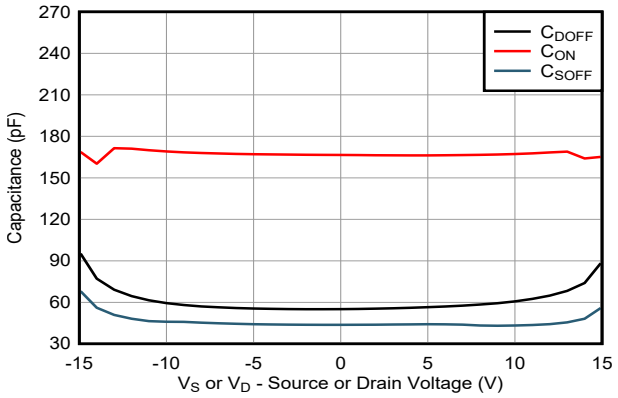



$V_{DD}$ = 15V, $V_{SS}$ = −15V

**Figure 5-24. On Response vs Frequency**

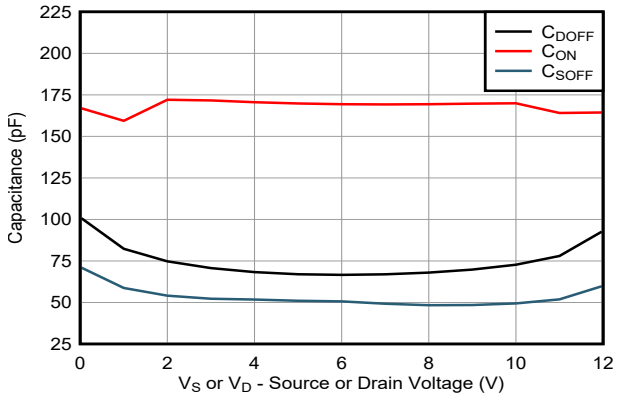
## 5.14 Typical Characteristics (continued)

at $T_A$ = 25°C (unless otherwise noted)




$V_{DD}$ = 15V, $V_{SS}$ = −15V

**Figure 5-25. Capacitance vs Source or Drain Voltage**




$V_{DD}$ = 12V, $V_{SS}$ = 0V

**Figure 5-26. Capacitance vs Source or Drain Voltage**

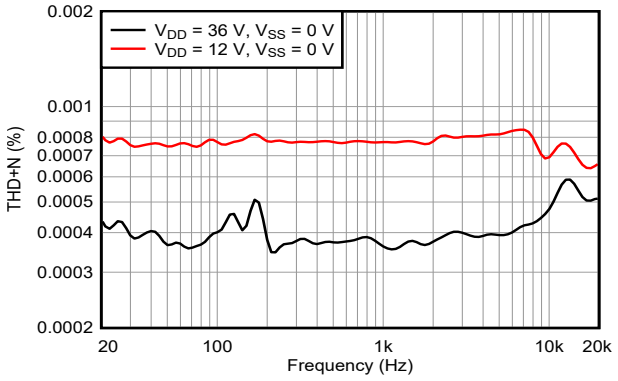



**Figure 5-27. THD+N vs Frequency – Single Supply**

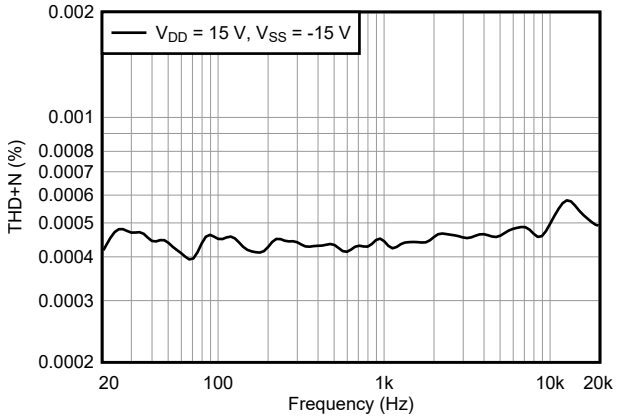
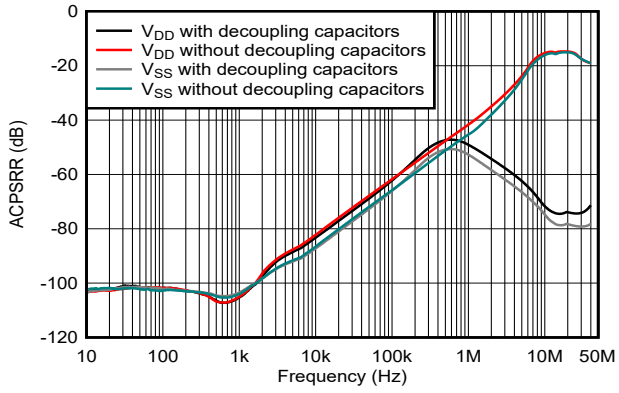



**Figure 5-28. THD+N vs Frequency – Dual Supply**




$V_{DD}$ = 15V, $V_{SS}$ = −15V

**Figure 5-29. ACPSRR vs Frequency**

# 6 Parameter Measurement Information

## 6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol $R_{ON}$ is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure $R_{ON}$. Voltage (V) and current ($I_{SD}$) are measured using this setup, and $R_{ON}$ is computed with $R_{ON} = V / I_{SD}$.

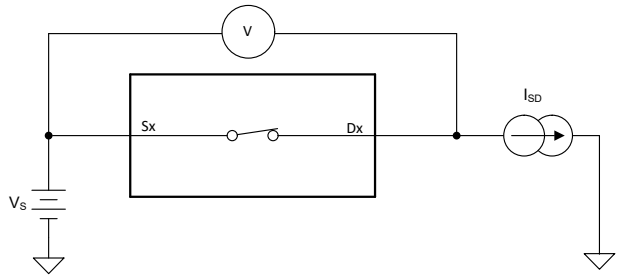



**Figure 6-1. On-Resistance Measurement Setup**

## 6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

- Source off-leakage current
- Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 6-2 shows the setup used to measure both off-leakage currents.

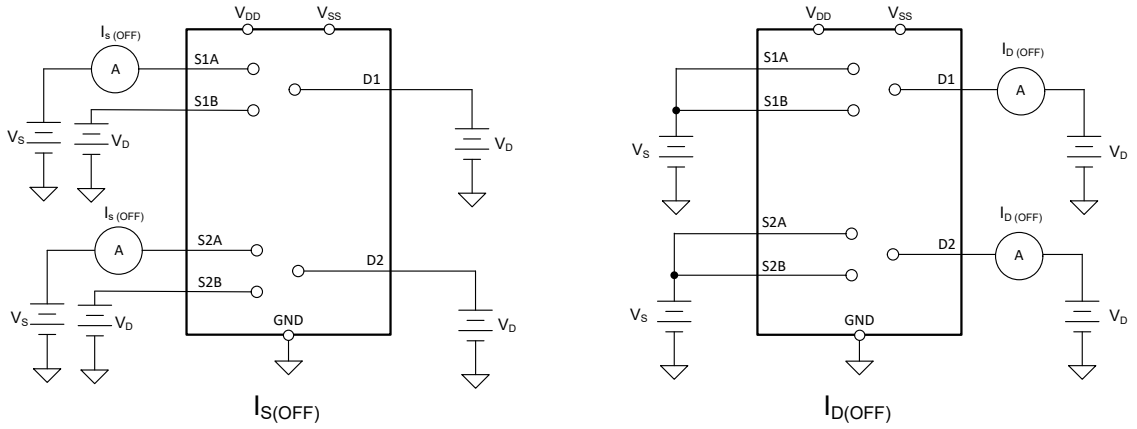



**Figure 6-2. Off-Leakage Measurement Setup**

## 6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

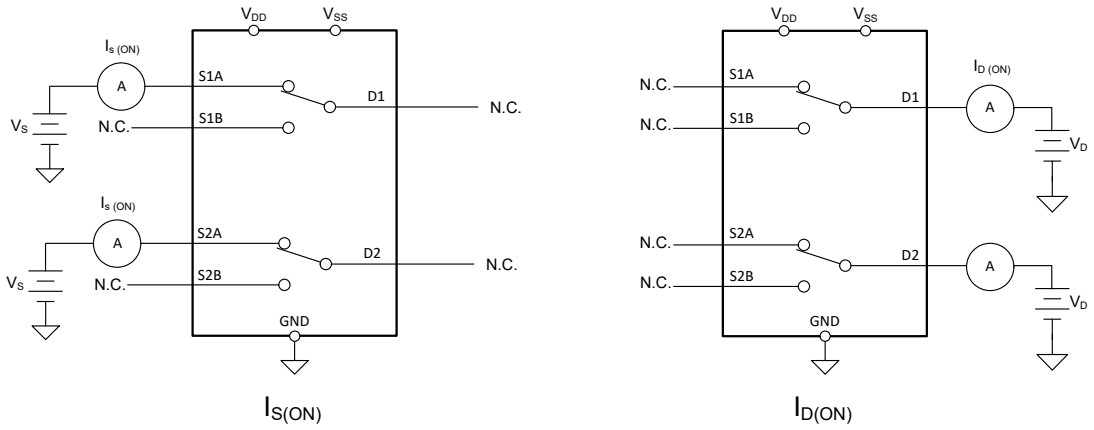



**Figure 6-3. On-Leakage Measurement Setup**

## 6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

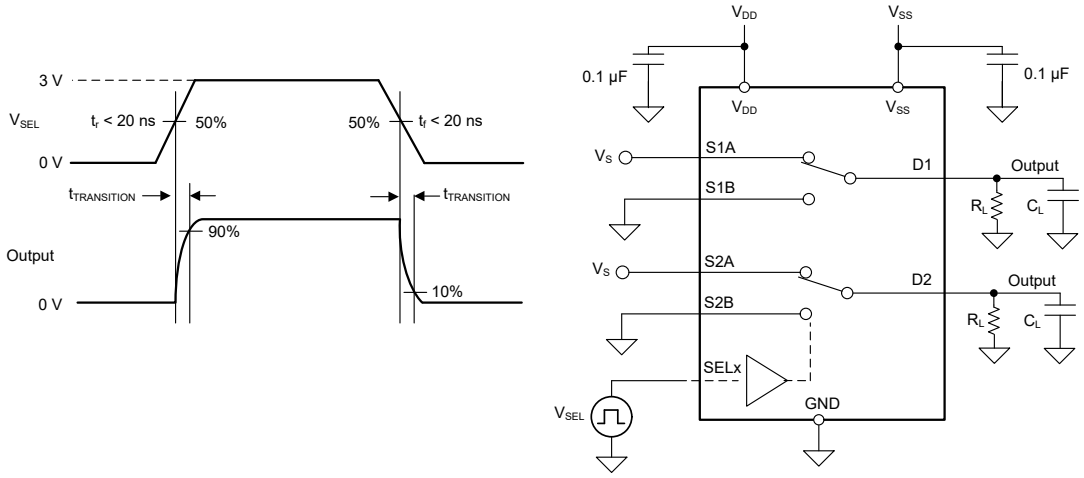



**Figure 6-4. Transition-Time Measurement Setup**

## 6.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-5 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-5 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

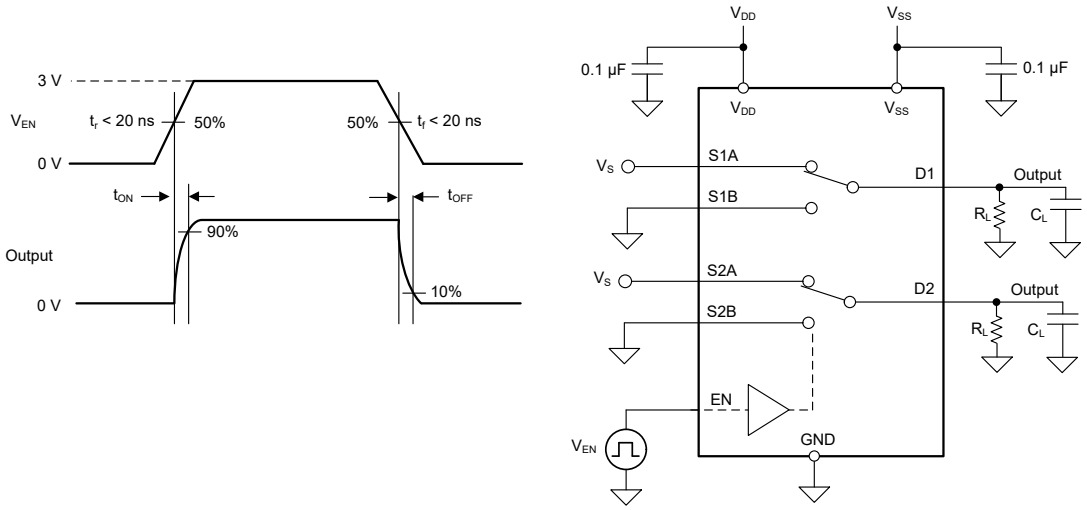



**Figure 6-5. Turn-On and Turn-Off Time Measurement Setup**

## 6.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 6-6 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

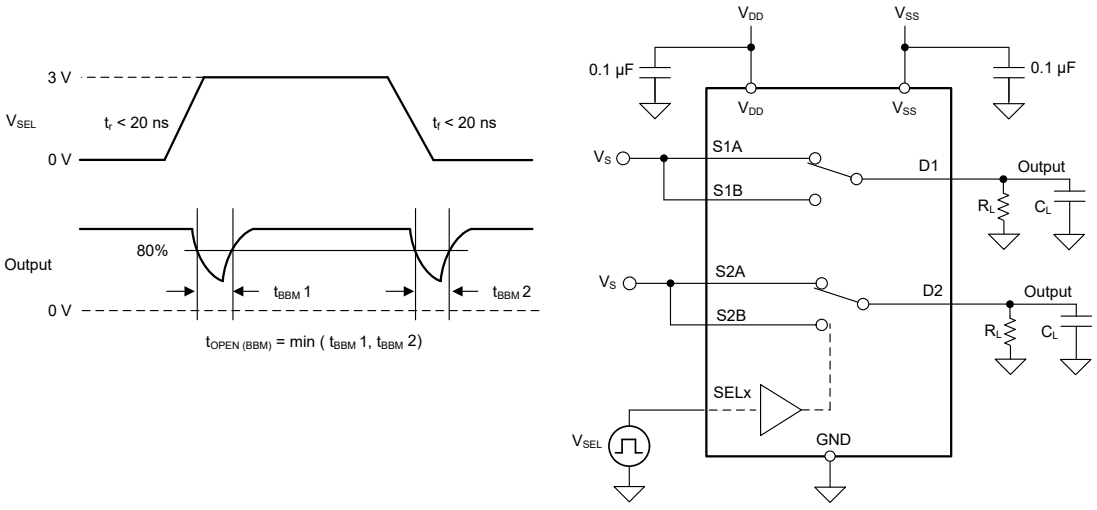



**Figure 6-6. Break-Before-Make Delay Measurement Setup**

## 6.7 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 6-7 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

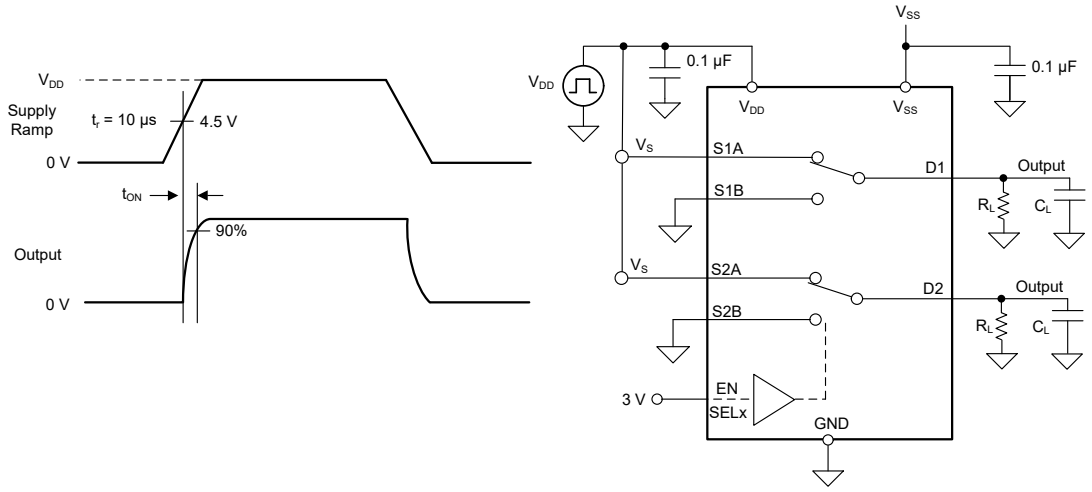



**Figure 6-7. $t_{ON\ (VDD)}$ Time Measurement Setup**

## 6.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-8 shows the setup used to measure propagation delay, denoted by the symbol $t_{PD}$.

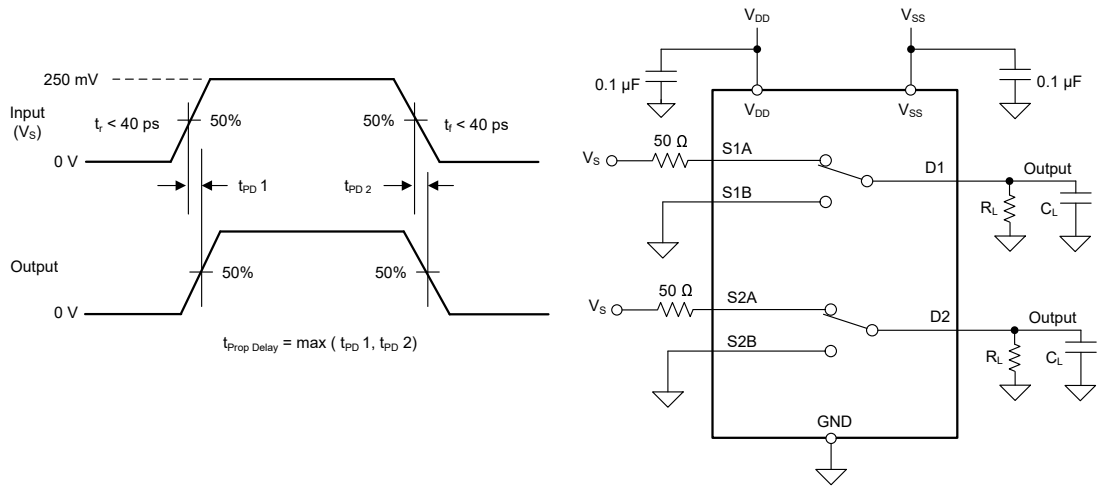



**Figure 6-8. Propagation Delay Measurement Setup**

## 6.9 Charge Injection

The TMUX6236 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol $Q_{INJ}$. Figure 6-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

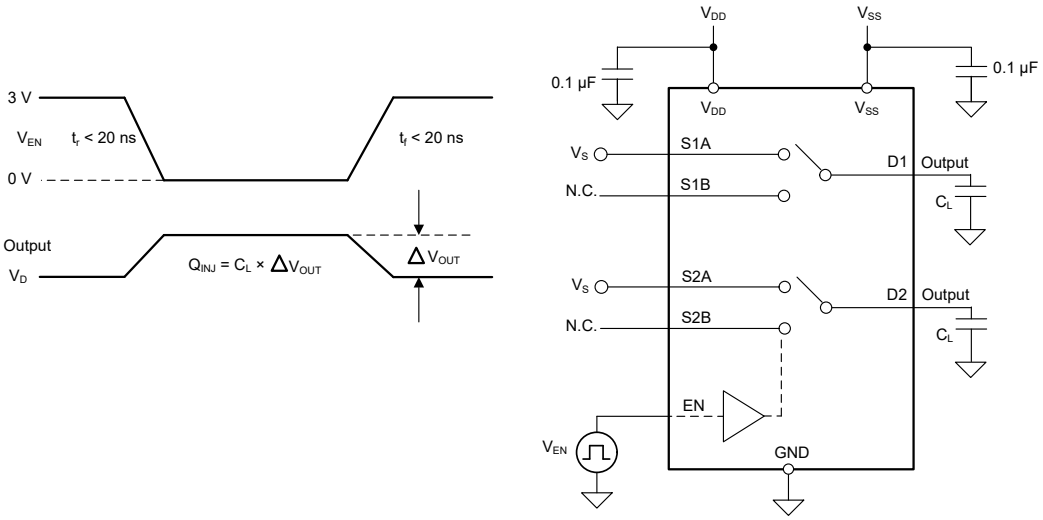



**Figure 6-9. Charge-Injection Measurement Setup**

## 6.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 6-10 shows the setup used to measure, and the equation used to calculate off isolation.

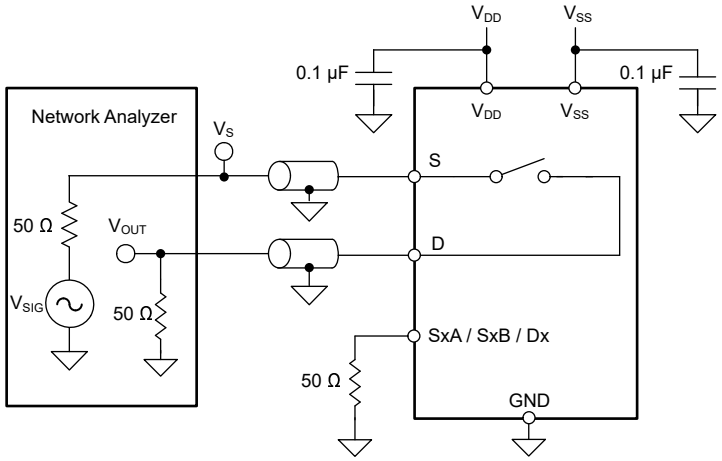



**Figure 6-10. Off Isolation Measurement Setup**

## 6.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 6-11 shows the setup used to measure and the equation used to calculate crosstalk.

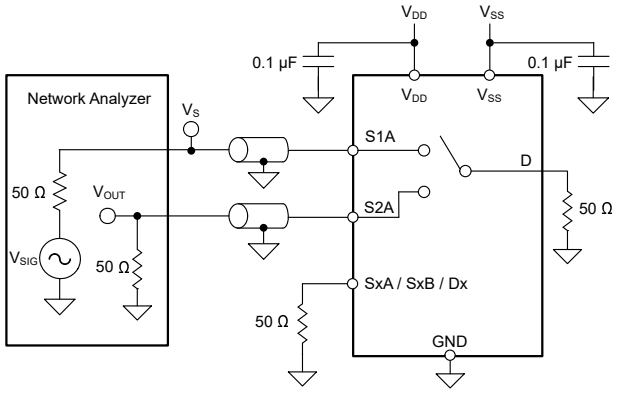



**Figure 6-11. Crosstalk Measurement Setup**

## 6.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 6-12 shows the setup used to measure bandwidth.

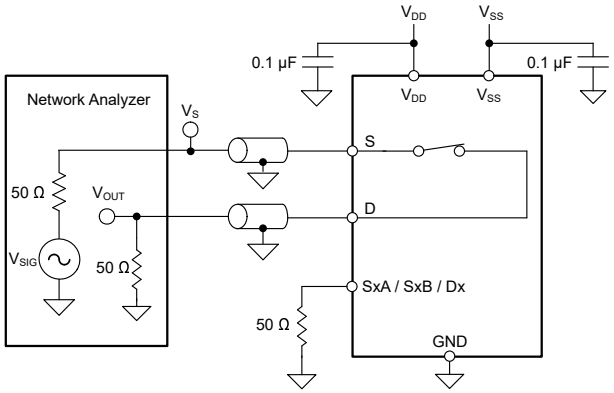



**Figure 6-12. Bandwidth Measurement Setup**

## 6.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD.

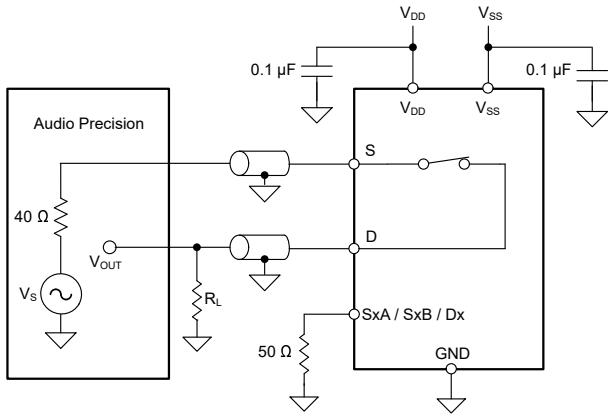



**Figure 6-13. THD Measurement Setup**

## 6.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

Figure 6-14 shows how the decoupling capacitors reduce high frequency noise on the supply pins. This helps stabilize the supply and immediately filter as much of the supply noise as possible.

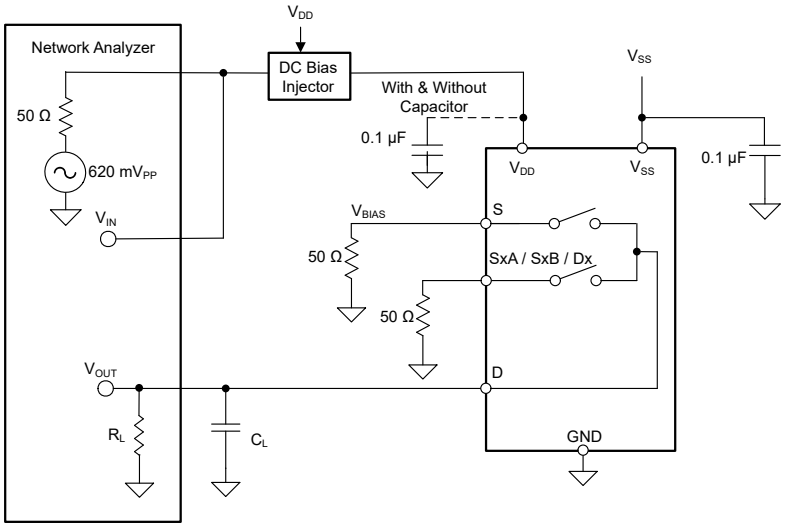
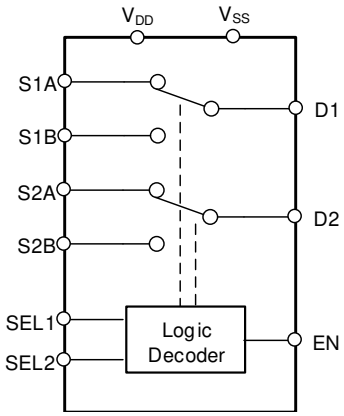



**Figure 6-14. ACPSRR Measurement Setup**

# 7 Detailed Description

## 7.1 Functional Block Diagram

The TMUX6236 is a 2:1, 2-channel multiplexer or demultiplexer. Each input is turned on or turned off based on the state of the select and enable pins.




## 7.2 Feature Description

### 7.2.1 Bidirectional Operation

The TMUX6236 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

### 7.2.2 Rail to Rail Operation

The valid signal path input or output voltage for TMUX6236 ranges from $V_{SS}$ to $V_{DD}$.

### 7.2.3 1.8V Logic Compatible Inputs

The TMUX6236 has 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the TMUX6236 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of materials (BOM) cost. For more information on 1.8V logic implementations, refer to *Simplifying Design with 1.8V logic Muxes and Switches*.

### 7.2.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX6236 has internal weak pull-down resistors to GND so that the logic pins are not left floating. The value of this pull-down resistor is approximately 4MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to three external components and reduces system size and cost.

### 7.2.5 Fail-Safe Logic

The TMUX6236 supports Fail-Safe Logic on the control input pins (EN and SEL) allowing for operation up to 36V above $V_{SS}$, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX6236 to be ramped to +36V while $V_{DD}$ and $V_{SS}$ = 0V. The logic control inputs are protected against positive faults of up to +36V in the powered-off condition, but does not offer protection against negative overvoltage conditions.

### 7.2.6 Latch-Up Immune

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX6236 is constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX6236 to be used in harsh environments. For more information on latch-up immunity refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

### 7.2.7 Ultra-Low Charge Injection

Figure 7-1 shows how the TMUX6236 device has a transmission gate topology. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

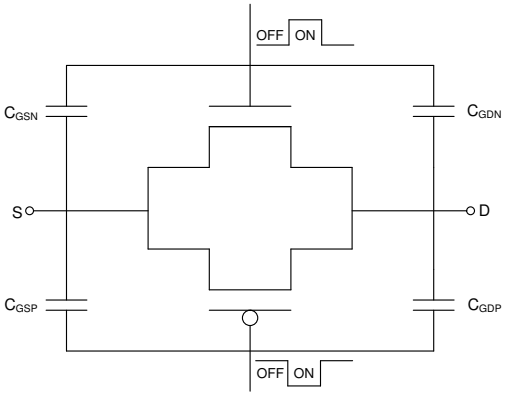



**Figure 7-1. Transmission Gate Topology**

The TMUX6236 contains specialized architecture to reduce charge injection on the Drain (Dx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the Source (Sx). This will push excess charge from the switch transition into the compensation capacitor on the Source (Sx) instead of the Drain (Dx). As a general rule, Cp should be 20x larger than the equivalent load capacitance on the Drain (Dx). Figure 7-2 shows charge injection variation with different compensation capacitors on the Source side. This plot was captured on the TMUX6219 as part of the TMUX62xx family with a 100pF load capacitance.

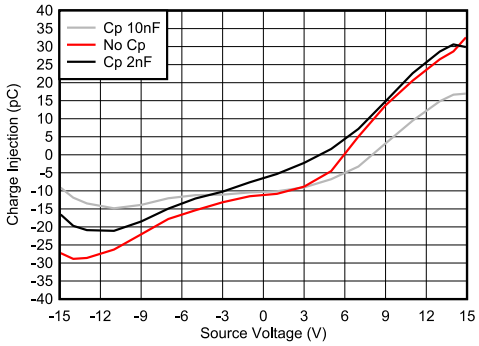



**Figure 7-2. Charge Injection Compensation**

## 7.3 Device Functional Modes

When the EN pin of the TMUX6236 is pulled high, one of the switches is closed based on the state of the SEL pin. When the EN pin is pulled low, both of the switches are in an open state regardless of the state of the SEL pin. The control pins can be as high as 36V.

## 7.4 Truth Tables

Table 7-1 provides the truth tables for the TMUX6236.

**Table 7-1. TMUX6236 Truth Table**

| EN | SELx | Selected Input Connected To Drain (D) Pin |
|---|---|---|
| 0 | X(1) | All channels are off (Hi-Z) |
| 1 | 0 | SxB |
| 1 | 1 | SxA |

(1) X denotes *do not care*.

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The TMUX6236 is part of the precision switches and multiplexers family of devices. This device operates with dual supplies (±4.5V to ±18V), a single supply (4.5V and 36V), or asymmetric supplies (such as, $V_{DD}$ = 5V and $V_{SS}$ = −8V), and offers rail-to-rail input and output. The TMUX6236 offers low $R_{ON}$, low on and off leakage currents and ultra-low charge injection performance. These features make the TMUX6236 a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

## 8.2 Typical Application

Differential reference signal switching is one application for the TMUX6236. AC reference signals are utilized in a variety of use cases as a stable reference in signal processing. Often times a differential signal is needed to reduce noise and keep signal integrity. To easily swap the direction and frequency of this reference signal, a 2:1, 2 channel precision multiplexer like the TMUX6236 can be used. Figure 8-1 shows a circuit example utilizing the TMUX6236 to control the AC reference signals. The switch can easily be configured for a differential signal on either X1 or X2. Additionally, if both SEL pins are low, then the output will be set to ground so that there is no active operation and reduce power consumption. The break-before-make feature allows transferring of a signal from one port to another, without shorting the inputs together. This device also offers low charge injection, which makes this device suitable for high precision systems.

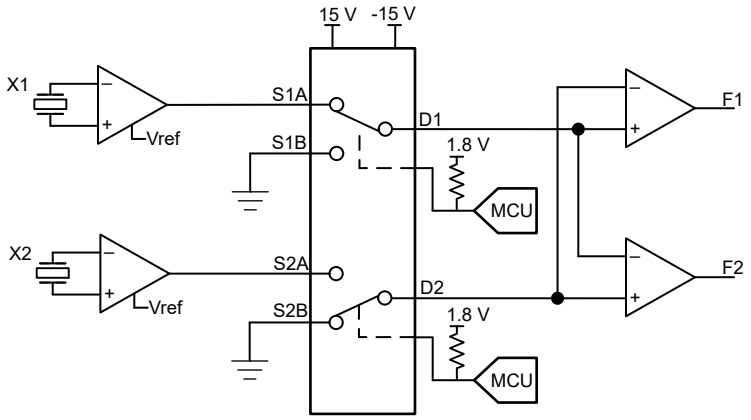



**Figure 8-1. Differential Reference Switching**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

**Table 8-1. Design Parameters**

| PARAMETERS | VALUES |
|---|---|
| Supply ($V_{DD}$) | 15V |
| Supply ($V_{SS}$) | −15V |
| MUX I/O signal range | −15V to 15V (Rail-to-Rail) |
| Control logic thresholds | 1.8V compatible (up to $V_{DD}$) |
| EN | EN pulled high to enable the switch |

### 8.2.2 Detailed Design Procedure

The TMUX6236 can operate without any external components except for the supply decoupling capacitors. All inputs passing through the switch must fall within the recommended operating conditions of the TMUX6236, including signal range and continuous current. The signal range for this design can be −15V to +15V and the maximum continuous current can be up to 330mA for wide-range current measurement with a positive supply of 15V on $V_{DD}$ and negative supply of −15V on $V_{SS}$ (for more information, see Section 5.4). The TMUX6236 device are bidirectional, single-pole double-throw (SPDT) switches that offer low on-resistance, low leakage, and low power. These features make these devices suitable for precision and power sensitive applications.

### 8.2.3 Application Curve

The low on-resistance of TMUX6236 and ultra-low charge injection performance make this device an excellent choice for implementing high precision industrial systems. The TMUX6236 contains specialized architecture to reduce charge injection on the Drain side (D) (for more details, see Section 7.2.7). Figure 8-2 shows the plot for the charge injection versus source voltage for the TMUX6236.

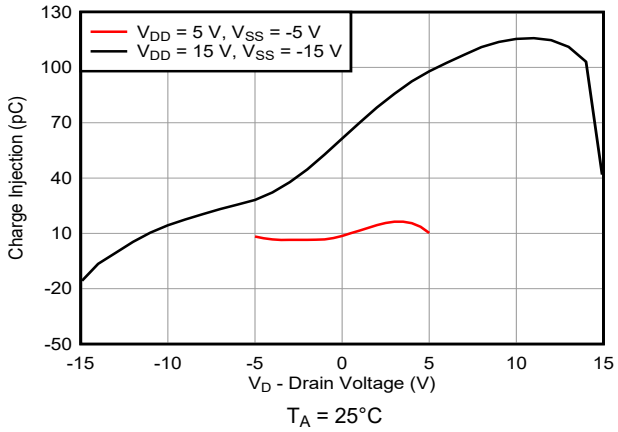



**Figure 8-2. Charge Injection vs Drain Voltage**

## 8.3 Power Supply Recommendations

The TMUX6236 operates across a wide supply range of ±4.5V to ±18V (4.5V to 36V in single-supply mode). The device also performs well with asymmetrical supplies such as $V_{DD}$ = 12V and $V_{SS}$= –5V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1µF to 10µF at both the $V_{DD}$ and $V_{SS}$ pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems or systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Always ensure the ground (GND) connection is established before supplies are ramped.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

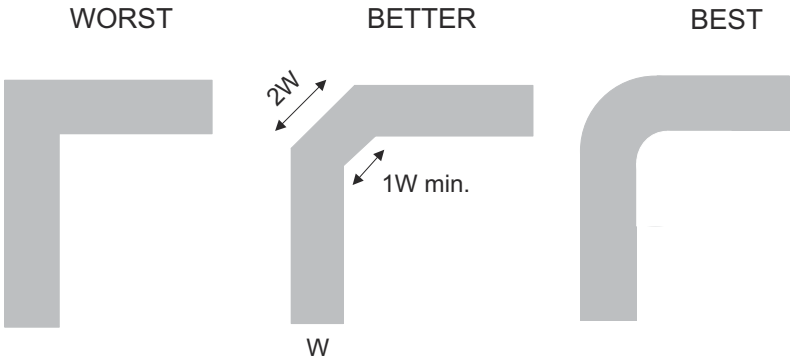



**Figure 8-3. Trace Example**

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points; through-hole pins are not recommended at high frequencies.

Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD/VSS and GND. TI recommends a 0.1µF and 1µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

### 8.4.2 Layout Example

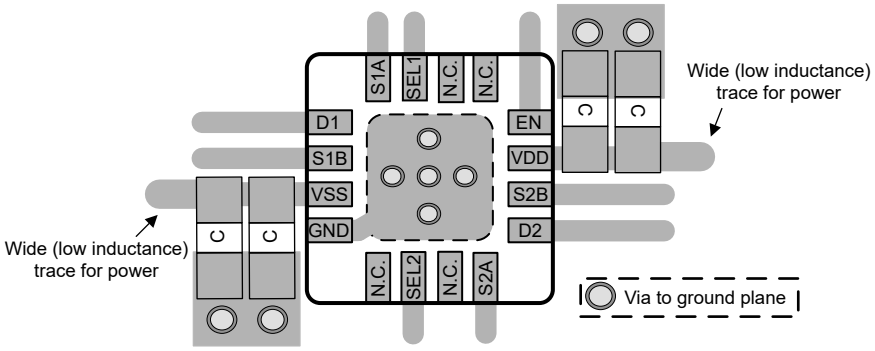



**Figure 8-4. TMUX6236RUM Layout Example**

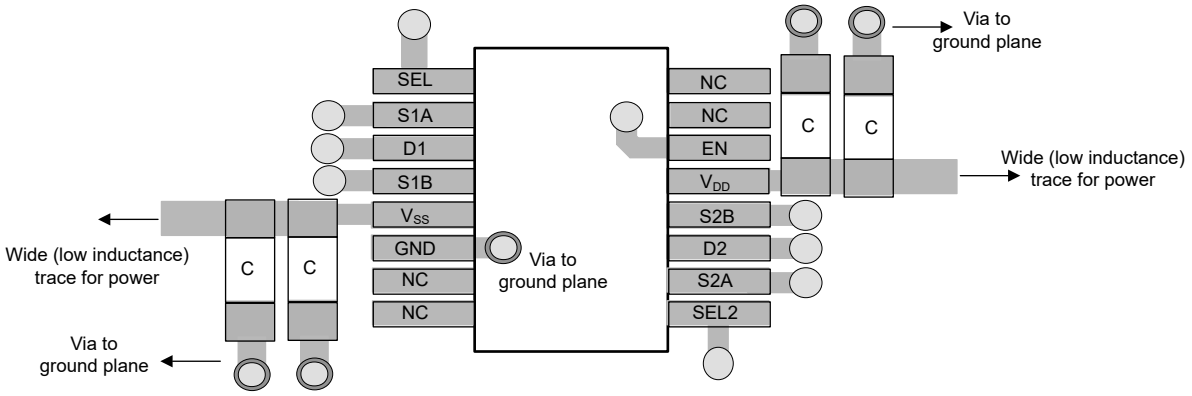



**Figure 8-5. TMUX6236PW Layout Example**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches* application brief
- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application reports
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit* circuit design

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

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## 9.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

## 9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (December 2023) to Revision C (February 2024) | Page |
|---|---|
| • Corrected pin numbers in the *Pin Functions* table | 3 |

| Changes from Revision A (July 2022) to Revision B (December 2023) | Page |
|---|---|
| • Added the *PW* package information | 1 |

| Changes from Revision * (April 2022) to Revision A (July 2022) | Page |
|---|---|
| • Changed the status of the data sheet from: *Advanced Information* to: *Production Data* | 1 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TMUX6236PWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T236 |
| TMUX6236PWR.B | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T236 |
| TMUX6236RUMR | Active | Production | WQFN (RUM) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TMUX T236 |
| TMUX6236RUMR.B | Active | Production | WQFN (RUM) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TMUX T236 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

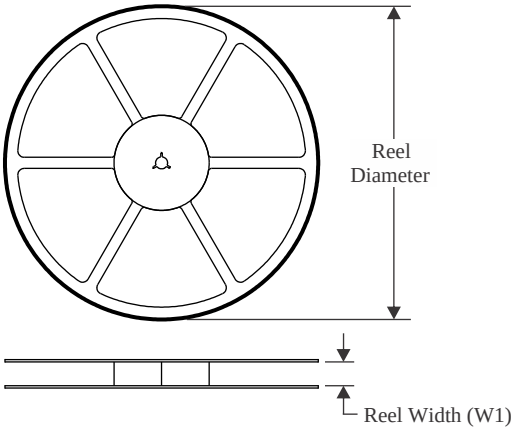
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

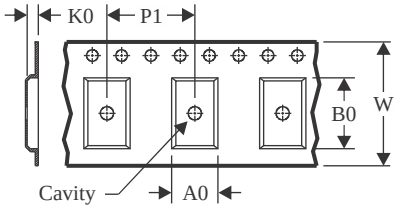
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

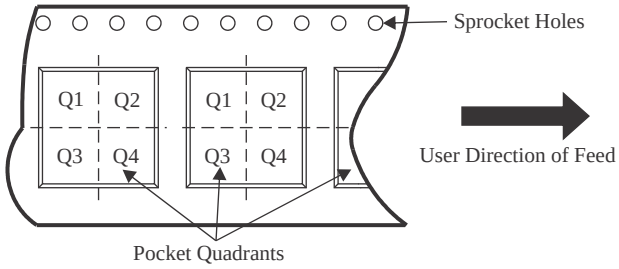



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

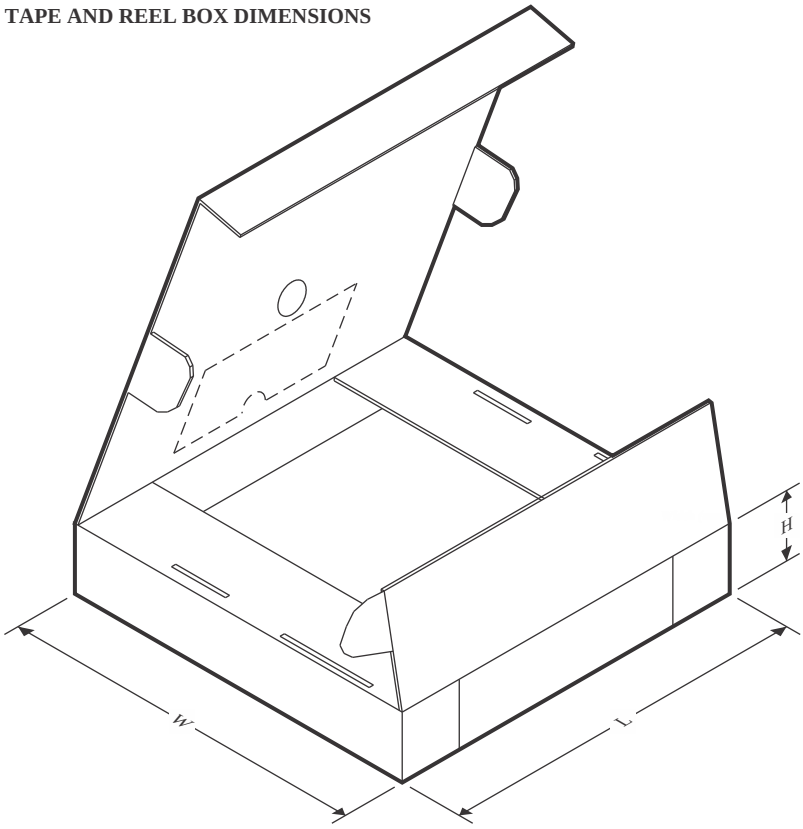
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX6236PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TMUX6236RUMR | WQFN | RUM | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMUX6236PWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| TMUX6236RUMR | WQFN | RUM | 16 | 3000 | 367.0 | 367.0 | 35.0 |

# GENERIC PACKAGE VIEW

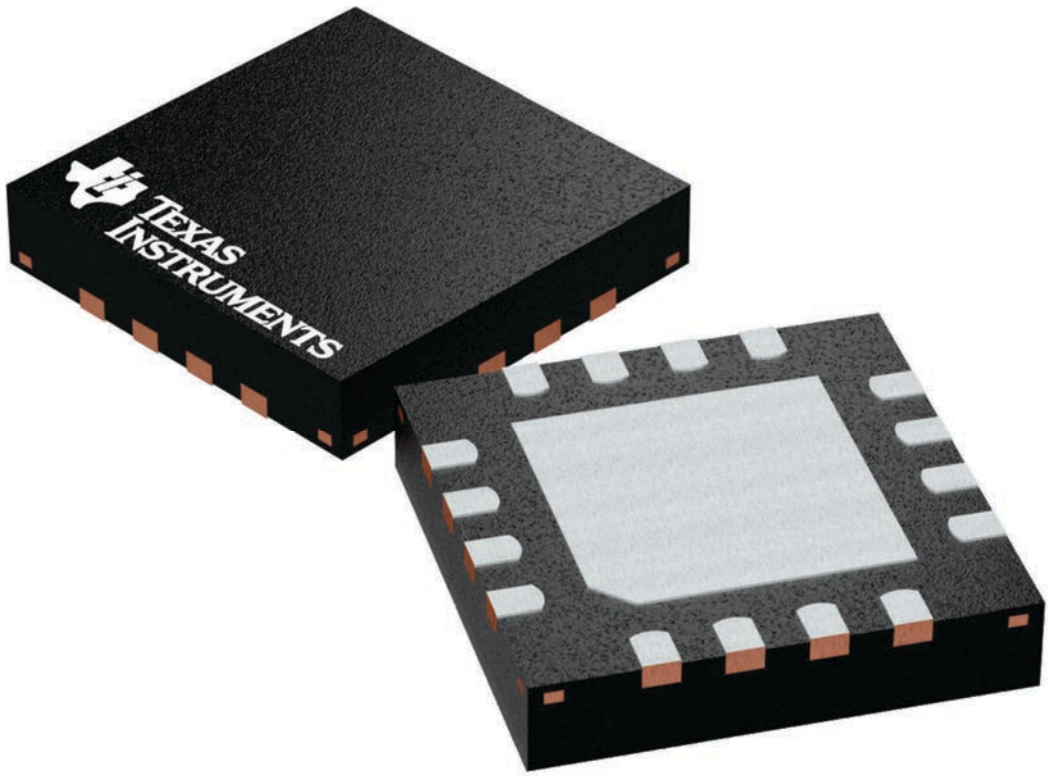
## RUM 16

## WQFN - 0.8 mm max height

**4 x 4, 0.65 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



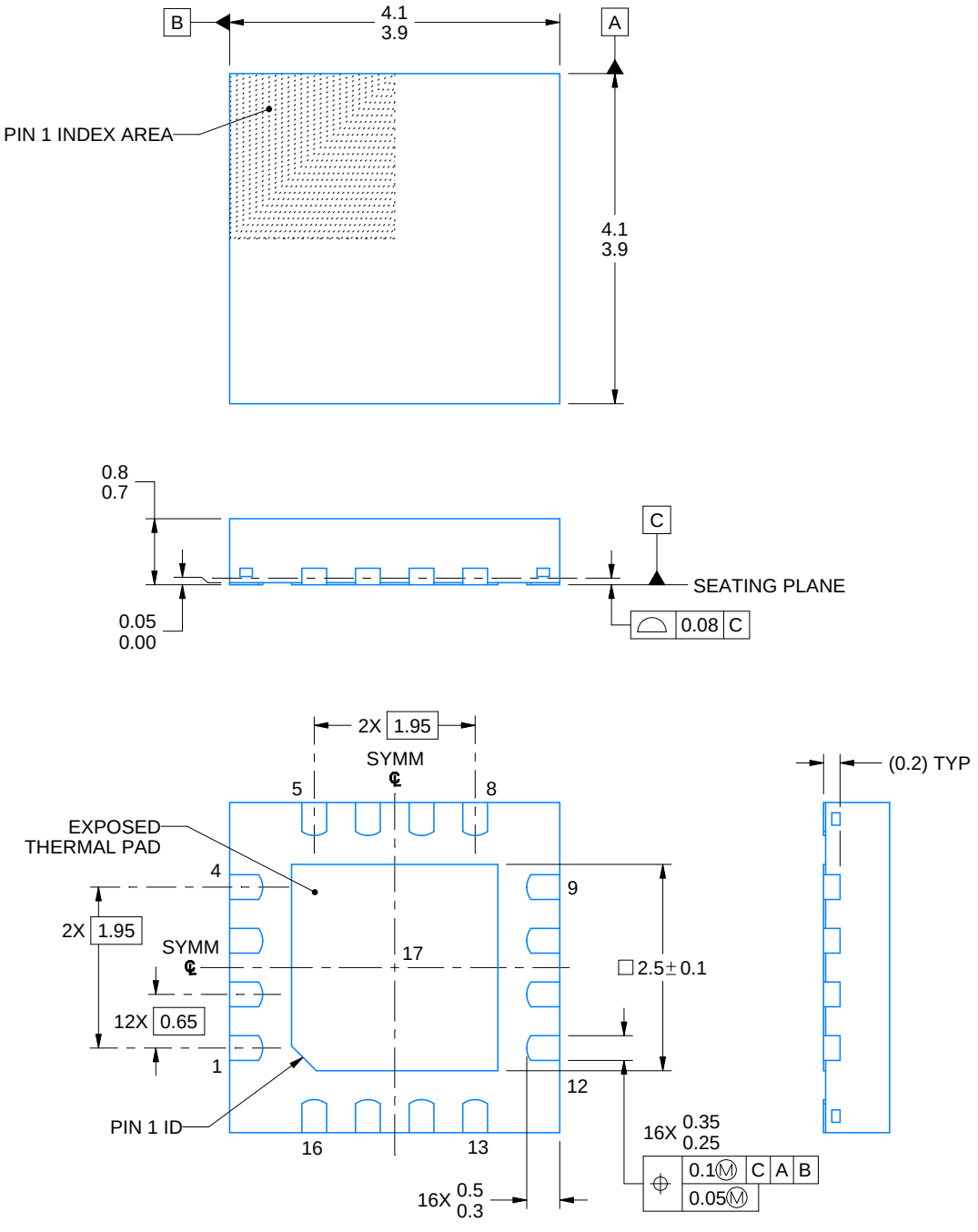

4224843/A

# RUM0016E

# PACKAGE OUTLINE

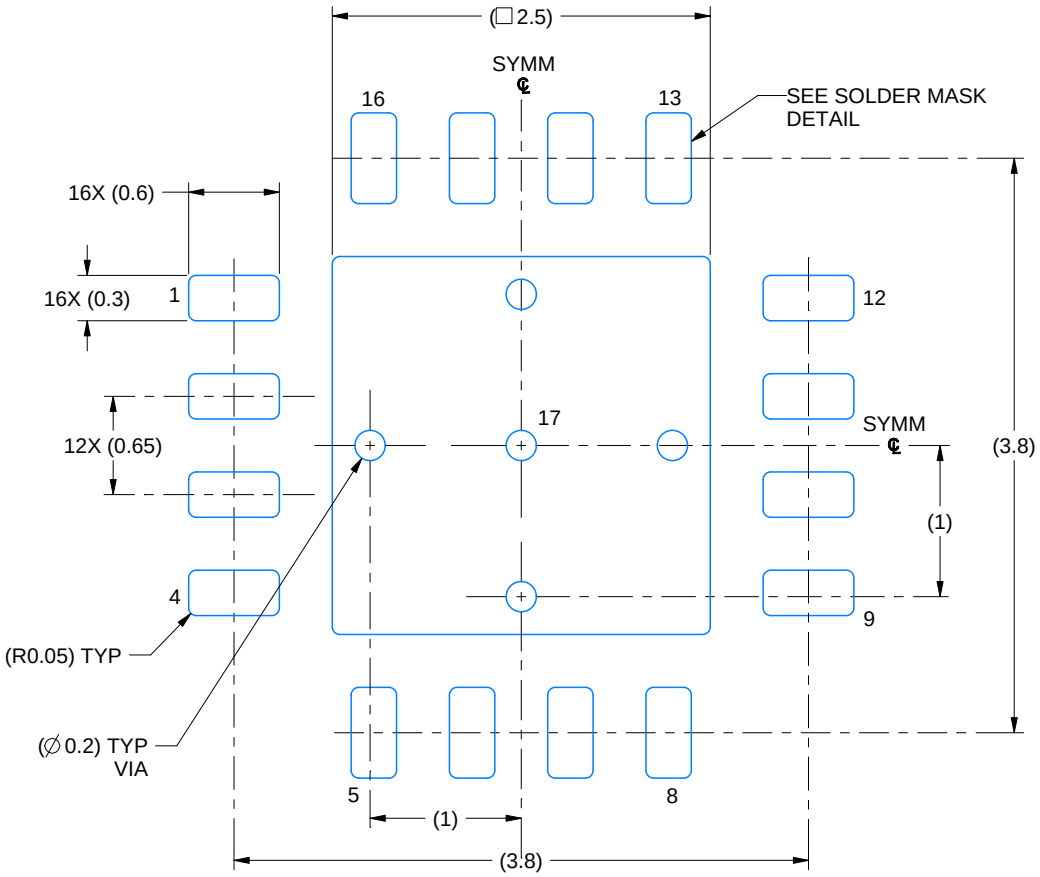
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

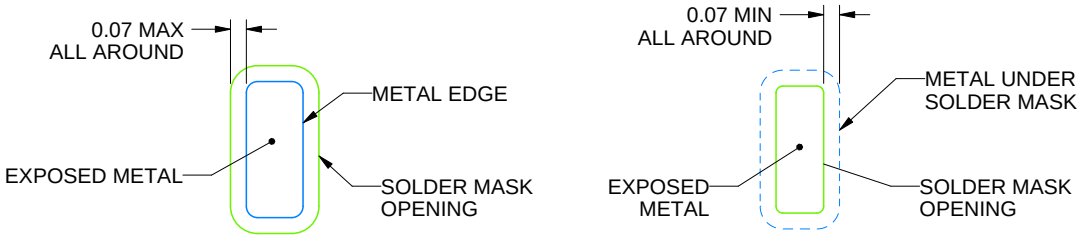



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

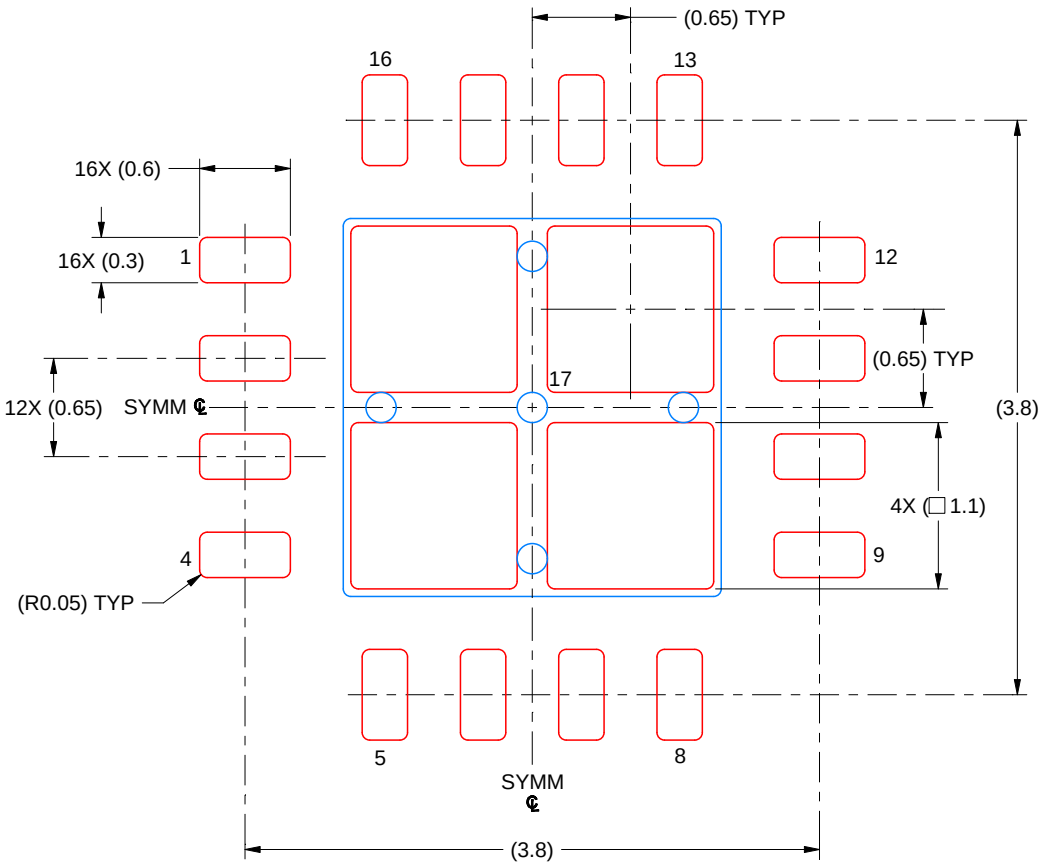



SOLDER MASK DETAILS

4224815/A 02/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224815/A 02/2019

NOTES: (continued)

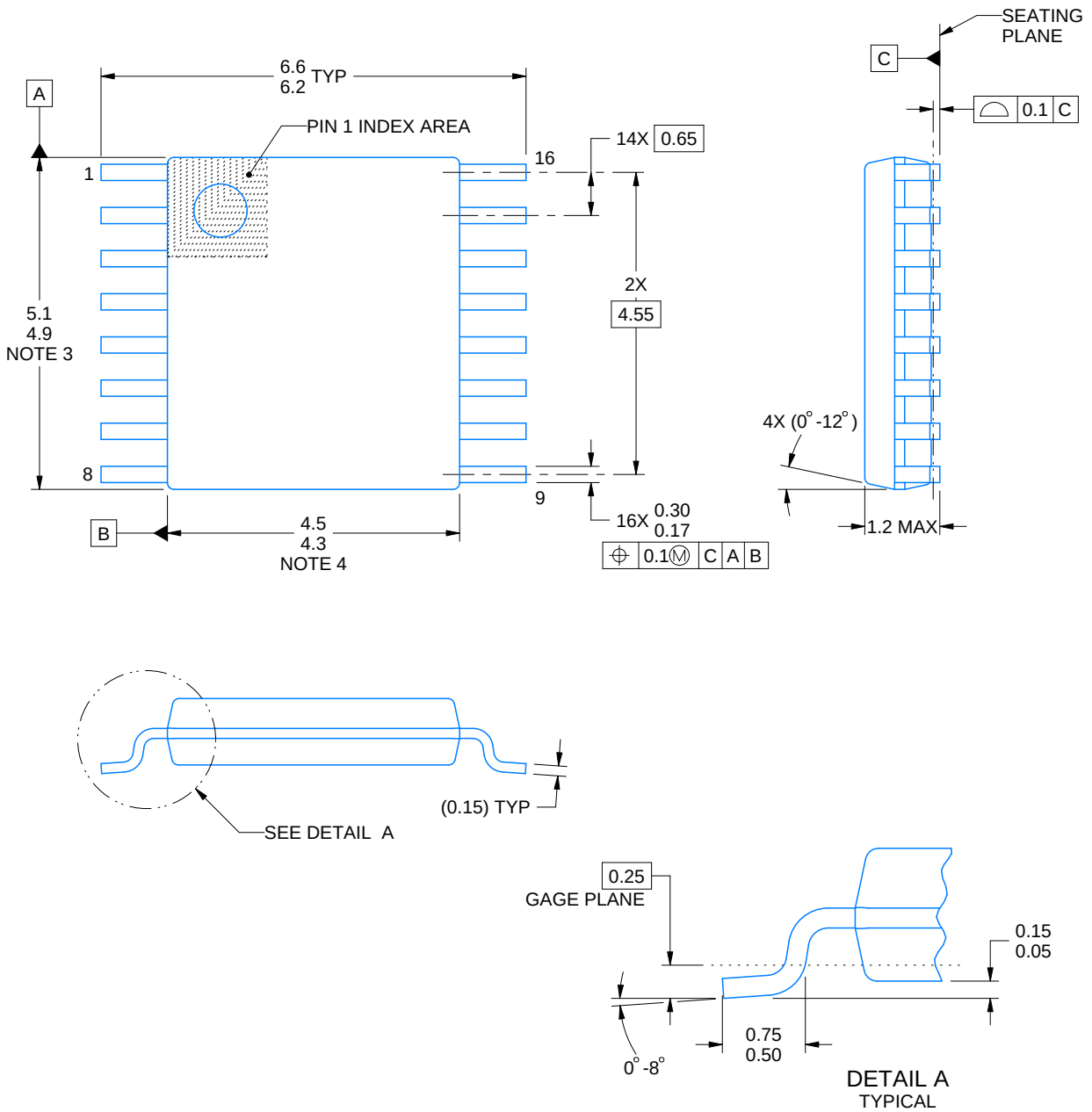
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## PW0016A

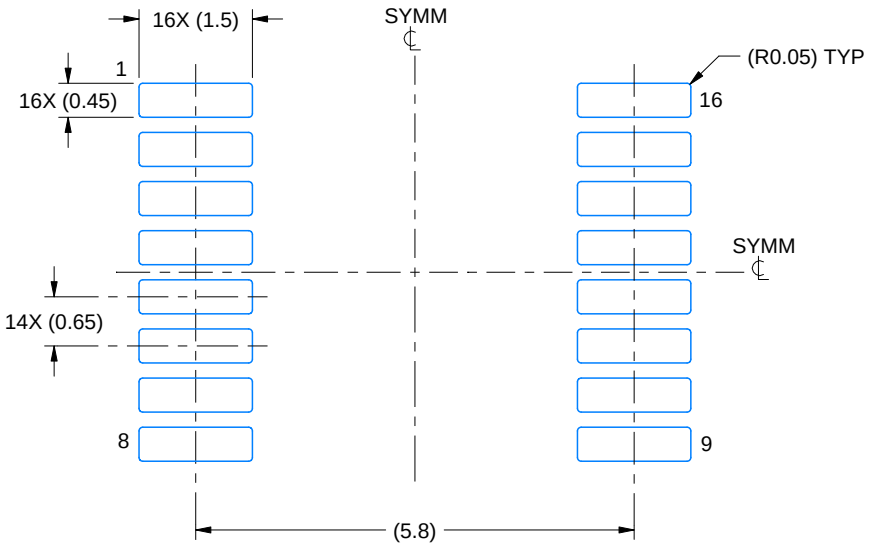
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



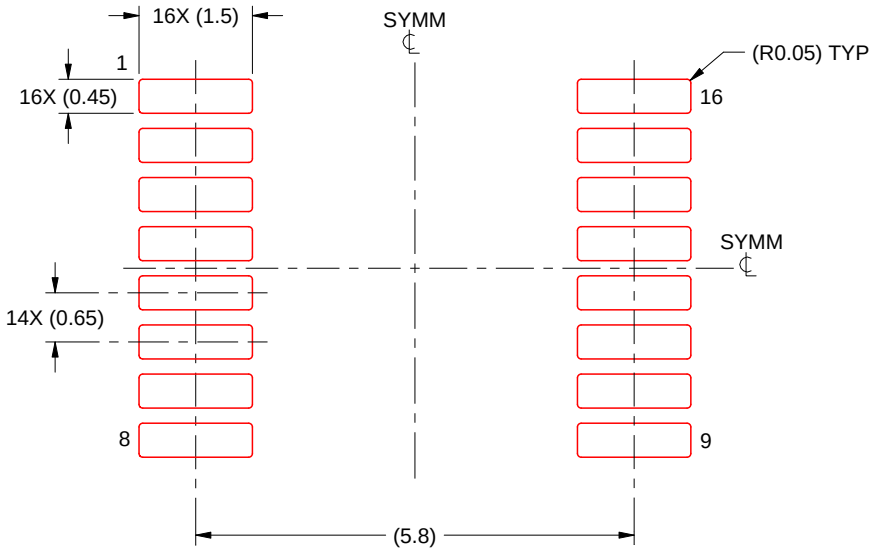

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

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