Application Note

Understanding TAS5431-Q1 Load Diagnostics

Trevor Finnigan

ABSTRACT

Reliable load diagnostics are critical in automotive audio applications to detect wiring faults and monitor speaker integrity. The TAS5431-Q1 automotive Class D amplifier integrates load diagnostic capabilities to detect common wiring and load faults. This application report details these capabilities and how to leverage them.

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1 Introduction

TAS5431-Q1 is an automotive-qualified mono Class-D audio amplifier that includes integrated load diagnostics to monitor the integrity of the wiring and speaker load. Figure 1-1 shows the typical application diagram for this device and the associated microprocessor.

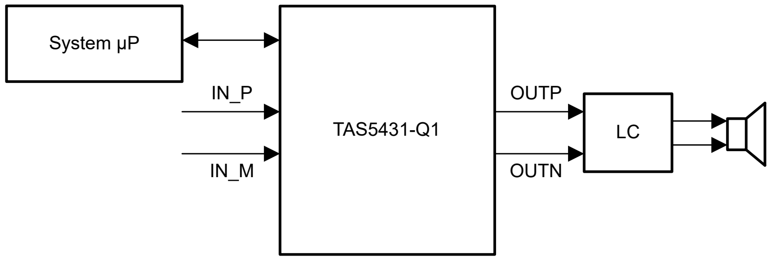

Figure 1-1. Simplified Application Diagram

These integrated diagnostics detect four types of speaker or wiring faults and report the fault status to the system micro-processor through I^{2}C and the $\overline{\text{FAULT}}$ pin, where appropriate. This application report details the load diagnostic capabilities of the amplifier including the types of faults monitored, the diagnostic sequence and associated timing, and the response of the amplifier to various fault conditions.

2 TAS5431-Q1 Load Diagnostics

2.1 Types of Load Faults Detected

TAS5431-Q1 load diagnostics monitor the following speaker conditions:

- Short-to-GND
- Short-to-PVDD
- Short across load
- Open load

2.2 Diagnostic Sequence, Timing, and Fault Response

The load diagnostic sequence occurs under these conditions:

- On de-assertion of the $\overline{\text{STANDBY}}$ pin
- Immediately following fault recovery from DC detect, overcurrent, overvoltage*, undervoltage, or overtemperature events

*Note, load diagnostics run after every two overvoltage (OV) events

The test sequence consists of four phases totaling approximately 229ms, assuming no fault is present:

1. Discharge phase (~75 ms)
2. Ramp up (~52 ms)
3. Check (~50 ms)
4. Ramp down (~52 ms)

During the *check* phase, 10mA is sourced through the load from OUTP to OUTM, and the differential voltage is measured to determine the state of the load. See the TAS5431-Q1 datasheet for specifications on the load diagnostics fault detection thresholds.

Upon completion of a load diagnostics sequence in which no faults are detected, the audio output starts. If a fault is detected, or if a large output capacitance exists, the check phase may repeat up to five times, resulting in a maximum duration of approximately 429ms for a single load diagnostics sequence. The response to the fault depends on the type of fault that is present:

Open Load:

- Audio remains enabled.
- Only fault register status is updated.

Shorted load, short-to-PVDD, short-to-GND:

- Output is forced into Hi-Z state
- Load diagnostics repeat indefinitely until fault is cleared
- Fault register status is updated
- $\overline{\text{FAULT}}$ pin is asserted

While the load diagnostics sequence is active, bit D5 of the *Status and Load Diagnostic Register* (0x02) is asserted. This bit does not get de-asserted until exiting the load diagnostic sequence and starting the audio output, either through passing the diagnostics check, or the detection of an open load. In the case of any other load diagnostics failure, the bit remains asserted the entire duration that the fault is present and the load diagnostics sequence is repeating.

If a fault unrelated to diagnostics (voltage fault, thermal fault, overcurrent fault) occurs during diagnostics, the device exits diagnostics early and it is possible this can result in a pop or a click on the speaker output.

Figure 2-1 summarizes the diagnostic sequence, timing, and fault response.

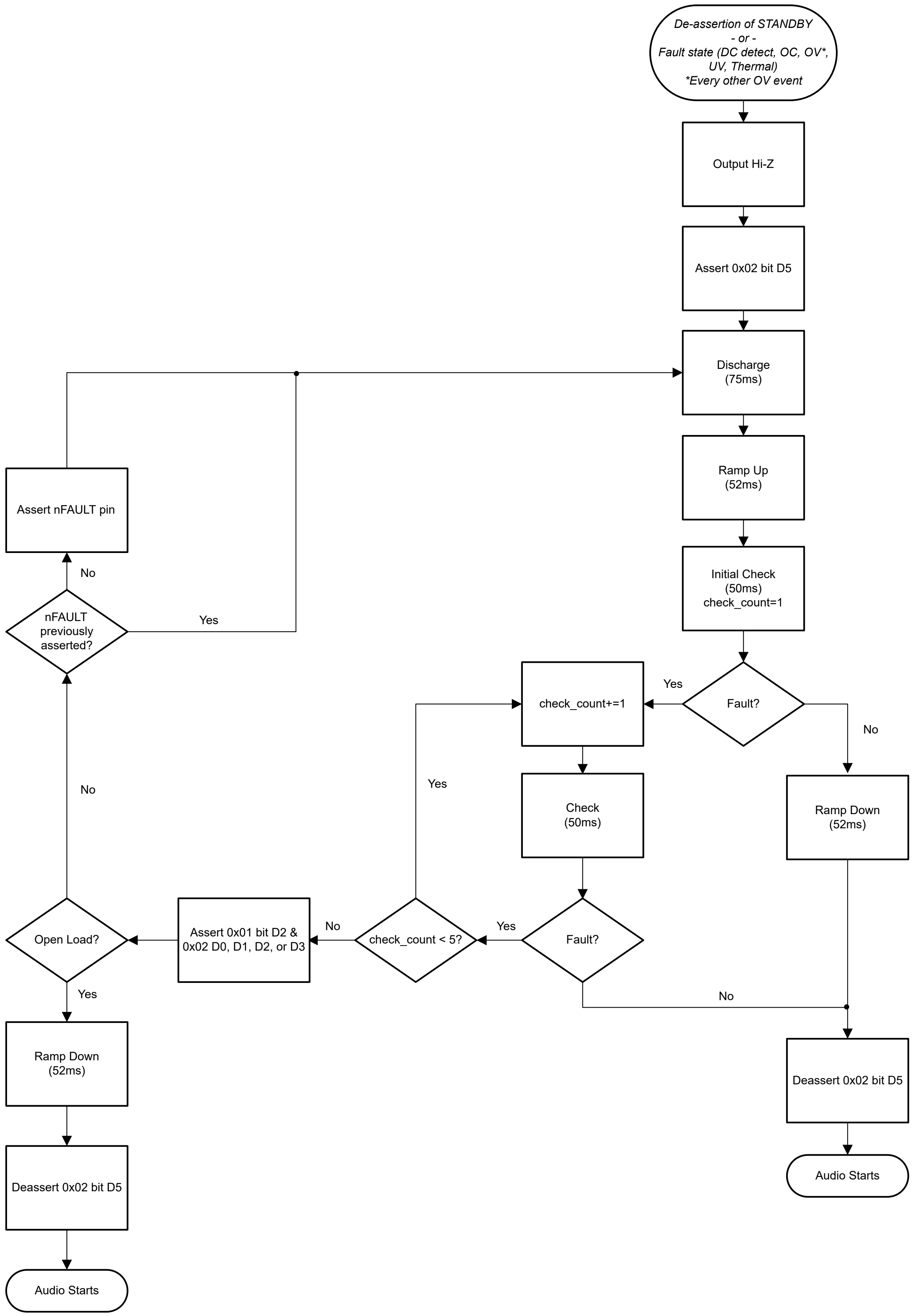

Figure 2-1. Flow Diagram of Diagnostic Sequence, Timing, and Fault Response

2.3 Register Reporting

If load diagnostics detects that a fault is present, bit D3 of the *Fault Register* (0x01) is asserted. The specific fault is further detailed in the *Status and Load Diagnostic Register* (0x02) as listed in Table 2-1

Table 2-1. Subset of the Status and Load Diagnostic Register Associated with Load Diagnostics Faults

Bit	Condition
D3	Open load detected
D2	Shorted load detected
D1	Output short to ground
D0	Output short to PVDD

2.4 Measuring the Load Diagnostics Waveform Using an Oscilloscope

When troubleshooting a fault scenario, it is helpful to use an oscilloscope to understand what is physically happening during the load diagnostics sequence. As indicated in section 2.2, during the load diagnostics *check* phase, 10mA is sourced through the load from OUTP to OUTM, and the differential voltage is measured by the IC to determine the state of the load. Since the reference point for the differential voltage measurement is the pin of the IC, it is important to place the oscilloscope probes as close as possible to the IC pins. Probing at the speaker itself leads to inaccurate results, as that bypasses the voltage drop introduced by the speaker wires.

The following set of figures shows the expected waveform of the diagnostics sequence under passing conditions and the various faulted conditions.

Figure 2-2 shows a passing waveform across an 8Ω load. Observe that the diagnostics sequence begins upon de-assertion of $\overline{\text{STANDBY}}$ and the sequence takes ~229ms to complete. During the 50ms *check* phase, the voltage differential is 80mV which is the expected result of the 10mA source current across the 8Ω load. The $\overline{\text{FAULT}}$ pin remains de-asserted the entire duration of the sequence.

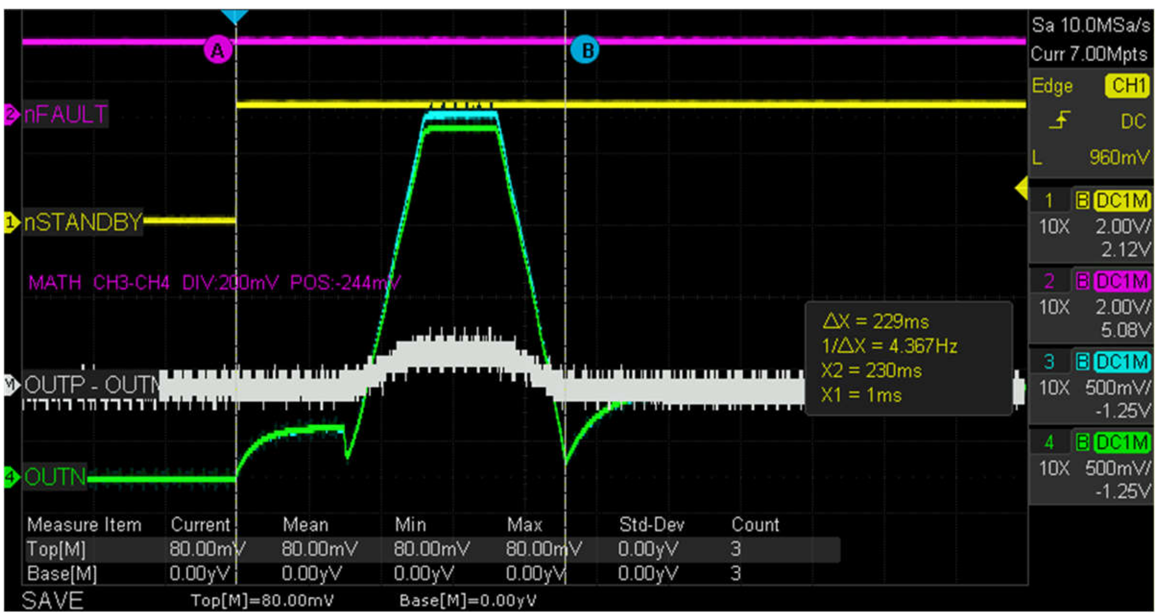

Figure 2-2. Oscilloscope Waveform for Normal Operation Across an 8Ω load

Figure 2-3 shows a waveform of the diagnostics sequence when an open load fault is present. Observe that the diagnostics sequence begins upon de-assertion of $\overline{\text{STANDBY}}$ and the sequence takes ~428ms to complete, with the *check* phase lasting 250ms. The differential voltage is observed to be 5.6V, which equates to 560Ω and exceeds the open-circuit detection threshold specified in the datasheet. The $\overline{\text{FAULT}}$ pin remains de-asserted the entire duration of the sequence.

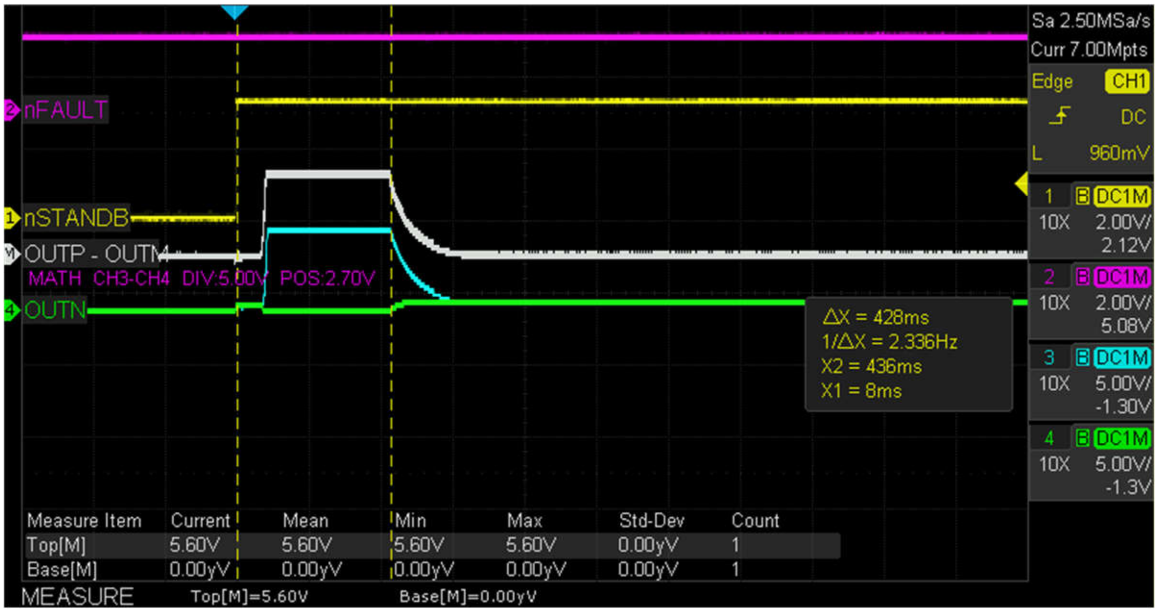

Figure 2-3. Oscilloscope Waveform for an Open-Load Condition

Figure 2-4, Figure 2-5, and Figure 2-6 show the waveforms for shorted load, speaker wire short-to-GND, and speaker wire short-to-power, respectively. In all three of the waveforms, observe that the initial diagnostics sequence begins upon de-assertion of $\overline{\text{STANDBY}}$, and each round of diagnostics takes approximatley 428ms to complete. Upon completion of the first diagnostic sequence, $\overline{\text{FAULT}}$ is asserted, and remains asserted due to the persistence of the fault. The fault sequence repeats indefinitely as long as the fault remains present.

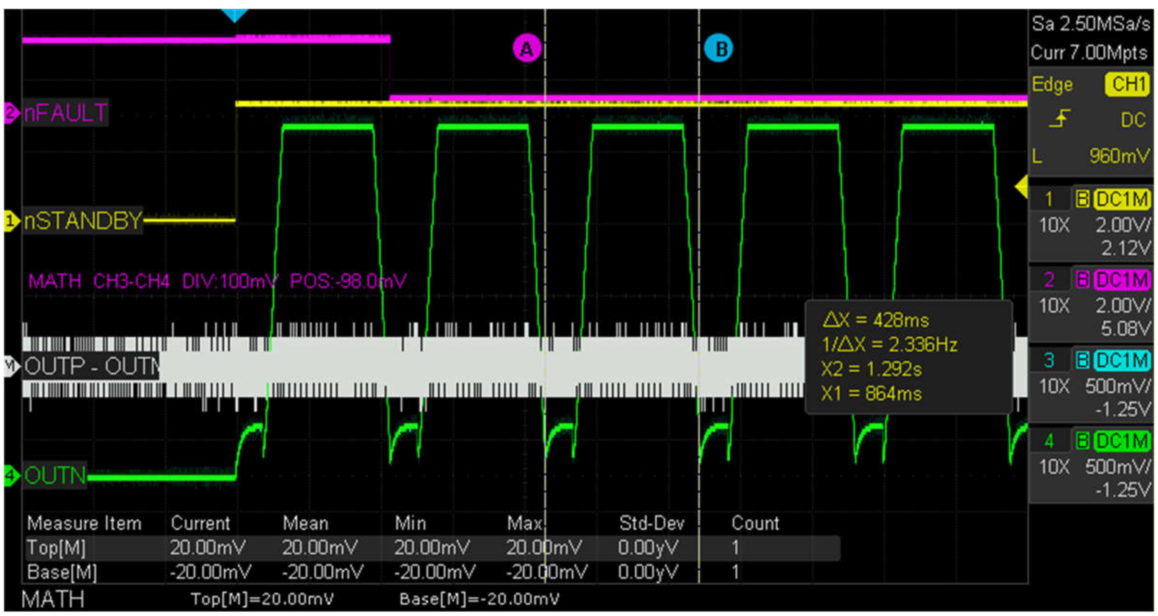

Figure 2-4. Oscilloscope Waveform for a Shorted-Load Condition

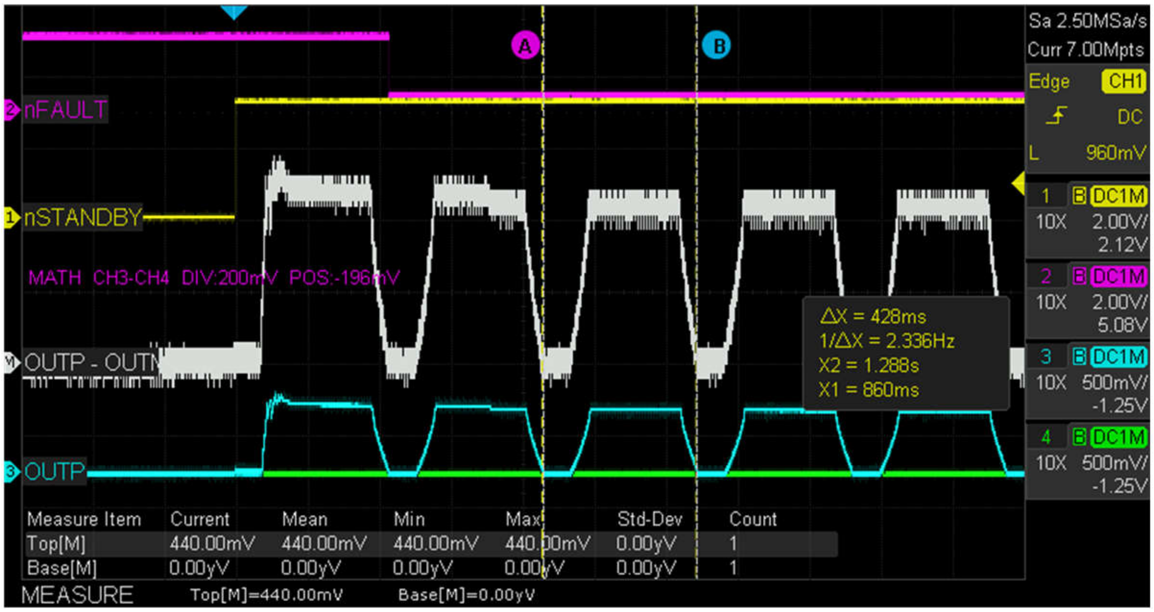

Figure 2-5. Oscilloscope Waveform for OUTN Shorted to Ground

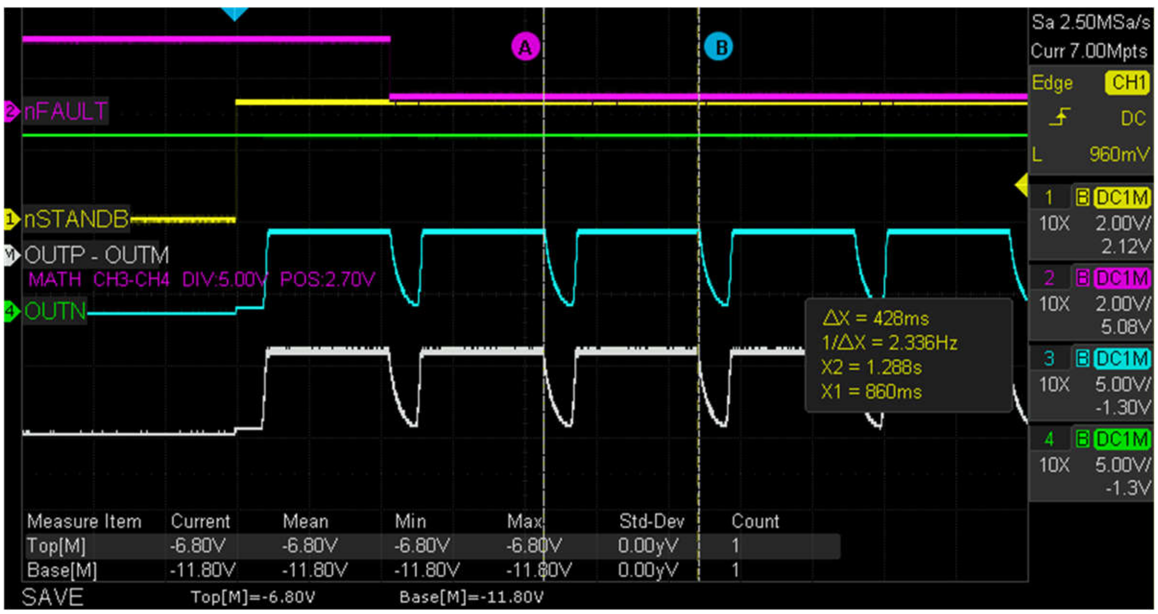

Figure 2-6. Oscilloscope Waveform for OUTN Shorted to PVDD

2.5 Troubleshooting Load Diagnostics Through Software

The PurePath Console 3 (PPC3) GUI, when paired with the TAS5431Q1EVM, allows the user to easily monitor device status including load diagnostic faults. The *Device Monitor & Control* tab provides two options for monitoring device status: *Live* and *Latched*. *Live* mode continuously tracks the diagnostic status via I^2C. When using this mode, the status register is polled every ~510 ms and the device's status is continuously output to the GUI. Alternatively, one can also use *Latched* mode to capture one-time status on demand. Figure 2-7shows a snapshot of the PPC3 GUI output in *Live* mode for a device that is continuously running Load Diagnostics due to a persistent shorted-load fault.

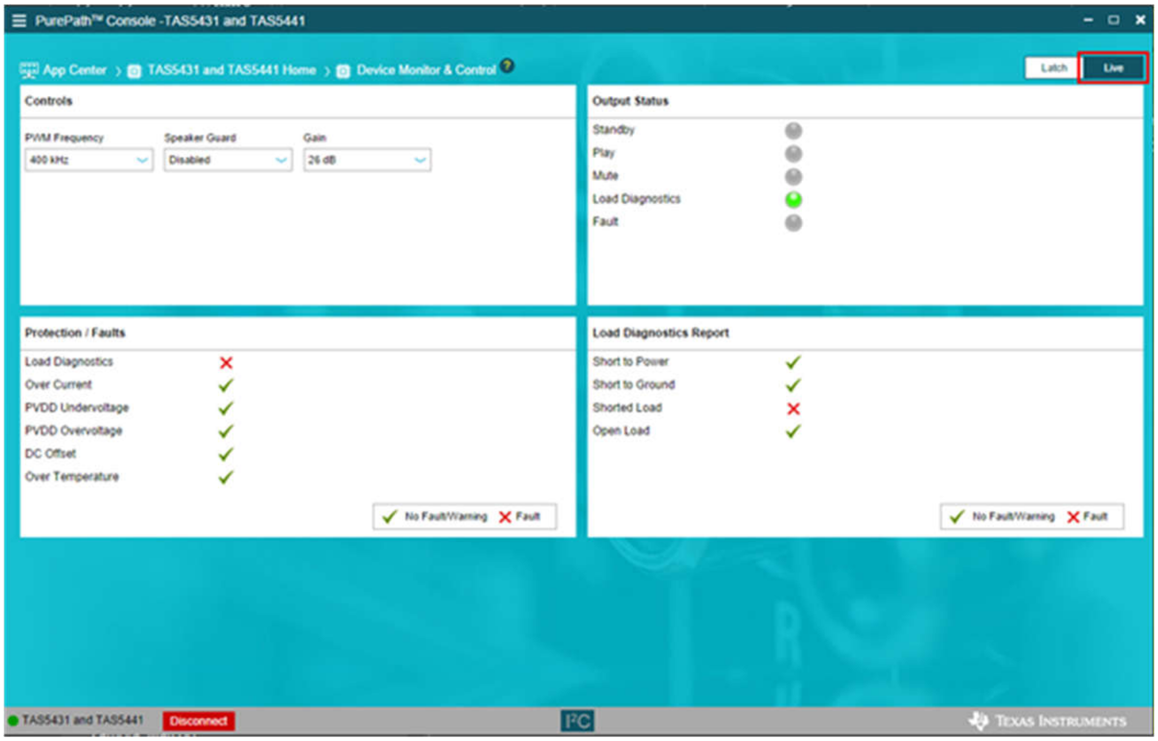

Figure 2-7. PurePath Console 3 *Device Monitor and Control Window Live* Status With Shorted-Load Fault

A similar approach can be taken on an ECU and/or vehicle containing TAS5431-Q1. Utilizing the system's micro-processor, the TAS5431-Q1 fault registers can be polled either periodically or on demand via I^2C to determine the state of the device and the load. This can be valuable for validating wiring and speaker integrity during prototype testing and system-level diagnostics.

2.6 Application-Level Considerations

To implement robust fault detection and performance in the vehicle, the system integrator must take into consideration the expected behavior of the load diagnostic features of TAS5431-Q1.

System firmware must account for the duration of load diagnostics before enabling audio after exiting standby. As demonstrated for the nominal case, load diagnostics is expected to complete in aoproximatrely 229ms. However, in the case of an intermittent fault (for example, a trunk slamming and introducing a temporary external vibration of the speakers) it is possible that a single cycle of the diagnostic sequence takes up to ~429ms. If audio is enabled prior to the completion of load diagnostics, it is possible the output will be truncated and/or a pop will be introduced upon exiting load diagnostics.

It is best practice to tie the TAS5431-Q1 $\overline{\text{FAULT}}$ pin to an I/O of the system micro-processor. In doing so, the system firmware can be configured to continuously monitor that I/O pin as a form of fault detection. Upon detecting the assertion of $\overline{\text{FAULT}}$, the system micro-processor can be configured to poll the TAS5431-Q1 fault registers through I^2C. Note that the open-load fault does not trigger an assertion of $\overline{\text{FAULT}}$.

Some system integrators can choose to poll the TAS5431-Q1 status registers at fixed intervals, and this can be beneficial to understand the state of the load. If the system requires detection of an open load condition, polling allows this to be detected given that fault mechanism does not assert the $\overline{\text{FAULT}}$ pin. Some applications may choose to poll the fault status registers after exiting standby and prior to enabling audio, to ensure that the device is no longer performing load diagnostics and no speaker faults have been reported. Additionally, some applications will poll the status registers and set a Diagnostic Trouble Code (DTC) if a fault is present for a fixed number of sequential status reads. Exact implementation of fault polling and reporting depends on the system requirements and must be implemented at the discretion of the system integrator.

Lastly, it is important that the system integrator is mindful of the output capacitance between the OUTx pins and GND, and designs the system in accordance with the Recommended Operating Conditions as described in the TAS5431-Q1 datasheet. Failure to do so can cause the load diagnostic check phase to repeat up to five times in an otherwise fault-free setup.

3 Summary

The TAS5431-Q1 Class D amplifier integrates load diagnostics capabilities to detect four common wiring and load faults. The information in this application note enables an automotive engineer or system integrator to effectively leverage these capabilities in the application, improving overall system robustness.

4 References

1. Texas Instruments, *TAS5431-Q1 8-W Mono Automotive Digital-audio Amplifier with Load Dump and I2C Diagnostics*, datasheet.