Application Note

MSPM0 VCORE Voltage Monitoring Recommendations

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ABSTRACT

This application note provides recommendations for external-voltage-monitoring designs for the MSPM0's VCORE and VDD pins. The application note discusses the background of the MSPM0's VCORE and the different methods for VCORE voltage monitoring.

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Trademarks

1 Introduction to Functional Safety Voltage Monitoring requirements for MSPM0

The VCORE signal is an output voltage tied to the core regulator/internal LDO within the MSPM0's PMU. It can be monitored to verify that the MSPM0 core voltage remains within the correct operating limits, ensuring proper device functionality. Furthermore, any VCORE monitoring block is considered external to the MCU; therefore, the FIT rate of the external circuit will need to be sourced from the respective FMEDA document, if one is available.

The PMU module has an internal set of thresholds that ensure the device's power is within expected operating conditions, as stated in each MSPM0's datasheet. This set of thresholds configures a different voltage-level monitor to ensure the device meets power requirements for proper operation. The different thresholds can be used to configure the device to perform specific actions when triggered. For more information, please refer to the PMU section of the Technical Reference Manual for the MSPM0 the application uses (e.g., PMU section in the MSPM0G family).

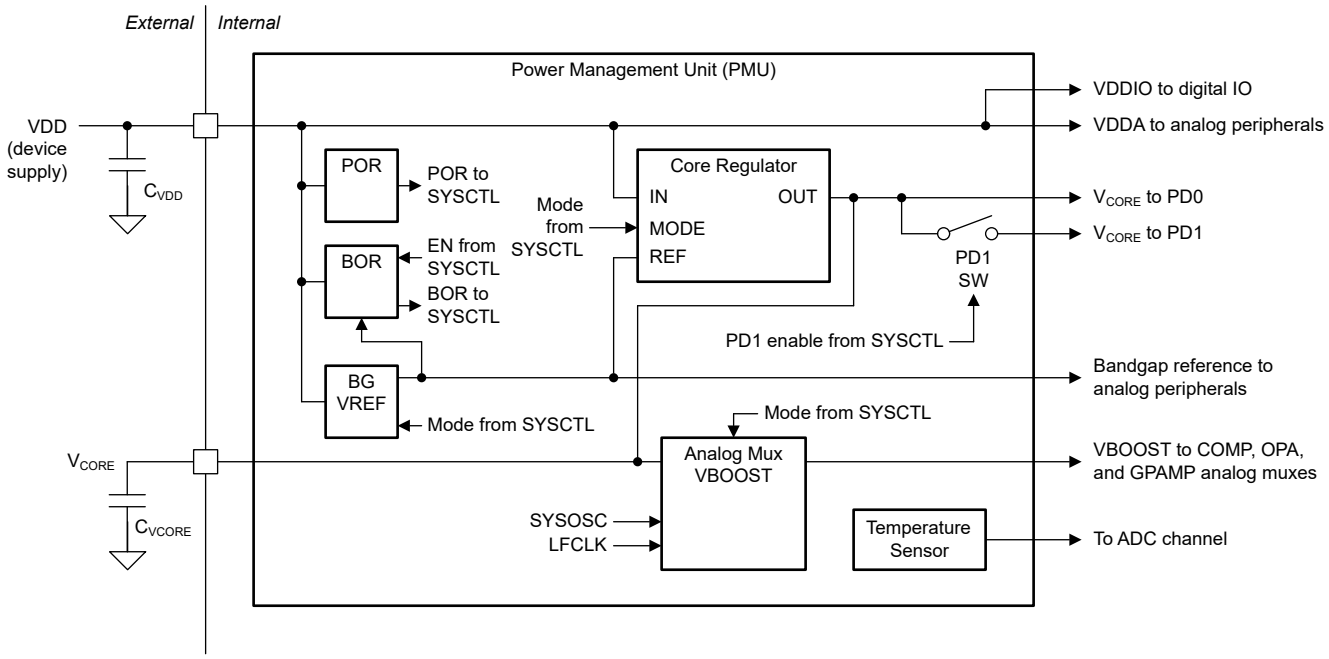


Figure 1-1. MSPM0Gxx PMU Block Diagram

The list below shows the current MSPM0 devices that have a VCORE pin and are/will be FuSa Compliant certified:

1. MSPM0LX22X
2. MPSM0GX51X & MSPM0G32XX
3. MSPM0G150X & MSPM0G3X0X
4. MSPM0L2116/7 & MSPM0L1126/7

The PMU does not monitor VDD overvoltage in the MSPM0. VDD monitoring is a requirement assumed to be covered at the system level; i.e., this Safety Mechanism is expected to be implemented externally. For more information on the specific test cases and considerations required for the MSPM0 to achieve Functional Safety compliance, please refer to the Functional Safety Manual for your respective MSPM0 device (see the table below). Nevertheless, this application note provides a recommended dedicated approach for monitoring VDD.

Table 1-1. MSPM0 Safety Manuals

Devices	Functional Safety Manual
MSPM0G3X0X	Functional Safety Manual for MSPM0G3x0x-Q1
MSPM0GX51X	Functional Safety Manual for MSPM0Gx51x
MSPM0LX22X	Functional Safety Manual for MSPM0Lx22x-Q1

2 Functional Safety External Voltage Monitoring Recommendations

2.1 MSPM0 VCORE and VDD recommended requirements

As mentioned in the safety mechanism regarding VCORE monitoring for the MSPM0 devices—using the MSPM0G3X0X and MSPM0GX51X devices as reference for the specific values used in this section —the following criteria must be fulfilled for the VCORE pin:

- The voltage on the pin must be continuously monitored so that the system can detect both undervoltage (UV) and overvoltage (OV) conditions. The general considerations are as follows:
  - The VCORE pin can source up to 100 µA when operating in RUN or SLEEP mode (including while the device is held in reset). In STOP and STANDBY modes, the VCORE pin can source up to 20 µA. In SHUTDOWN mode the device is inactive, so no current can be sourced.
  - The VCORE pin cannot sink any current in any mode or at any point during the MCU's operation.

The following VCORE values can be used as reference:

Table 2-1. VCORE Voltage Requirement Tables

VCORE recommended limits	Min	Typ	Max	Units	Recommendation background
VCORE LDO Output Valid Limits	1.3	1.35	1.39	V	The limits given are intended to prevent triggering any OV or UV condition as long as VCORE remains within these limits.
VCORE Absolute	1.27		1.42	V	The limits given are intended to not be violated; otherwise, the device will go out of spec.
UV Threshold	1.27	1.285	1.3	V	Allows for a margin of +/-1.17%
OV Threshold	1.39	1.405	1.42	V	Allows for a margin of +/-1.07%

Note

The VCORE pin is physically present to provide access for a tank capacitor, which is part of the VCORE LDO circuit used to stabilize the VCORE voltage supplied to the internal circuits.

For system design purposes, the MSPM0 general guideline on VDD overvoltage is that the supply voltage should not exceed the recommended VDD maximum value (in this case, 3.6 V). Furthermore, the FTTI specifications for system fault detection and reaction must be defined by the designer, as they are dependent on the application.

The actions to take when a fault occurs depend on the application requirements. As mentioned in the specific device's safety manual, the actions that can be taken in the event of a fault range from communicating the error to a host CPU and allowing the system to take an appropriate action or resetting the MSPM0 device to ensure a "safe state" (in this context, this refers to setting the device to a state similar to reset, where pins and certain behaviors are set to a specific, known state).

Since a fault in VCORE can affect reset conditions in the MSPM0 device, it is required to consider only Power-On Reset (POR) as the default reset level the MSPM0 must undergo to be considered "reset." Furthermore, the voltage level at which the device is considered "powered off" must be at or below 0.9 V — the POR− device threshold — and this voltage level must be sustained for a period equal to or greater than 100 µs. Additionally, some of the potential failure modes resulting from a VCORE fault include the following:

- Unkown state pins
- Loss of the NRST mechanism
- Loss of SRAM contents
- Incomplete ongoing flash program/erase operations

Assuming the NRST is still valid (i.e. a VCORE fault is not ongoing), the following bench tested current consumption values can be used as a reference when the device is powered at the specified VDD levels while in the device is hold in reset:

- Less than 20µA at VDD < 0.9V
- Less than 30µA at VDD < 1.3V
- Less than 700µA at VDD < 1.6V

Note

The currents above were measured while an MSPM0G3519 ran an empty project. Current values may vary depending on the application.

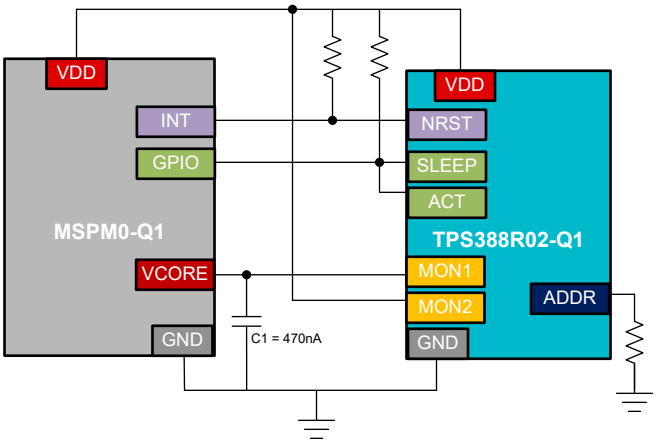
2.2 Voltage Monitor Approaches

2.2.1 Voltage Supervisor - Multichannel Channel

A voltage supervisor is a device that monitors or “supervises” a voltage rail within a system. When the monitored voltage rail, in our case, the VDD and VCore rails, falls below or rises above a predetermined threshold voltage, the supervisor will assert a signal that can enable, disable, or reset another device.

In the figure below, we show a system that uses a TPS388RX-Q1 to monitor the VCORE pin in the MSPM0.

Figure 2-1. 2 Channel Voltage Supervisor for VDD and VCORE Monitoring



The TPS388RX-Q1 is a 2-to-8-channel window supervisor IC. This high-accuracy multichannel voltage supervisor is designed for systems that operate on low-voltage supply rails and have narrow supply tolerance margins.

For monitoring the MSPM0 VDD and VCORE rails, the 2-channel variant **TPS388R02M01RTERQ1 (Preview)** is available for sampling by contacting TI directly. Please note that this device has not yet been released to market yet.

Table 2-2. TPS388R02M01RTERQ1 Device Setting

Device	MON1	MON2	MON3	MON4	MON5	MON6	MON7	MON8
TPS388R02M01RTERQ1 (Preview)	UVHF: 1.285V	UVHF: N/A	N/A	N/A	N/A	N/A	N/A	N/A
	OVHF: 1.405	OVHF:3.58V						

Key Advantages

- **No External Resistors Required:** The TPS388R02M01RTERQ1 sets overvoltage and undervoltage reset thresholds internally, eliminating the need for external resistors. This optimizes overall accuracy, reduces cost and board space, and improves reliability in safety critical systems and making it fully capable of meeting MSPM0 VCORE and VDD recommended requirements.
- **Industry-Leading Threshold and Hysteresis Accuracy:** The TPS388RX-Q1 delivers ±7.5 mV threshold accuracy across the full –40°C to +125°C temperature range. The TPS388RX-Q1 enables tight margin monitoring of low voltage supply rails. It's critical for microcontrollers like the MSPM0 that operate with narrow voltage tolerances.
- **Low Current Consuption at MONx channel**: Each MON channel offers different scaling options; to meet the VCORE rail sinking current requirement, MON2 is configured at ×1 scale.

- **Integrated Glitch Immunity & Noise Filtering:**Internal glitch immunity and noise filters eliminate the need for external RC components, preventing false resets caused by power transients. A per-channel debounce filter is available and is pre-configured to **51.2 µs** for the TPS388R02M01RTERQ1.

Please see the worst case analysis for VDD and VCORE monitoring in below:

VCore Abs Max Limit	MON2 Threshold Settings for TPS388R02M01RTERQ1	Worst case analysis
Undervoltage (UV) Limit=1.27V	UV threshold (UV_HF)=1.285V	UV_HF_Min= 1.285V-7.5mV = 1.278V
Overvotlage (OV) Limit=1.42	OV threshold (OV_HF)=1.405V	OV_HF_Max= 1.405V + 7.5mV= 1.413V

For ASIL-B level requirements, the**TPS388C0-Q1**, a multichannel device integrating a window monitor reset IC with a window watchdog is also recommended as a complementary solution. Both the TPS388RX-Q1 and TPS388C0-Q1 share the same package and include comprehensive **Functional Safety Compliance documentation**, helping designers determine the optimal implementation approach for their systems.

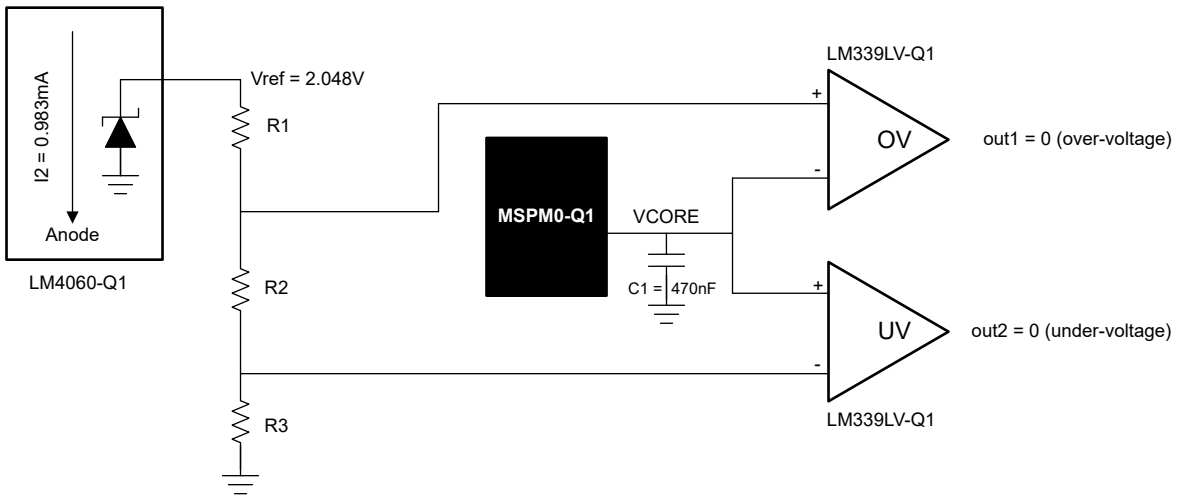
Device	Safety document
TPS388RX-Q1	Request now
TPS388C0-Q1	Request now

2.2.2 Discrete Approach

Discrete designs are often selected for straightforward, cost-effective solutions to voltage monitoring.

The figure below shows a system that uses a series of resistor dividers, comparators, and a precision shunt voltage reference to detect over- and under-voltage conditions on the VCORE pin of the MSPM0.

Figure 2-2. Discrete VCORE Monitoring



Note

Each comparator's output could require a pull-up resistor depending on the system's requirements.

The design uses a precision voltage reference to generate around 2V of reference, which is then applied to the resistor ladder. The resistor ladder consists of a series of resistors whose ratio determines the voltage input to the comparator. The comparators are configured as window comparators to detect overvoltage and undervoltage conditions in the system.

The selected device meets the MSPM0 requirements specified in the MSPM0 VCORE and VDD recommended requirements.

The LM4060-Q1 is the recommended precision shunt voltage reference due to its ±0.05% (A grade) accuracy and a detection time of less than 1 µs. Since the LM4060-Q1 continuously draws input current, the MSPM0 is assumed to not enter a low-power mode. Note that additional mechanisms may be required to sink the current in order to match the selected MSPM0 low-power mode.

The Threshold Generator using the series resistance is used as a simple way to set the limits in both comparators. The following represents the limits set by the series resistors:

$$OV\ Threshold = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times VREF \quad (1)$$

$$UV\ Threshold = \frac{R_3}{R_1 + R_2 + R_3} \times VREF \quad (2)$$

The LM339LV-Q1 is the recommended comparator because it offers low voltage offset and input bias current across the system ranges, doesn't violate the VCM ranges, and has input bias current less than the recommended value for the VCORE pin.

The user can calculate the worst-case scenario to evaluate a system’s reliability. The following is an example of such an evaluation using a combination of maximum worst-case error and RMS additions. The component errors are considered/listed as the following:

1. Assume the system uses resistors with the characteristics shown below. The following factors can be considered to determine the total error for this component:
   a. Initial Resistor variation

b. Temperature coefficient of resistance in ppm/°C

$$Resistor\ Temp\ Error\ \% = \frac{Temp\ Coefficient\ of\ Resistance}{1000000} \times Temp\ variation \times 100\% \quad (3)$$

c. Resistor Aging Error

The total resistor error (using percentage values) can be calculated with an RMS addition:

Total Resistor Error

$$Total\ Resistor\ Error = \sqrt{Initial\ Resistor\ variation^2 + Resistor\ Temp\ error^2 + Resistor\ Aging\ error^2} \quad (4)$$

2. Using the Shunt Voltage Reference specifications, the following factors can be considered to find the total error in this component:
   a. VREF Reverse breakdown voltage accuracy
   b. Output voltage temperature coefficient in ppm/°C (divide by one million to get rid of the ppm). Assume a temperature variation of about 100 °C, and use the following formula to calculate the VREF temperature error:

$$VREF\ Temp\ Error = \frac{Output\ voltage\ temp\ coefficient}{1000000} \times Temp\ variation \times 100\% \quad (5)$$

   c. Long-term stability coefficient in ppm, and use the following formula to calculate the VREF long-term reliability error:

$$VREF\ Longterm\ stability\ Error = \frac{Longterm\ stability\ coefficient}{1000000} \times 100\% \quad (6)$$

The total VREF error (using percentage values) is obtained by RMS addition:

$$Total\ VREF\ Error = \sqrt{VREF\ Reverse\ breakdown\ volt\ error^2 + VREF\ Temp\ Error^2 + VREF\ Longterm\ stability\ Error^2} \quad (7)$$

3. Using the Comparator specifications, the following factors can be considered to find the total error in this component:
   a. Input Offset Voltage in volts. The following formula can be used to calculate the Comparator Input Offset error:

$$Comparator\ Input\ Offset\ Error = \frac{Input\ Offset\ voltage}{UV\ Threshold_{typ}} \times 100\% \quad (8)$$

Voltage offset only is considered here as this is the dominant error in the comparator.

After calculating the individual errors, determine the variation values for R_1, R_2, and R_3 (the resistor ladder) and for the VREF output. Assuming all resistors have an internal error of 1%, a temperature variance of 25 ppm/°C, and an aging error of 0.15%, the table below shows the resulting values for each component that affect the resistor-ladder thresholds for VCORE.

Table 2-3. Resistor and VREF Voltage in values with errors

Components	Range	Values	Component Error (%)
R_1 (Ω)	Min	62145.854	1.042
	Typ	62800	
	Max	63454.146	
R_2 (Ω)	Min	11578.129	1.042
	Typ	11700	
	Max	11821.871	

Table 2-3. Resistor and VREF Voltage in values with errors (continued)

Components	Range	Values	Component Error (%)
R_3 (Ω)	Min	124192.750	1.042
	Typ	125500	
	Max	126807.250	
VREF Output Voltage (V)	Min	2.044	0.206
	Typ	2.048	
	Max	2.052	

After obtaining the variations of the individual components, the over-voltage and under-voltage values—and their deviation from the typical expected value—can be determined using the following formula:

$$OV\ Real\ Threshold_{(min,\ typ,\ \max)} = \frac{R2_{(min,\ typ,\ \max)} + R3_{(min,\ typ,\ \max)}}{R1_{(max,\ typ,\ \min)} + R2_{(min,\ typ,\ \max)} + R3_{(min,\ typ,\ \max)}} \times VREF_{(min,\ typ,\ max)} \quad (9)$$

$$UV\ Real\ Threshold_{(min,\ typ,\ \max)} = \frac{R3_{(min,\ typ,\ \max)}}{R1_{(max,\ typ,\ \min)} + R2_{(max,\ typ,\ \min)} + R3_{(min,\ typ,\ \max)}} \times VREF_{(min,\ typ,\ max)} \quad (10)$$

Table 2-4. OV and UV Limits Values with Errors

Limits	Range	Min	Error (%)
OV	Min	1.39282	-0.87
	Typ	1.40493	-0.01
	Max	1.41700	0.85
UV	Min	1.27249	-0.97
	Typ	1.28512	0.01
	Max	1.29774	0.99

Note

Adding a 0.1 % tolerance resistor to either R_1 and R_3 will improve drastically the worst case error

Finally, the worst-case error is calculated by finding the maximum absolute error among the previously determined OV and UV values and adding the total comparator error.

$$Worst\ case\ error = (Max(|OVERE_{min}|, |OVERE_{max}|, |UVERE_{min}|, |UVERE_{max}|) + Total\ Comparator\ Error) \times 100\% \quad (11)$$

Assuming the system uses the values established earlier, the worst-case error will be approximately **±1.213 %**.

3 Summary

This application note provides the VCORE and VDD recommendations and specifications needed to evaluate how to monitor either signal in the MSPM0, while also providing two approaches to implement such monitoring.

4 References

- Texas Instruments, *MSPM0 G-Series 80MHz Microcontrollers*, technical reference manual.
- Texas Instruments, *MSPM0 L-Series 80MHz Microcontrollers*, technical reference manual.
- Texas Instruments, MSPM0G3507, product page.
- Texas Instruments, MSPM0G1507, product page.
- Texas Instruments, MSPM0G3519, product page.
- Texas Instruments, MSPM0L2228, product page.
- Texas Instruments, MSPM0L2117, product page.
- Texas Instruments, MSPM0G3218-Q1, product page.
- Texas Instruments, MSPM0G3519, product page.
- Texas Instruments, TPS388RX-Q1, product page.
- Texas Instruments, TPS388CX-Q1, product page.
- Texas Instruments,LM4060-Q1, product page.
- Texas Instruments, LM339LV-Q1, product page.
- Texas Instruments, *Functional Safety Manual for MSPM0G3x0x-Q1*, functional safety manual.
- Texas Instruments, *Functional Safety Manual for MSPM0Gx51x*, functional safety manual.
- Texas Instruments, *Functional Safety Manual for MSPM0Lx22x-Q1*, functional safety manual.

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