Application Note

Start-Up Behavior Analysis of TPS53689T/C9T: Bump Reduction and Integration Time Constant Dependency

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ABSTRACT

During start-up, with constant ON time (COT) controller output voltage is seen oscillating for a short while. In multiphase voltage regulator (VR) systems supplying modern processors, such bumps can over stress downstream devices, trigger false fault conditions, or impact system stability. To mitigate this phenomenon, bump reduction technique is implemented. This application note analyzes root causes of bump phenomena in power management ICs and presents practical bump reduction technique as implemented in the TPS53689T /C9T multiphase controller. Measurement results are provided to validate effectiveness of these techniques under representative operating conditions.

Table of Contents

Trademarks

1 Introduction

In high-current multiphase voltage regulator (VR) applications, stable and predictable start-up behavior is essential for reliable system operation. Modern digital controllers often include advanced start-up features, such as bump reduction, to mitigate output voltage ringing during power-up.

During system evaluation of the TPS53689T multiphase controller on a customer platform, an abnormal start-up condition was observed with bump reduction feature. Specifically, the output voltage failed to ramp up successfully, and controller reported undervoltage (UV) fault. On increasing integration low time constant, this issue was resolved.

This application paper analyzes the root cause of this behavior and demonstrates how control-loop parameter tuning—specifically the Final_INT_LOW_TC setting—can improve start-up robustness while retaining bump reduction functionality.

2 Definition of Bump in Multiphase VR Systems

Controller monitors difference between actual output voltage (V_{OUT}) and set point (VDAC) during soft-start. If the difference exceeds a predefined threshold, 50mV, all PWM are tri-stated until the control loop demands another PWM pulse. TI recommend that the Bump Reduction Function must be enabled only if there is high inrush current and large VOUT bump during soft-start.

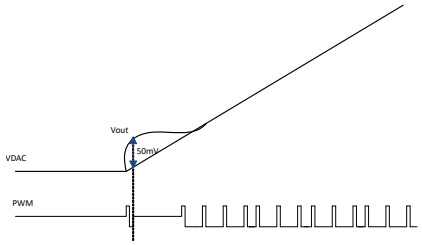


Figure 2-1. Bump Reduction Enable

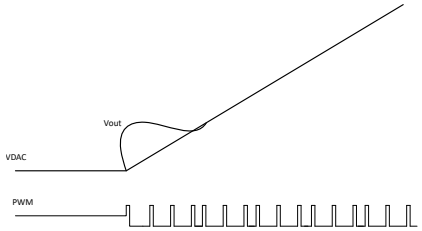


Figure 2-2. Bump Reduction Disable

Note

Output voltage waveform is just a depiction and actual behavior is a function of loop compensation, min_ton start and output power delivery network

3 System Description and Observed Error

During evaluation on the customer's board, an abnormal start-up behavior was observed. The system failed to complete the start-up sequence when the bump reduction feature was enabled (Figure 3-1). In contrast, normal start-up operation was achieved after the bump reduction feature was disabled (Figure 3-2). Under the failed start-up condition, a VOUT_UV protection event was logged by the controller.

Since the exact timing and condition of the undervoltage (UV) trigger cannot be directly identified from external measurements, an emulated controller was utilized to further investigate the event. By monitoring the internal VDAC voltage of the emulated controller and reporting its status through SMBus Alert, the occurrence of the UV trigger was successfully confirmed.

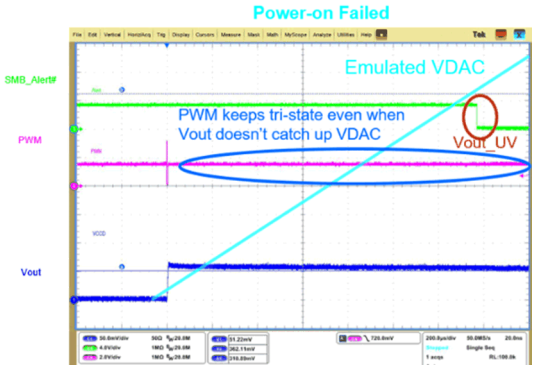


Figure 3-1. Bump Reduction Enable

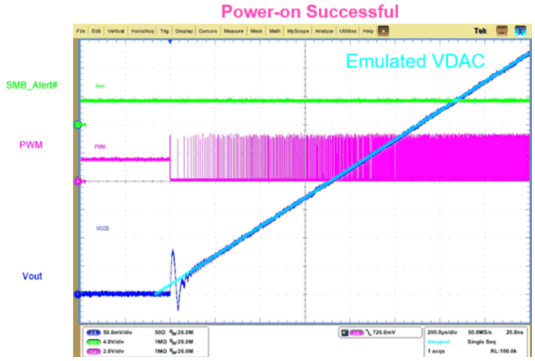


Figure 3-2. Bump Reduction Disable

As shown in Figure 3-1, the output voltage stalls after the first few PWM pulses, as the controller stops PWM pulses. The question then arises as to why the controller stops generating PWM pulses. In simulation, the issue was observed to be related to saturation (high negative value) of the controller integrator.

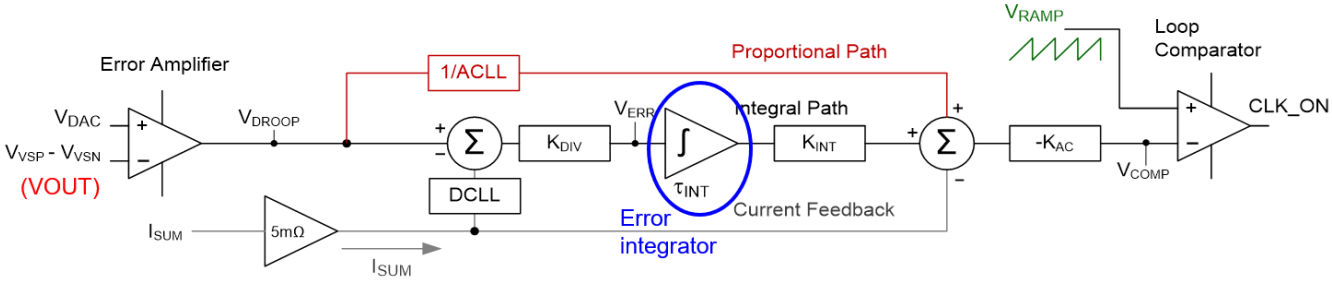


Figure 3-3. Loop Compensation Conceptual Block Diagram

Position of integrator (τ_{INT}) in the control loop is shown in Figure 3-3. In GUI, this is expressed as Int Time Constant (Figure 3-4). However, during bump reduction, a different value of τ_{INT} is used, which is stored in reg location 0xCE<14:12> (not in GUI) and denoted as Int_low_TC. The final value of the time constant, is $\tau_{INT} \times G_{INT}$ as shown in Table 3-1.

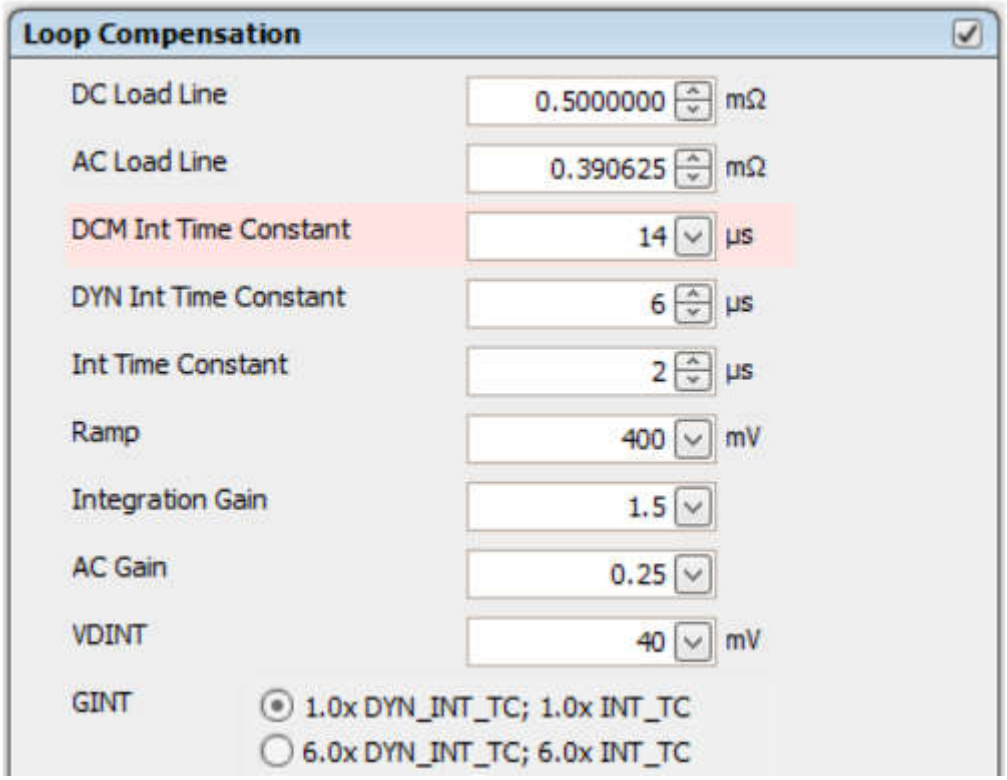


Figure 3-4. Loop Timing Parameters in Fusion GUI

Table 3-1. Effective Integration Time Constant

Board	INT_TC GUI value	INT_LOW_TC Reg name	GINT	Final INT_TC	Final INT_LOW_TC	Boot Up Successful?
1U	2us	125ns	6	12us	750ns	Yes
2U	8us	125ns	1	8us	125ns	No
2U experiment	8us	1000ns	1	8us	1000ns	Yes

4 Simulation Analysis and Sequence of Events

Integrator circuit for different modes of operation is shown in Figure 4-1, where final integration time constant is *1 / RC*. In the very beginning, integrator output, V_I is zero. The sequence of event is explained below in conjunction with simulation results (Figure 4-2).

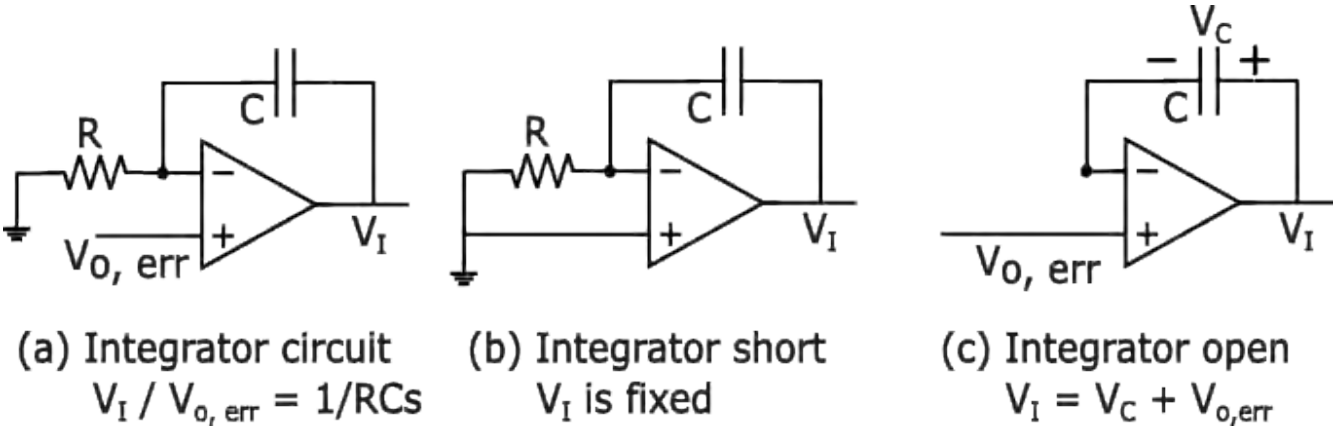
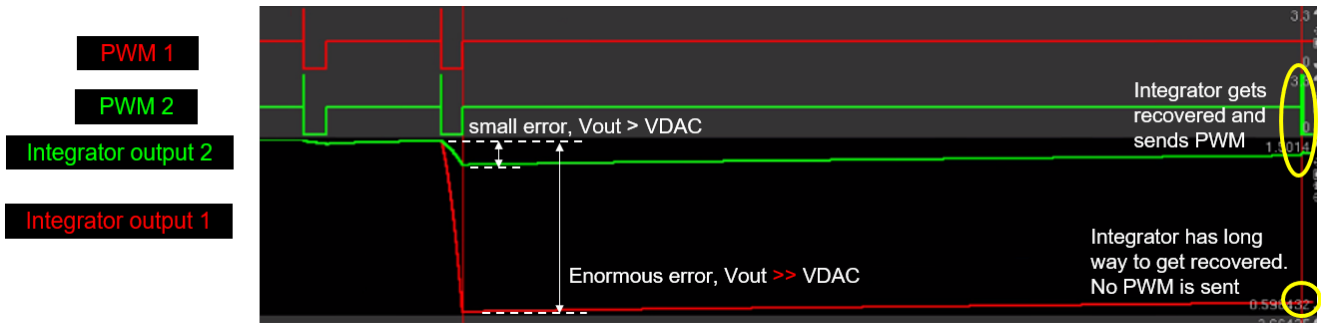


Figure 4-1. Integrator Circuit During Different Modes of Operation

1. At initial state, PWM is tri-state and Integrator is shorted as shown in Figure 4-1b. The connection remains intact for first two PWMs during boot up.
2. When first PWM comes, output bumps up. This is as per power-stage inductor and capacitor configuration. Also, Int low TC is activated. It remains active for first two PWM after tri-state mode. Note that integrator is still short.
3. When VOUT (at AVSP-AVSN) jumps above bump reduction threshold, PWM is tri-state, integrator is opened (Figure 4-1). Therefore error integration is stopped. But, integrator output moves at same rate as VOUT error (V_I = constant + $V_{o,error}$)
4. When VOUT falls below bump reduction threshold, another PWM is issued. This is second PWM, normal error integration is started.
5. Since integration time constant is low (high integration multiplier), the integrator output rapidly moves to saturation in about 200ns.
6. At this point the output has jumped up again to detect a second bump reduction event which tri-states the PWM and opens the integrator.
7. Since the integrator was in saturated condition (or extreme negative) and the integrator is opened, the next ON pulse does not come for a very long time and PWM remains tri-state waiting for next ON pulse.
8. This leads to UV fault as the DAC keeps going up without PWM.

Simulation results also show that Final INT_LOW_TC being 1000ns slows down the integration rate of the internal error integrator during the start-up phase, making the integrator less prone to saturation when the output voltage rise is temporarily limited. Under this condition, the controller is able to continue generating PWM pulses, allowing the output voltage to ramp up smoothly. This difference in integrator behavior provides a clear explanation for the divergent start-up behavior observed between the two board designs.

These results indicate that final INT_LOW_TC plays a critical role in determining start-up stability when bump reduction is enabled.



Waveform 1 (Red) is bump reduction enabled with (Final INT_LOW_TC) = 125ns

Waveform 2 (Green) is bump reduction enabled with (Final INT_LOW_TC) = 1000ns

Figure 4-2. Simulation Results with Different Final INT_LOW_TC

5 Undervoltage Fault Trigger Identification

During the failed start-up condition, a VOUT_UV fault was recorded by the controller. However, the exact timing of the UV trigger could not be directly determined from external measurements alone.

To address this, an emulated controller was used to monitor the internal VDAC voltage. The fault status was reported through SMBus Alert#, allowing the timing of the undervoltage event to be identified. In Figure 3-1, SMBus_ALERT# asserts at VDAC at approximately 400mV. This is 350mV higher than VOUT, 50mV.

This method confirmed that the UV fault was triggered after the output voltage stalled, consistent with integrator saturation preventing further PWM activity.

6 Measurement Validation

The analysis and simulation results were further validated through bench testing. As shown in Figure 6-1, when final INT_LOW_TC is set to 125ns, the output voltage fails to start up properly. When final INT_LOW_TC is increased to 1000ns, as shown in Figure 6-2, the output voltage is able to start up successfully. Although the internal integrator requires a calibration period during the initial start-up phase, the output voltage does not fall below the UV threshold, thereby preventing the undervoltage protection from being triggered and allowing the output voltage to ramp up normally.

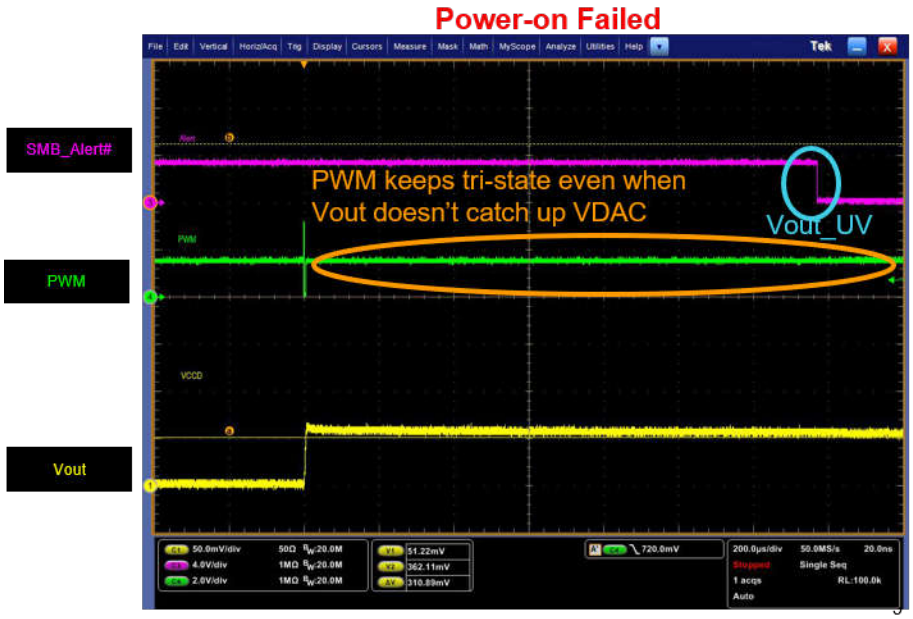


Figure 6-1. Bump Reduction Enable and Final INT_LOW_TC = 125ns

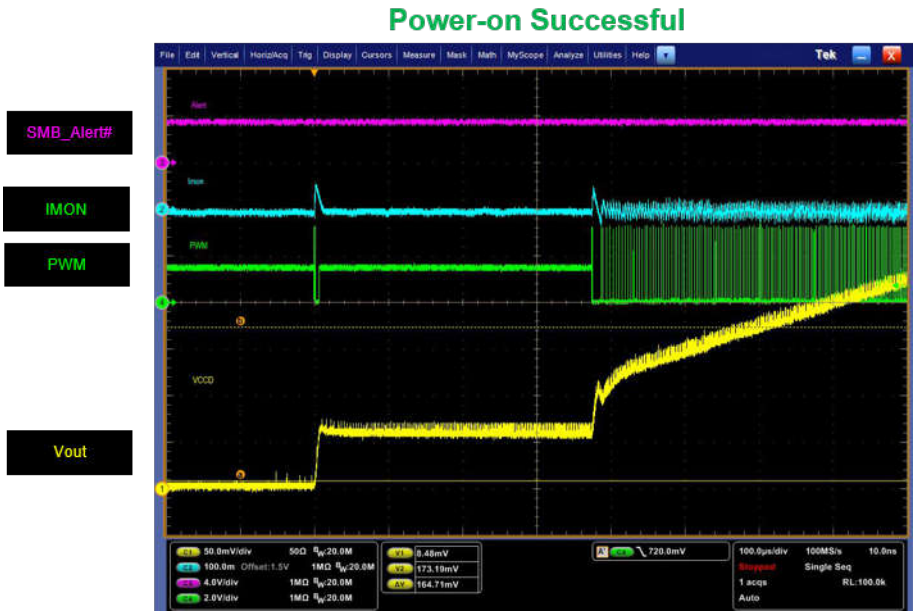


Figure 6-2. Bump Reduction Enable and Final INT_LOW_TC = 1000ns

7 Summary

This application note demonstrates that start-up instability observed on TPS53689T-based designs with bump reduction enabled can be attributed to internal error integrator saturation caused by an overly aggressive Final_INT_LOW_TC setting.

Through control-loop analysis, simulation, and bench validation, this is shown that increasing Final_INT_LOW_TC effectively prevents integrator saturation, avoids unintended undervoltage fault triggering, and enables reliable start-up behavior.

Proper tuning of control-loop parameters is therefore essential when enabling bump reduction in high-current multiphase VR applications.

8 References

1. Texas Instruments, TPS53689T Dual- channel (N + M ≤ 8 phase) D-CAP+, Step-down, Multiphase Controllers with TLVR support, PMBus and VR14 SVID Interfaces, datasheet.
2. Texas Instruments, TPS536C9T Dual- channel (N + M ≤ 12 phase) D-CAP+, Step-down, Multiphase Controllers with TLVR support, PMBus and VR14 SVID Interfaces, datasheet.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2026) to Revision A (August 2026)	Page
• Updated the spelling of "startup" to "start-up" throughout the document	0
• Updated formatting of τ_{INT} in text in *System Description and Observed Error* section	3
• Updated formatting of *1 / RC* in text in *Simulation Analysis and Sequence of Events* section	5

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Last updated 10/2025