Application Note

TJA1103 to DP83TC1103x-Q1 Rollover Guide

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Abstract

The DP83TC1103x-Q1 PHY is designed to be pin to pin compatible with TJA1103. This document serves as a reference for changing a TJA1103 design to a DP83TC1103x-Q1 design. In many cases, the same board design used for TJA1103 can be used to support DP83TC1103x-Q1. However, it may be necessary to adjust passive components supporting the PHY.

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1 Introduction

The DP83TC1103A-Q1 PHY supports RGMII, RMII, MII, and is designed to be pin to pin compatible with TJA1103A. Similarly, the DP83TC1103B-Q1 PHY supports SGMII and is designed to be pin to pin compatible with TJA1103B. This application note compares pins between the DP83TC1103x-Q1 and TJA1103 devices, highlights pin provisions, and serves as a reference for designing with the DP83TC1103x-Q1 PHY.

GENERIC PART NUMBER	SUPPORTED MAC INTERFACES
DP83TC1103A-Q1	MII, RMII, RGMII
DP83TC1103B-Q1	SGMII

2 Common Features and Differences

The DP83TC1103x-Q1 and TJA1103 offer similar functionality in the same package, allowing for most board designs to support either PHY. The following table highlights shared features and differences between these PHYs.

Table 2-1. Common Features and Differences

PARAMETER	DP83TC1103x-Q1 AND TJA1103 COMMON FEATURES	DP83TC1103x-Q1 AND TJA1103 DIFFERENCES
Package	36-WQFN 6mm × 6mm 0.5mm pitch Similar DAP size	N/A
Pinout	Keys pins including MDI, xMII, common supplies, and clocks.	DP83TC1103x-Q1 may have no connect (NC) pins in place of unused supply pins, and reserved pins in place of GPIO.
Power rails	Single supply 3.3V mode.	2.5V supply mode is not supported on DP83TC1103x-Q1. Individual supply (TI dual supply) modes are not supported.
Interfaces	DP83TC1103A-Q1 / TJA1103A: • RGMII • RMII-clkmode, rev-RMII mode • MII DP83TC1103B-Q1 / TJA1103B: • SGMII	DP83TC1103A-Q1 / TJA1103A:RMII mode
Straps	Selective common PHY addresses supported. Selective strap functions.	A limited set of TJA1103 strap configurations are supported. Software configuration may be required on DP83TC1103x-Q1 to reach the same configuration as TJA1103. See Strap Configuration for additional details.
Features	TC-10 802.1AS	DP83TC1103x-Q1 does not support JTAG

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3 Pinout Comparison and Pin Provisions

3.1 DP83TC1103A-Q1 Pinout Comparison and Pin Provisions

While DP83TC1103A-Q1 is designed to be pin to pin compatible with TJA1103A, there are some minor variations in the pinouts between devices. This is illustrated in the following figure.

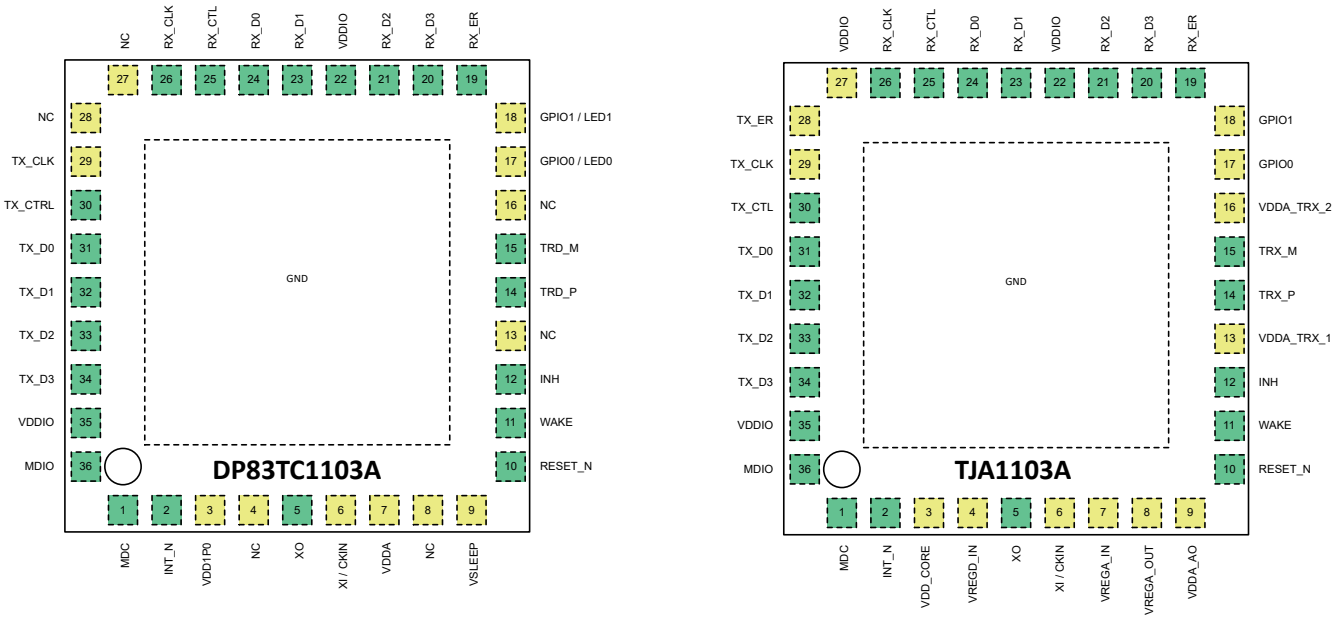


Figure 3-1. DP83TC1103A-Q1 vs TJA1103A Pinout

LEGEND	
Pins with same core functionality	Pins may have different function or may require schematic level provision. See Table 3-1

Pin differences between DP83TC1103A-Q1 and TJA1103A are highlighted in Table 3-1. The provisions in this table are the minimum required for functional design. More thorough provisioning is present in the DP83TC1103A-Q1 Common Schematic.

Table 3-1. DP83TC1103A-Q1 vs TJA1103A Pinout Differences

PIN NO.	DP83TC1103A-Q1 PIN NAME	TJA1103A PIN NAME	PROVISION REQUIRED	NOTES
3	VDD1P0	VDD_CORE	None	DP83TC1103A-Q1 uses for internal LDO decoupling capacitor. Depopulate any connections to external supply. See Power Supply Recommendations.
4	NC	VREGD_IN	None	Voltage regulator for the digital domain is internally connected on die for DP83TC1103x-Q1. No external connection is required.
5	XO	XO	Optional	Series resistor can be provisioned for tuning crystal power.
6	XI	XI	Optional	TI recommends 100Ω series resistor for optimum EMC performance when using crystal.
7	VDDA	VREGA	None	3.3V power rail for both devices. See Power Supply Recommendations..

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Table 3-1. DP83TC1103A-Q1 vs TJA1103A Pinout Differences (continued)

PIN NO.	DP83TC1103A-Q1 PIN NAME	TJA1103A PIN NAME	PROVISION REQUIRED	NOTES
8	NC	VREGA_OUT	None	DP83TC1103A-Q1 package NC.
9	VSLEEP	VDDA_AO	None	Always on power rail for TC-10. See Power Supply Recommendations..
13	NC	VDDA_TRX_1	None	DP83TC1103A-Q1 package NC.
16	NC	VDDA_TRX_2	None	DP83TC1103A-Q1 package NC.
17	GPIO0 / LED0	GPIO0	Optional	Register configuration may be needed for intended LED functionality.
18	GPIO1 / LED1	GPIO1	Optional	
27	NC	VDDIO	None	DP83TC1103A-Q1 package NC.
28	NC	TX_ER	None	DP83TC1103A-Q1 package NC.
29	TX_CLK	TX_CLK	Yes	In RMII-clkmode, TJA1103A recieves 50MHz RMII clock input on TX_CLK. In DP83TC1103A-Q1 RMII Follower Mode (comparable to RMII-clkmode), 50MHz RMII clock input should be received on XI. Provisions should be added to route 50MHz clock accordingly if RMII Follower Mode is used.

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3.2 DP83TC1103B-Q1 Pinout Comparison and Pin Provisions

While DP83TC1103B-Q1 is designed to be pin to pin compatible with TJA1103B, there are some variations in the pinouts between devices. This is illustrated in the following figure.

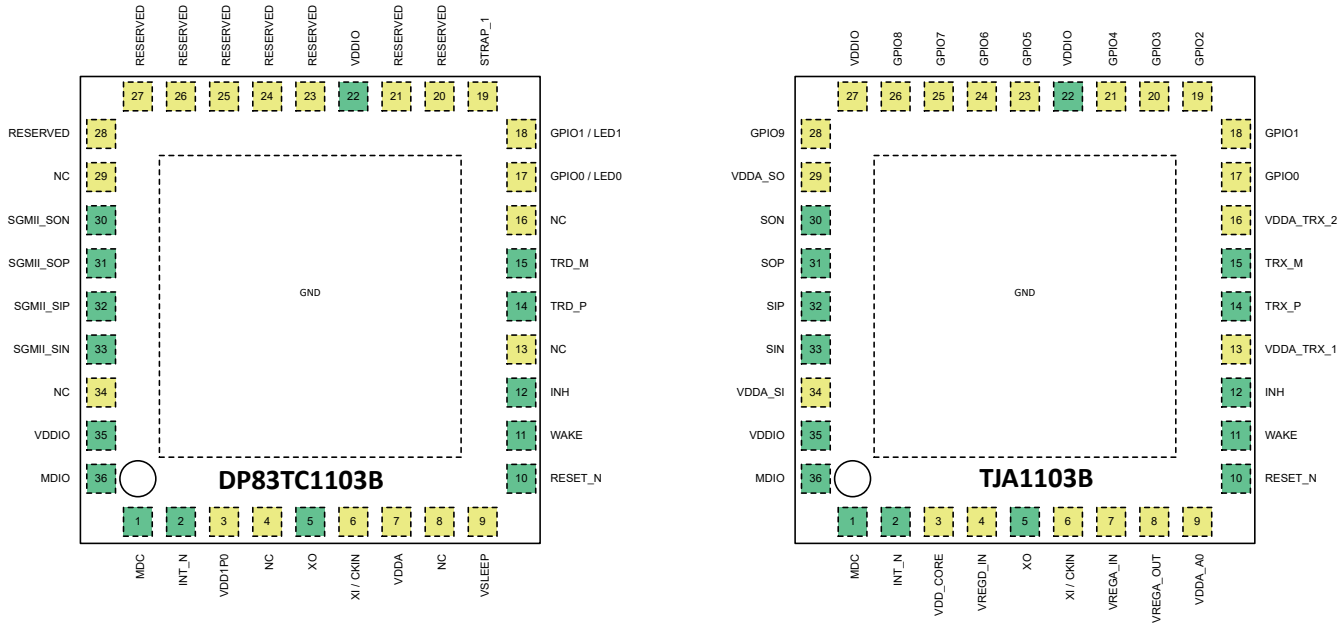


Figure 3-2. DP83TC1103B-Q1 vs TJA1103B Pinout

LEGEND	
Pins with same core functionality	Pins may have different function or may require schematic level provision. See Table 3-2

Pin differences between DP83TC1103B-Q1 and TJA1103B are highlighted in Table 3-2. The provisions in this table are the minimum required for functional design. More thorough provisioning is present in the DP83TC1103B-Q1 Common Schematic.

Table 3-2. DP83TC1103B-Q1 vs TJA1103B Pinout Differences

PIN NO.	DP83TC1103B-Q1 PIN NAME	TJA1103B PIN NAME	PROVISION REQUIRED	NOTES
3	VDD1P0	VDD_CORE	None	DP83TC1103B-Q1 uses for internal LDO decoupling capacitor. Depopulate any connections to external supply. See Power Supply Recommendations.
4	NC	VREGD_IN	None	Voltage regulator for the digital domain is internally connected on die for DP83TC1103x-Q1. No external connection is required.
5	XO	XO	Optional	Series resistor can be provisioned for tuning crystal power.
6	XI	XI	Optional	TI recommends 100Ω series resistor for optimum EMC performance when using crystal.
7	VDDA	VREGA	None	3.3V power rail for both devices. See Power Supply Recommendations.
8	NC	VREGA_OUT	None	DP83TC1103B-Q1 package NC.
9	VSLEEP	VDDA_AO	None	Always on power rail for TC-10. See Power Supply Recommendations.
13	NC	VDDA_TRX_1	None	DP83TC1103B-Q1 package NC.
16	NC	VDDA_TRX_2	None	DP83TC1103B-Q1 package NC.

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Table 3-2. DP83TC1103B-Q1 vs TJA1103B Pinout Differences (continued)

PIN NO.	DP83TC1103B-Q1 PIN NAME	TJA1103B PIN NAME	PROVISION REQUIRED	NOTES
17	GPIO0 / LED0	GPIO0	Optional	Register configuration may be needed for intended LED functionality.
18	GPIO1 / LED1	GPIO1	Optional	
19	STRAP_1	GPIO2	Optional	DP83TC1103B-Q1 uses for PHY address strap. See DP83TC1103B-Q1 Strap Configuration .
20	RESERVED	GPIO3	Optional	DP83TC1103B-Q1 input, can be connected to a signal not exceeding VDDIO voltage.
21	RESERVED	GPIO4	Optional	
23	RESERVED	GPIO5	Yes	Can be connected to a signal not exceeding VDDIO voltage. When device is in RESET mode or if the supplies of the device are ramping up (before Power-On RESET), this pin must not be driven externally. While this pin is expected to be in input mode when the device is in normal functional state, this pin can be driven by DP83TC1103B-Q1 until device initialization configuration is complete
24	RESERVED	GPIO6	Yes	Can be connected to a signal not exceeding VDDIO voltage. While this pin is expected to be in input mode when the device is in normal functional state, this pin can be driven by DP83TC1103B-Q1 until device initialization configuration is complete.
25	RESERVED	GPIO7	Yes	
26	RESERVED	GPIO8	Yes	
27	RESERVED	VDDIO	Optional	DP83TC1103B-Q1 input, can be connected to VDDIO supply or a signal not exceeding VDDIO voltage.
28	RESERVED	GPIO9	Optional	DP83TC1103B-Q1 input, can be connected to a signal not exceeding VDDIO voltage.
29	NC	VDDA_SO	None	DP83TC1103B-Q1 package NC.
34	NC	VDDA_SI	None	DP83TC1103B-Q1 package NC.

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4 Power Supply Recommendations

PIN NO.	DP83TC1103	TJA1103	NOTES
3	VDD1P0	VDD_CORE	VDD1P0 is connected to internal LDO on DP83TC1103x-Q1. TI recommends 100nF and 2.2µF decoupling capacitors. VDD1P0 does not require any external power connection.
7	VDDA	VREGA	3.3V power rail. TI recommends 10nF and 470nF decoupling capacitors. An optional ferrite bead can be used between VDDA and system 3.3V power rail.
9	VSLEEP	VDDA_AO	Always ON power rail for TC-10. TI recommends 100nF decoupling capacitor.
22, 35	VDDIO	VDDIO	1.8V, 2.5V, or 3.3V supply. TI recommends 470nF and 10nF decoupling capacitors.

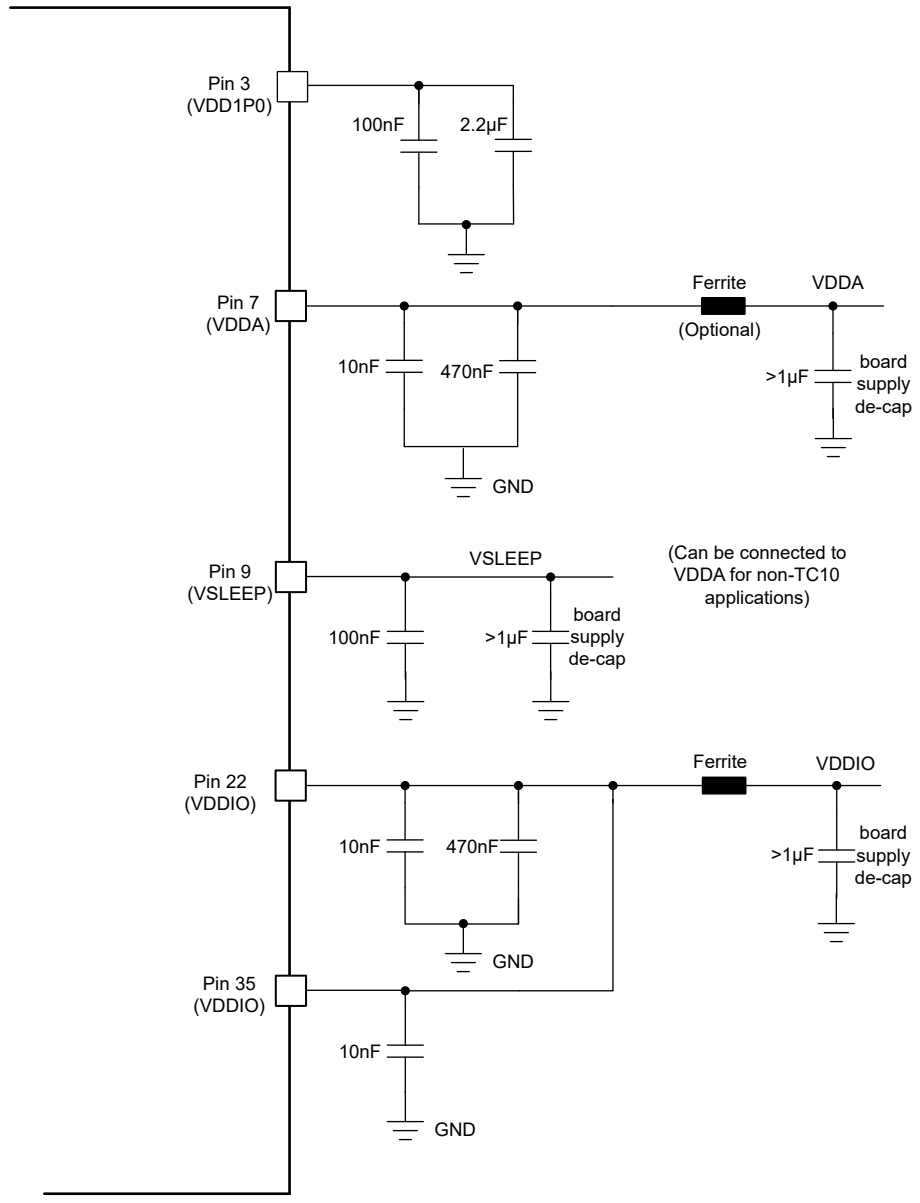


Figure 4-1. Decoupling Network - VDD1P0, VDDA, VSLEEP, VDDIO

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5 Strap Configuration

The DP83TC1103x-Q1 supports 2-level pin strapping. By default, internal pulldown resistors will strap pins to mode 1. An external 2.49kΩ pullup resistor can be populated to select mode 2.

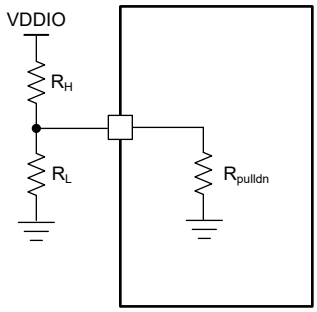


Figure 5-1. Strap Circuit

Table 5-1. Recommended 2-Level Strap Resistors

MODE	IDEAL RH (kΩ)
1	OPEN or PULL DOWN of any value
2	2.49

Note

- DP83TC1103x-Q1 MDI interface powers up in Follower mode. There is not a strap option for Leader mode. See Leader Mode Configuration.
- DP83TC1103x-Q1 MDI interface powers up in Managed mode. There is not a strap option for Autonomous mode. See Autonomous Mode Configuration.
- DP83TC1103x-Q1 does not support disabling polarity detection and correction. This is enabled by default.
- DP83TC1103A-Q1 does not have a strap option to enable MII. See MII Configuration.
- DP83TC1103B-Q1 does not have a strap option to enable SGMII. See SGMII Configuration.

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5.1 DP83TC1103A-Q1 Strap Configuration

Table 5-2. Bootstraps

PIN NAME	PIN NO.	DOMAIN	DEFAULT MODE	STRAP FUNCTION		DESCRIPTION
GPIO0	17	VDDIO	1	MODE	PHY_AD[2]	PHY_AD: PHY Address ID
				1	0	
				2	1	
RX_ER	19	VDDIO	1	MODE	PHY_AD[1]	
				1	0	
				2	1	
RX_D3	20	VDDIO	1	MODE	PHY_AD[0]	
				1	0	
				2	1	
RX_D2	21	VDDIO	1	MODE	MAC[1]	MAC: MAC Interface Selection
				1	0	
				2	1	
RX_D1	23	VDDIO	1	MODE	MAC[0]	
				1	0	
				2	1	
GPIO1	18	VDDIO	1	MODE	RESERVED	GPIO1 must be strapped into MODE 1.
				1	0	
				Reserved		

Table 5-3. PHY Address Bootstraps

PHY_AD[2:0]	GPIO0 STRAP MODE	RX_ER STRAP MODE	RX_D3 STRAP MODE	DESCRIPTION
000	1	1	1	PHY Address: d27 (0x1B)
001	1	1	2	PHY Address: d25 (0x19)
010	1	2	1	PHY Address: d21 (0x15)
011	1	2	2	PHY Address: d19 (0x13)
100	2	1	1	PHY Address: d9 (0x09)
101	2	1	2	PHY Address: d7 (0x07)
110	2	2	1	PHY Address: d3 (0x03)
111	2	2	2	PHY Address: d1 (0x01)

Table 5-4. MAC Interface Selection Bootstraps

MAC[1]	MAC[0]	DESCRIPTION
0	0	RGMII ID (RX delay only)
0	1	RGMII (No ID)
1	0	RMII Leader
1	1	RMII Follower

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5.2 DP83TC1103B-Q1 Strap Configuration

Table 5-5. Bootstraps

PIN NAME	PIN NO.	DOMAIN	DEFAULT MODE	STRAP FUNCTION		DESCRIPTION
GPIO0	17	VDDIO	1	**MODE**	**PHY_AD[1]**	PHY_AD: PHY Address ID
				1	0	
				2	1	
RX_ER	19	VDDIO	1	**MODE**	**PHY_AD[0]**	
				1	0	
				2	1	
GPIO1	18	VDDIO	1	**MODE**	**RESERVED**	GPIO1 must be strapped into MODE 1.
				1	0	
				Reserved		

Table 5-6. PHY Address Bootstraps

PHY_AD[1:0]	GPIO0 STRAP MODE	RX_ER STRAP MODE	DESCRIPTION
00	1	1	PHY Address: d27 (0x1B)
01	1	2	PHY Address: d21 (0x15)
10	2	1	PHY Address: d9 (0x09)
11	2	2	PHY Address: d3 (0x03)

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6 Register Configuration

DP83TC1103x-Q1 supports access to clause 45 registers using clause 22 indirect access method. More details on this can be found in the data sheet.

6.1 Leader Mode Configuration

The DP83TC1103x-Q1 devices power up in Follower mode by default. The PHY can be configured to Leader mode.

Table 6-1. Leader Mode Configuration

MMD [HEX]	REGISTER [HEX]	VALUE [HEX]	DESCRIPTION
01	0834	C000	Configure PHY to Leader Mode

6.2 Autonomous Mode Configuration

The DP83TC1103x-Q1 devices power up in managed mode by default. The PHY can be configured to Autonomous mode.

Table 6-2. Autonomous Mode Configuration

MMD [HEX]	REGISTER [HEX]	VALUE [HEX]	WRITE MASK [HEX]	DESCRIPTION
1F	018B	0040	0040	Configure PHY to Autonomous mode

6.3 MII Configuration

The DP83TC1103A-Q1 does not have a MII strap option. MII can be enabled via register configuration.

Table 6-3. MII Configuration

MMD [HEX]	REGISTER [HEX]	VALUE [HEX]	DESCRIPTION
1F	0600	0020	Disable RGMII
1F	0648	0100	Disable RMII

6.4 SGMII Configuration

The DP83TC1103B-Q1 powers on with SGMII disabled by default. SGMII must be enabled through register configuration.

Table 6-4. SGMII Configuration

MMD [HEX]	REGISTER [HEX]	VALUE [HEX]	DESCRIPTION
1F	0608	027B	Enable SGMII
1F	0600	0020	Disable RGMII
1F	0648	0100	Disable RMII

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7 Common Schematic

The common schematics included in this section showcase designs that would support either DP83TC1103x-Q1 or TJA1103 through the selection of passive components. The schematics also serve as reference schematics for DP83TC1103x-Q1 PHYs.

7.1 DP83TC1103A-Q1 Common Schematic

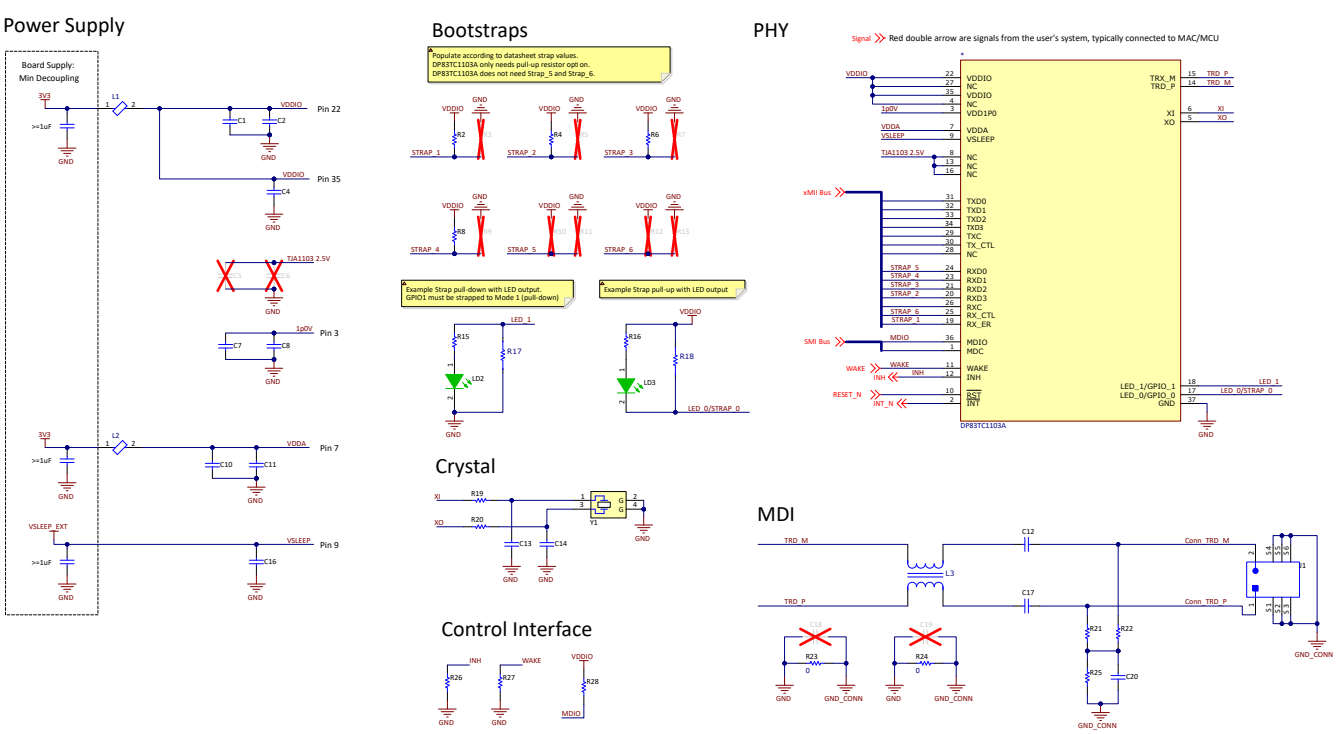


Figure 7-1. DP83TC1103A-Q1 Common Schematic

Table 7-1. DP83TC1103A-Q1 Common Schematic Component List

Functional Block	Reference Designator	DP83TC1103A-Q1 Component Value
VDDIO	L1	BLM18KG601SH1D
	C1	470nF
	C2	10nF
	C4	10nF
TJA1103 2.5V	C5	DNP
	C6	DNP
1.0V	C7	2.2µF
	C8	100nF
VDDA	L2	BLM18KG601SH1D
	C10	470nF
	C11	10nF
VSLEEP	C16	100nF
Control Interface	R26	10kΩ
	R27	10kΩ
	R28	2.2kΩ
Crystal	R19	100Ω
	R20	0Ω

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Table 7-1. DP83TC1103A-Q1 Common Schematic Component List (continued)

Functional Block	Reference Designator	DP83TC1103A-Q1 Component Value
MDI	L3	DLW43MH201XK2L, DLW32MH201XK2, AE2002, or ACT1210L-201
	C12	0.1µF
	C17	0.1µF
	R21	1kΩ
	R22	1kΩ
	R25	100kΩ
	C20	4.7nF
	C18	DNP
	C19	DNP
	R23	0Ω
	R24	0Ω

7.2 DP83TC1103B-Q1 Common Schematic

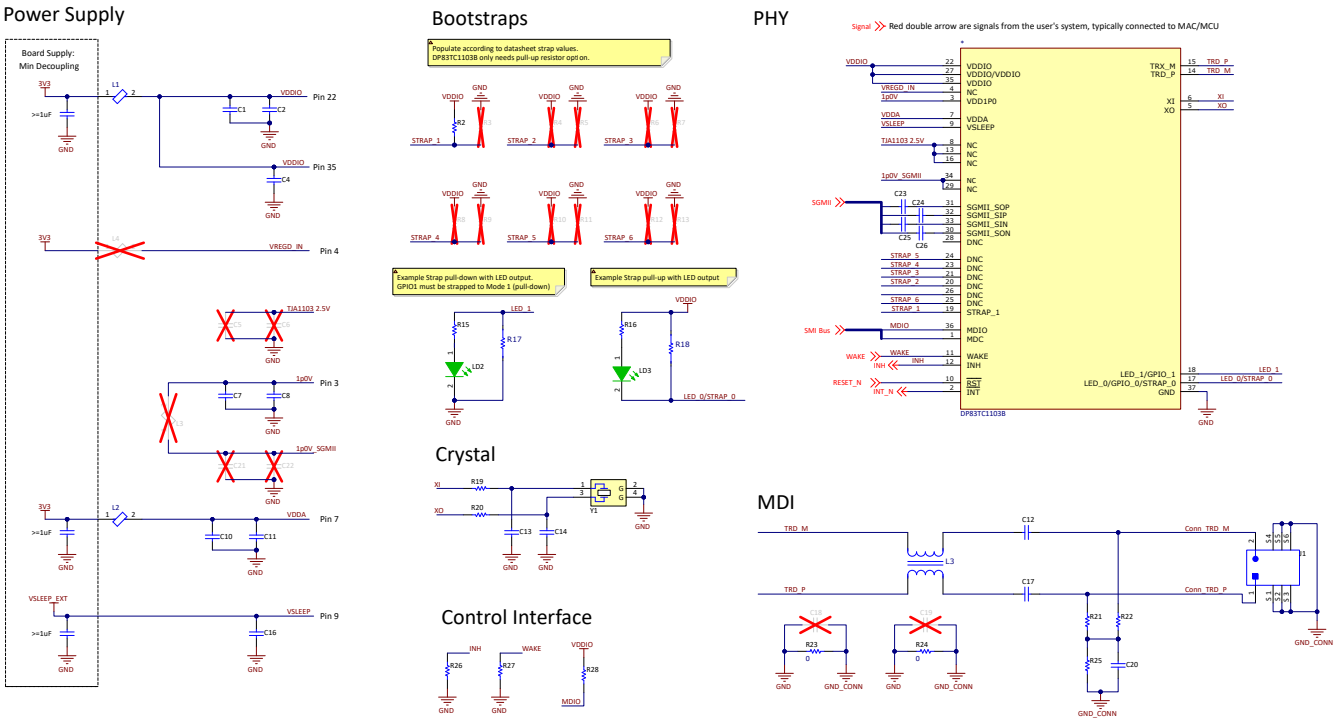


Figure 7-2. DP83TC1103B-Q1 Common Schematic

Functional Block	Reference Designator	DP83TC1103B-Q1
VDDIO	L1	BLM18KG601SH1D
	C1	470nF
	C2	10nF
	C4	10nF
TJA1103 2.5V	C5	DNP
	C6	DNP
1.0V	C7	2.2µF
	C8	100nF

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Functional Block	Reference Designator	DP83TC1103B-Q1
VDDA	L2	BLM18KG601SH1D
	C10	470nF
	C11	10nF
VSLEEP	C16	100nF
Control Interface	R26	10kΩ
	R27	10kΩ
	R28	2.2kΩ
Crystal	R19	100Ω
	R20	0Ω
SGMII	C23	0.1µF
	C24	0.1µF
	C25	0.1µF
	C26	0.1µF
MDI	L3	DLW43MH201XK2L, DLW32MH201XK2, AE2002, or ACT1210L-201
	C12	0.1µF
	C17	0.1µF
	R21	1kΩ
	R22	1kΩ
	R25	100kΩ
	C20	4.7nF
	C18	DNP
	C19	DNP
	R23	0Ω
	R24	0Ω
TJA1103 VREGD	L4	DNP
TJA1103 SGMII Power	L3	DNP
	C21	DNP
	C22	DNP

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8 Summary

The DP83TC1103x-Q1 PHYs offer sourcing flexibility by enabling a single board design to support multiple PHYs. By using the reference information in this application note, it is possible to quickly identify how a design can support DP83TC1103x-Q1.

9 References

- Texas Instruments, *DP83TC1103x-Q1 100Base-T1 Automotive Ethernet PHY Transceiver With IEEE802.1AS and TC10 Sleep-Wake*, datasheet.

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