

A Simple Diode Clamping Method to Generate Positive and Negative Output Voltages Using Single TPS61170



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Abstract

This application note introduces a simple and practical diode clamping method to generate the both positive and negative output voltages using Boost topology with TPS61170. A negative output voltage (-9V) is achieved by using two additional diodes while a positive output voltage (9V) is achieved by a typical application with Boost topology from 3V to 8V input voltage range. This method is simpler and offers cost advantages compared to using two different circuit topologies in parallel to generate the positive and negative supply rails. This approach is also excellent option for the input supply voltages of TI PMICLOADBOARD EVM ([PMICLOADBOARD EVM User Guide](#)). This application note demonstrates that the proposed application method performs well, as verified through simulation and experimental validation.

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1 Introduction

The TPS61170 is a monolithic, high-voltage switching regulator with integrated 1.2A, 40V power MOSFET. This device is mainly configured in Boost or SEPIC topologies with 1.2MHz fixed switching frequency, and external loop compensation components provide the application flexibility to optimize the performance.

The Boost topology is widely used when the output voltage is higher than the input voltage, and [Figure 1-1](#) shows a typical application circuit for 9V output from 5V input using the TPS61170. Although the implementation of a single output voltage is important, this application note presents a method for generating dual supply voltages (9V and -9V). The proposed approach can be widely used for biasing circuits for op amps and can also serve as an effective power supply design for the TI PMICLOADBOARDVM.

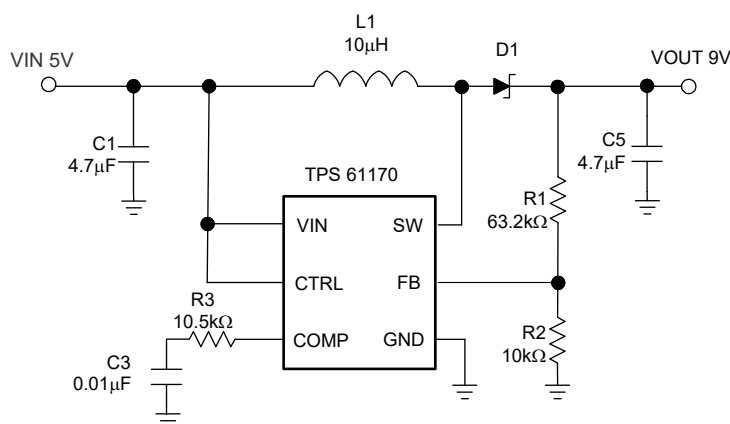


Figure 1-1. Typical Application Circuit for Boost Converters

2 Proposed Application Schematic

Figure 2-1 shows the proposed application schematic using the TPS61170 to have the both 9V and -9V from the input voltage range from 3V to 8V. This method presents a highly cost-competitive strategy that implements two output voltages over the wide input voltage range using one TPS61170 device. Figure 2-2 shows the main waveforms to achieve the both positive and negative output voltages.

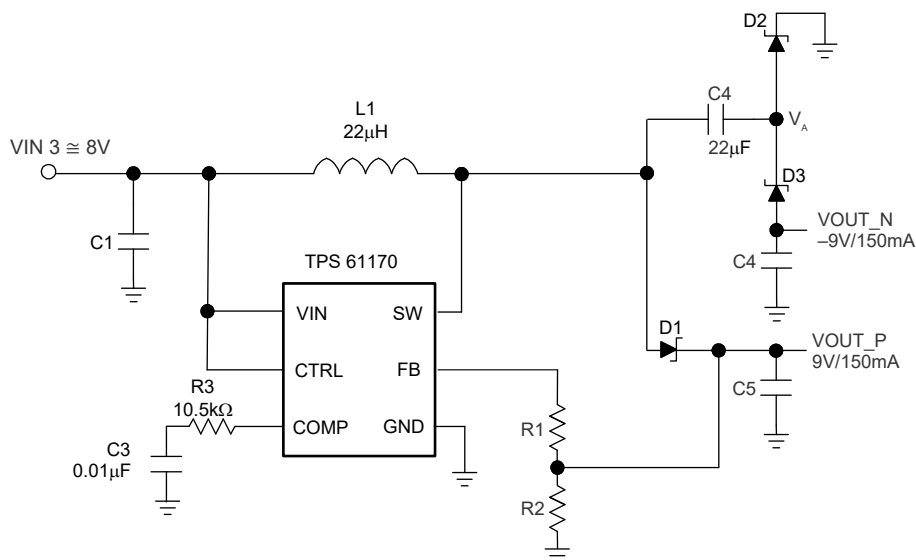


Figure 2-1. Proposed Application Circuit

When the internal switch of the TPS61170 is turned on, energy is stored in the inductor L1. Also, when the internal switch is turned off, the input voltage (V_{IN}) and the voltage across L1 (v_{L1}) are added together and applied to V_{SW} . During the off period of the internal switch, the stored energy in L1 is transferred to the two outputs. V_{OUT_P} is generated through D1 in the same manner as a conventional boost converter, while V_{OUT_N} is generated by C2, D2, and D3. At this time, the maximum voltage at V_A is limited to approximately +0.5V (V_{F_D2}) by D2, and the minimum voltage is maintained at approximately -9V by D3

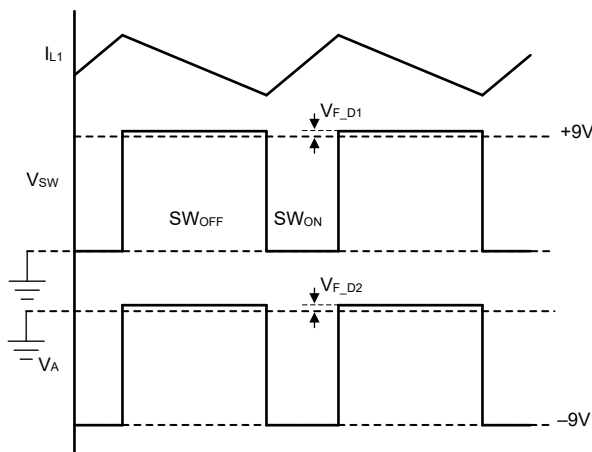


Figure 2-2. Principal Waveforms of the Proposed Method

For accurate output voltage regulation, the voltage of V_{OUT_P} is sensed, and this voltage must be tightly regulated. However, V_{OUT_P} is determined after the forward voltage drop across D1 from the V_{SW} node while V_{OUT_N} has two forward voltage drops through D2 and D3 during the switching operation inherently. As a result, an inherent voltage difference of approximately 0.5V occurs, causing V_{OUT_N} to be maintained at about -8.5V rather than exactly -9V in this case.

If this small voltage difference is not critical, the design shown in [Figure 2-1](#) can be used. However, if such a voltage deviation is not acceptable, the issue can be resolved by adding D4, as shown in [Figure 2-3](#), so that the same forward voltage drop is introduced on the positive output side. In this case, output voltage accuracy is improved, but efficiency is reduced due to the additional voltage drop introduced by D4.

[Figure 2-4](#) shows the main waveforms to achieve more accurate VOUT_N by adding D4. The important point here is that, to maintain VOUT_P at 9V, V_{SW} is determined by D1 and D4 as 9V + (V_{F_D1} + V_{F_D4}). Since these two diodes (D1 and D4) create the same forward voltage drops as those involved in establishing VOUT_N, a more accurate VOUT_N can be achieved.

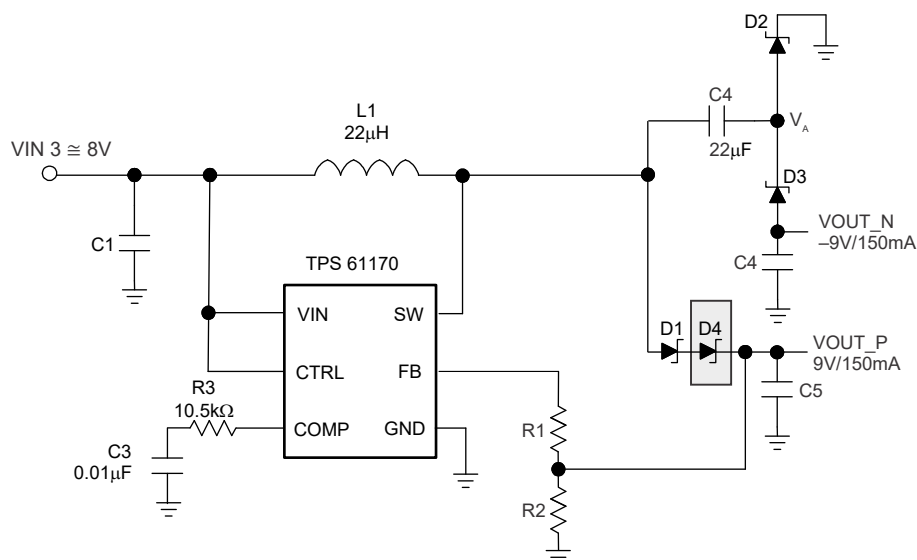


Figure 2-3. Proposed Method for Improving Negative Output Voltage by Adding D4

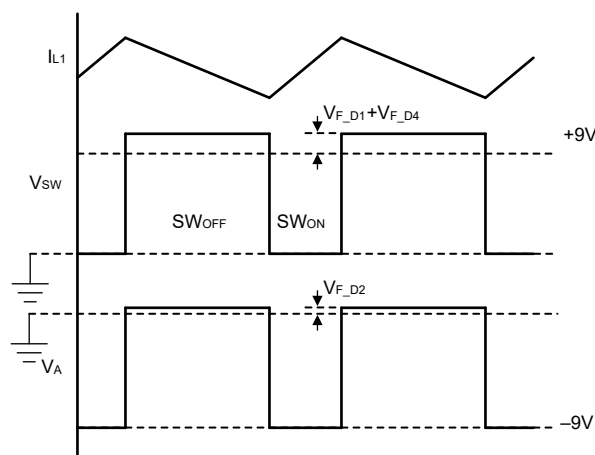


Figure 2-4. Principal Waveforms for Improving Negative Output Voltage Accuracy

3 Simulation Results

Figure 3-1 shows the simulation results during initial startup based on the schematic as shown in Figure 2-1 using D1 only. When the input voltage is 7V and the CTRL pin of the TPS61170 transitions from Low to High, the results demonstrate that both VOUT_P and VOUT_N outputs are properly regulated and stabilized normally.

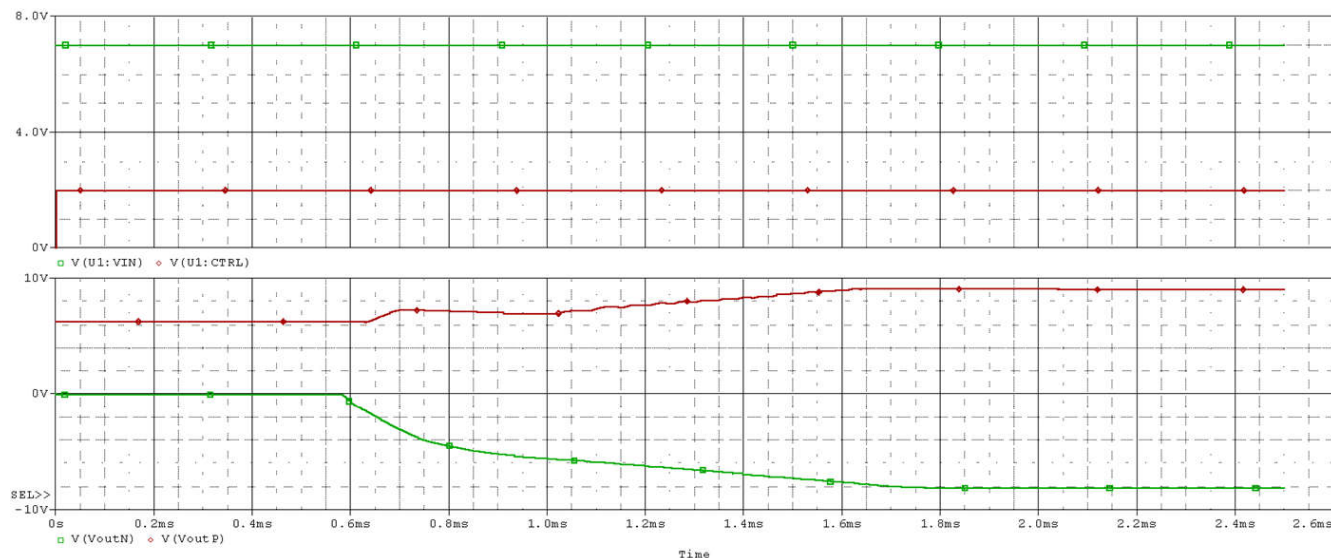


Figure 3-1. Initial Startup for the Both VOUT_P and VOUT_N

Figure 3-2 shows the principle current and voltage waveforms in steady-state operation. The VOUT_P and VOUT_N outputs are properly regulated, and the voltage waveforms of VSW and VA are also operating normally at a switching frequency of 1.2MHz. In addition, the inductor current of L1 is observed to operate in CCM.

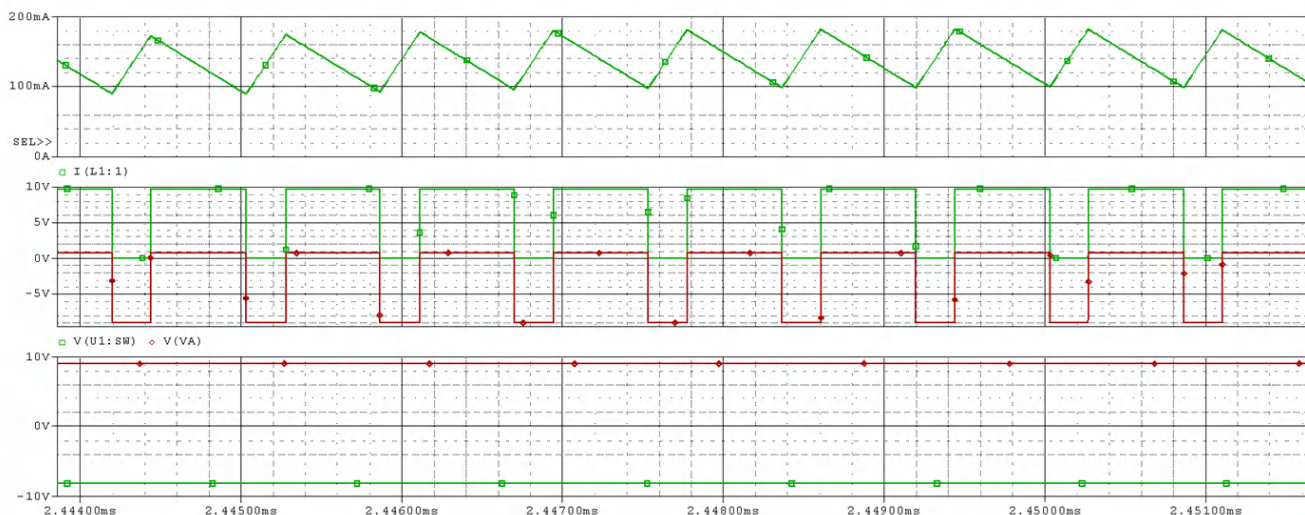


Figure 3-2. Principal Waveforms Under Steady-State Operation

Figure 3-3 shows the simulation results during initial startup based on the schematic as shown in Figure 2-3 using D1 and D4 together. When the input voltage is 7V and the CTRL pin of the TPS61170 transitions from Low to High in the same way, the results demonstrate that both VOUT_P and VOUT_N outputs are properly regulated and stabilize with more accurate VOUT_N output as it is shown in the simulation results below.

Simulation Results

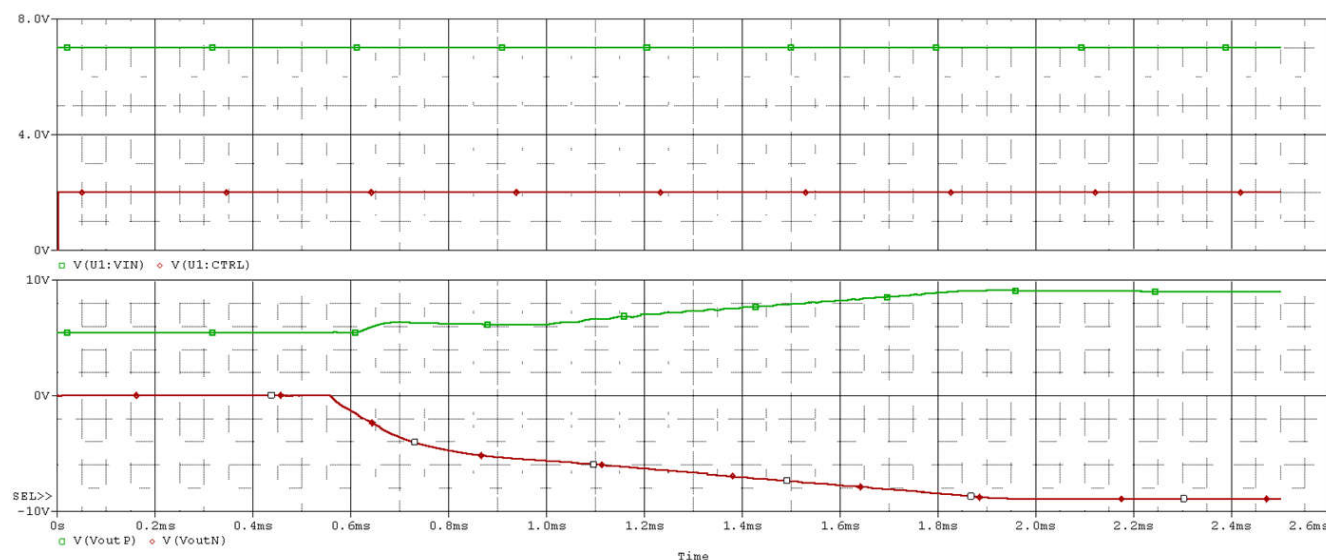


Figure 3-3. Initial Startup for the Both VOUT_P and VOUT_N Using D1 and D4

Figure 3-4 shows the principle current and voltage waveforms in steady-state operation using D1 and D4. The VOUT_P and VOUT_N outputs are properly regulated, and this allows a more accurate VOUT_N output to be obtained as shown in Figure 3-4.

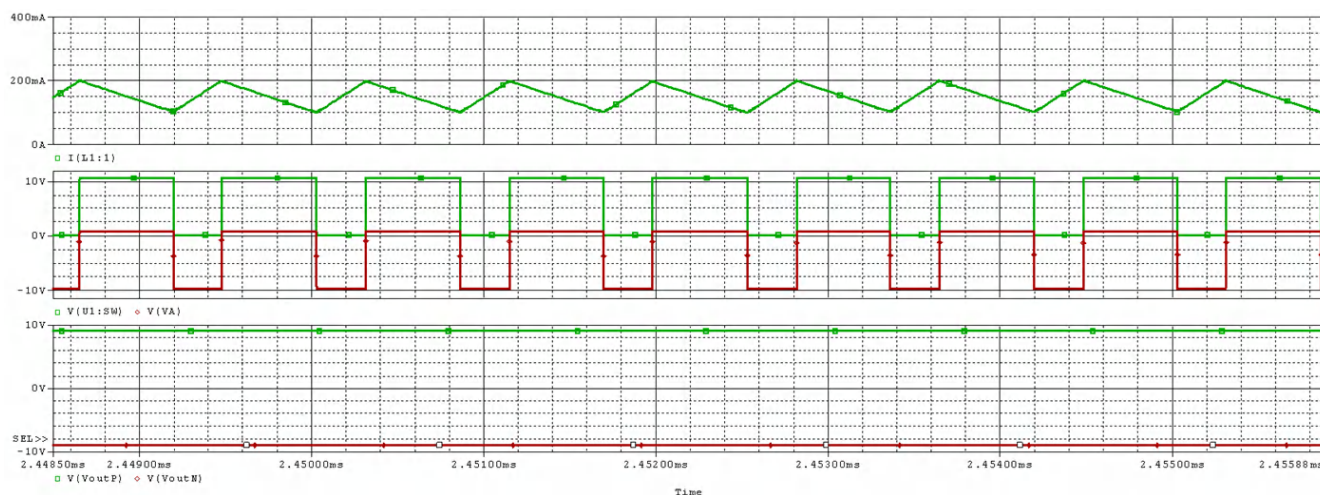


Figure 3-4. Principal Waveforms Under Steady-State Operation Using D1 and D4

4 Experimental Results

Figure 4-1 shows the experimental results (VIN: Ch4 in green with 5V/div, V_{OUT (+9V)}: Ch2 in light blue with 5V/div, V_{OUT (-9V)}: Ch3 in purple with 5V/div), demonstrating that both output voltages (9V and -9V) are properly regulated at an input voltage of 5V using D1. Since the internal MOSFET current limit of the TPS61170 is minimum 0.96A, the output load must be carefully considered to verify that this limit is not exceeded.

In addition, during initial startup, the output current is required not only to supply the output load but also to charge the output capacitors, resulting in a higher inductor current than that under normal steady-state operation.

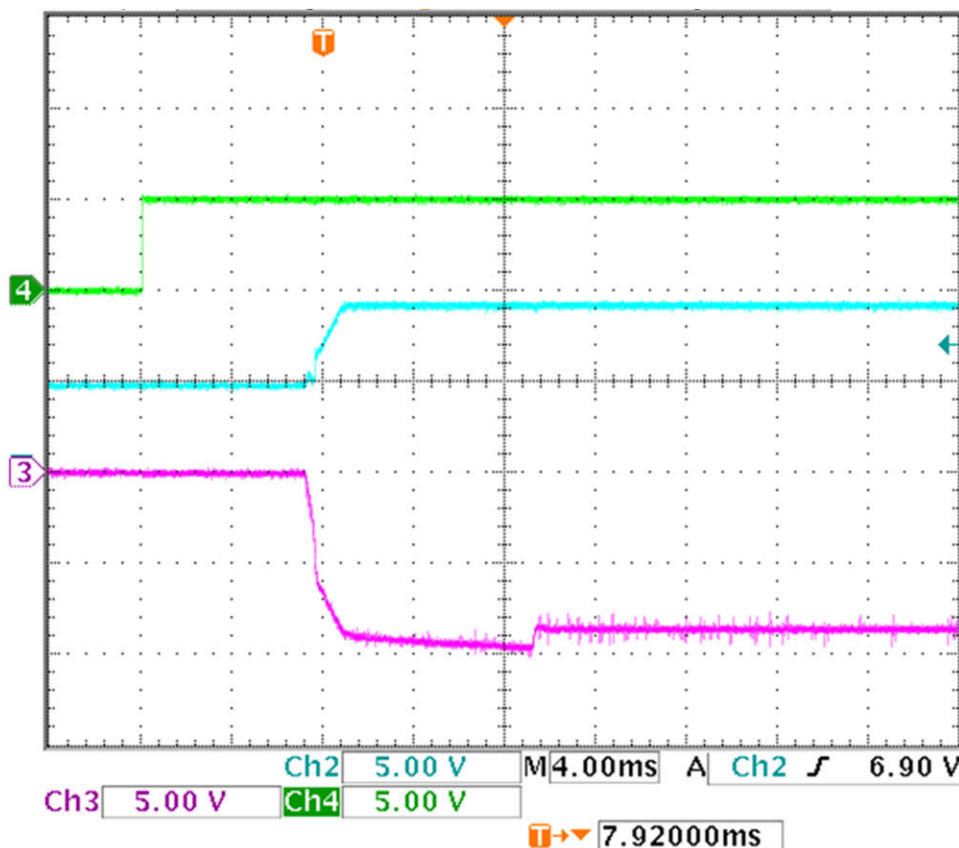


Figure 4-1. Startup Waveforms with 5V Input Using D1

Figure 4-2 shows the key voltage and current waveforms under steady-state operation (VSW: Ch4 in green with 5V/div, V_{OUT (9V)}: Ch2 in light blue with 5V/div, V_{OUT (-9V)}: Ch3 in purple with 5V/div, IL1: Ch1 in blue with 250mA/div). The 9V and -9V outputs are properly regulated, and the waveforms of VSW and inductor current of L1 are also operating normally at a switching frequency of 1.2MHz.

Figure 4-3 shows the waveforms when the TPS61170 is disabled, and this experimental waveform shows that both positive and negative output voltages turn off as the input voltage drops and reaches about 2.2V, which is the UVLO threshold voltage of the TPS61170.

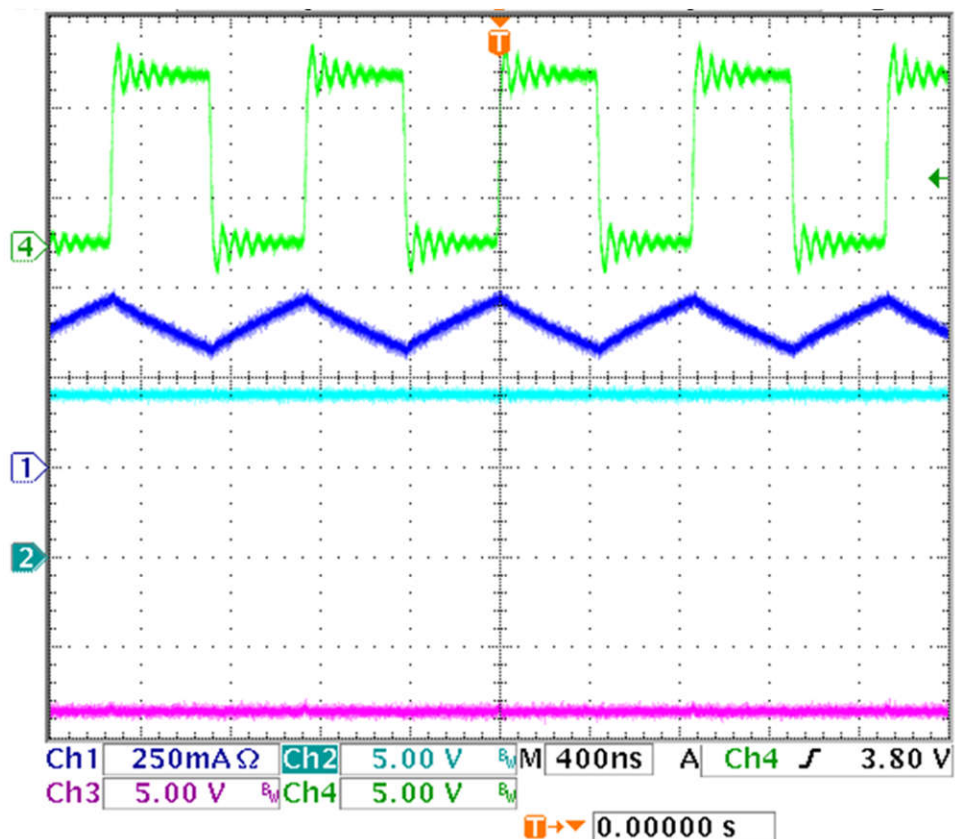


Figure 4-2. Key Waveforms Under Steady-State Operation

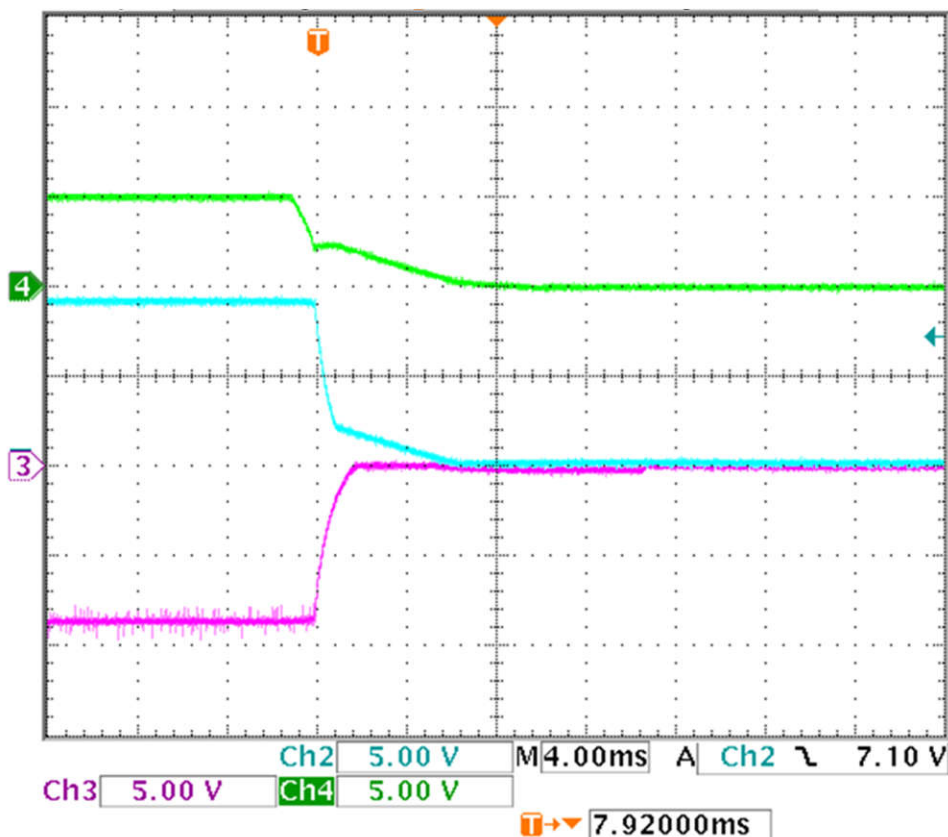


Figure 4-3. Waveforms When the TPS61170 is Disabled

Figure 4-4 shows the experimental results (V_{IN} : Ch4 in green with 5V/div, $V_{OUT (+9V)}$: Ch2 in light blue with 5V/div, $V_{OUT (-9V)}$: Ch3 in purple with 5V/div) using D1 and D2 in this case. The both output voltages (+9V and -9V) are properly regulated at an input voltage of 5V, and this method provides more accurate V_{OUT_N} as shown in the following waveform. Figure 4-5 shows the key waveforms when the TPS61170 is disabled with the same test conditions.

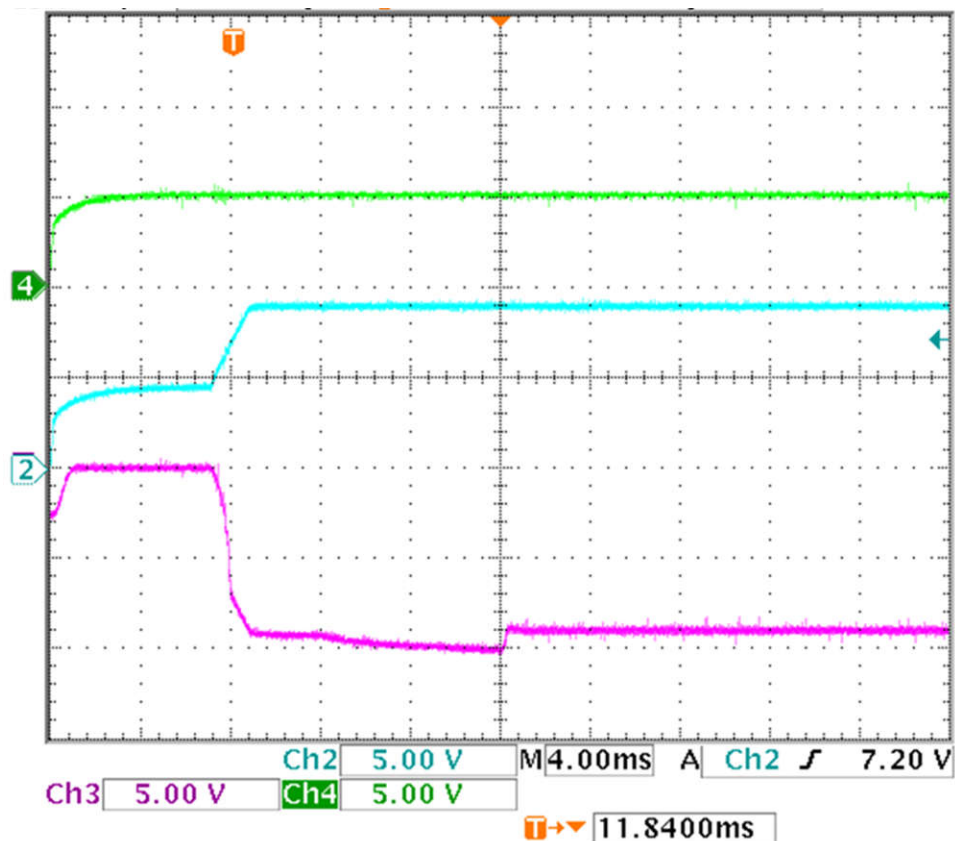


Figure 4-4. Startup Waveforms With 5V Input Using D1 + D4

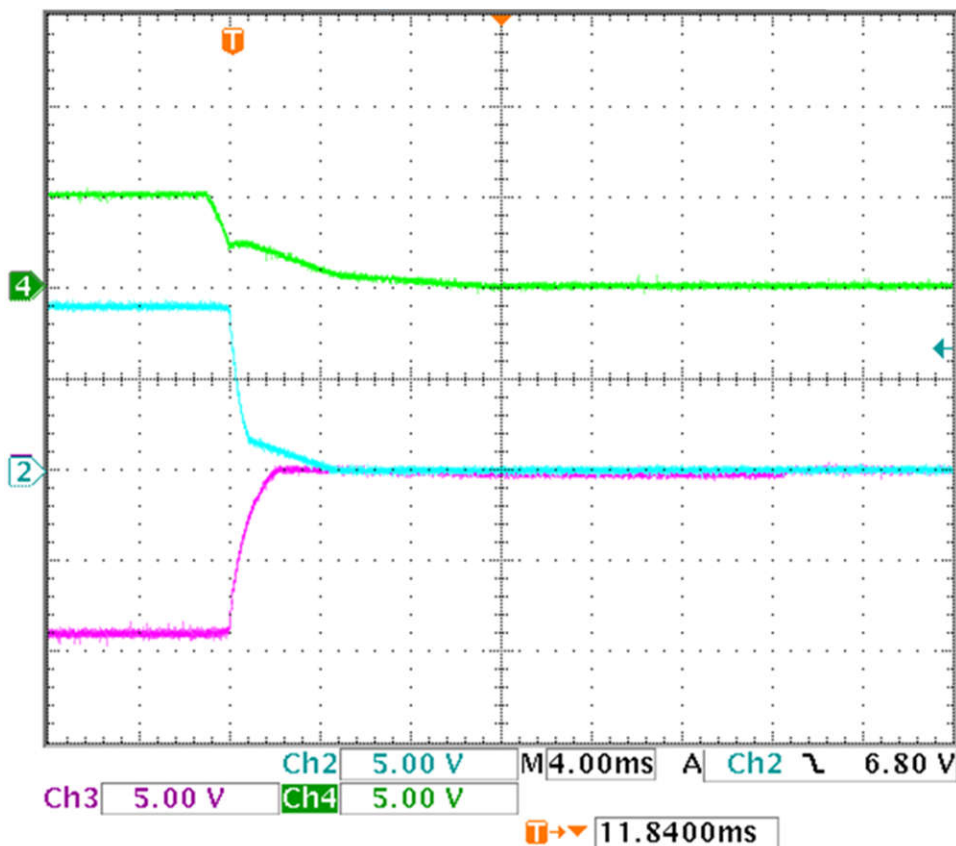


Figure 4-5. Waveforms when the TPS61170 is disabled

Figure 4-6 shows loop gain and phase margin for the both D1 and D1+D4 cases. As shown in the measured loop gain results, when only D1 is used, the crossover frequency is 31kHz and the phase margin is approximately 53 degrees. When D1 and D4 are used together, the crossover frequency is 27kHz and the phase margin is approximately 50 degrees. In both cases, stable frequency response characteristics are achieved.

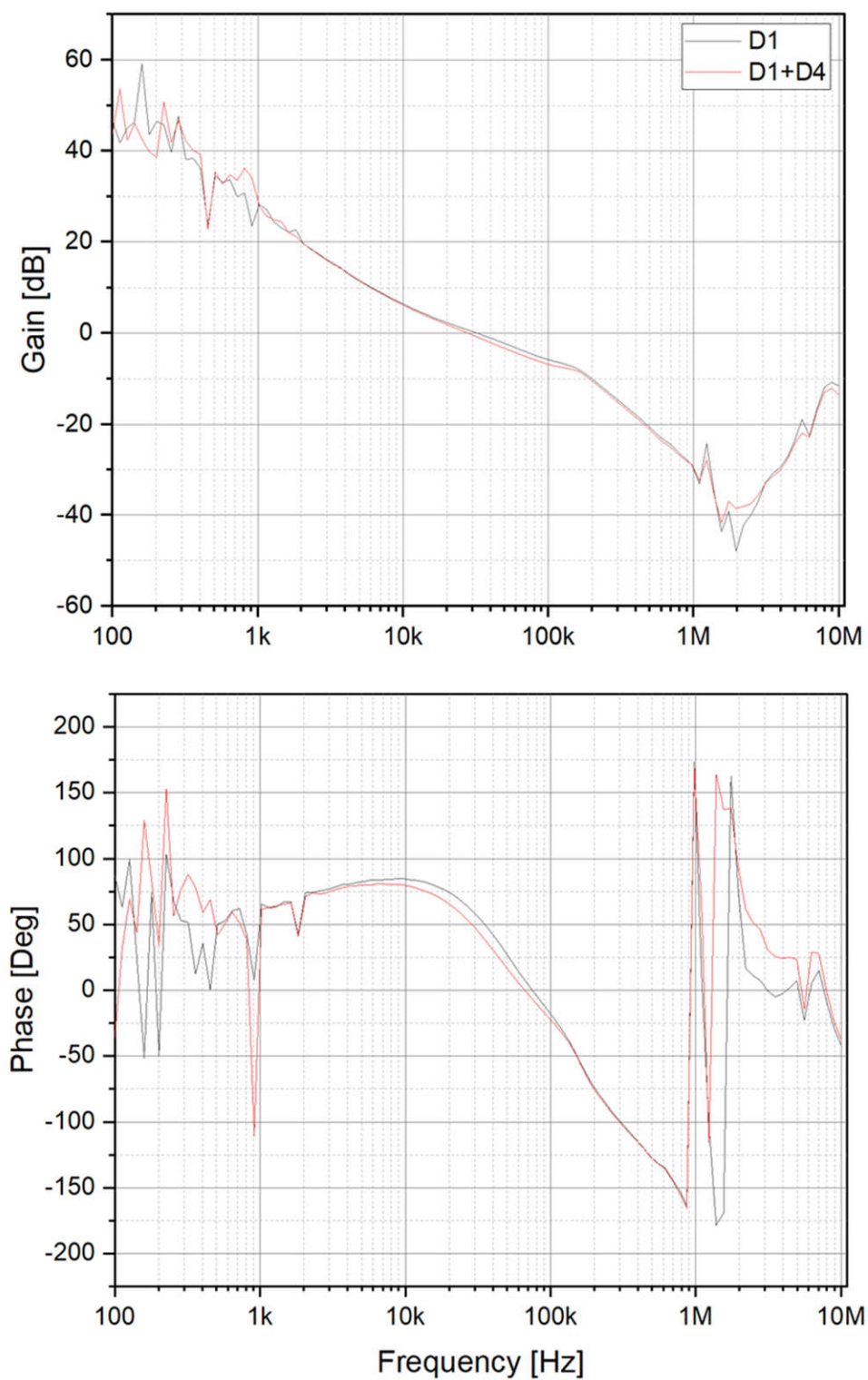


Figure 4-6. Loop Gain and Phase Margin

5 Summary

A practical approach to achieving positive and negative output voltages (9V and -9V) with Boost topology is proposed in this application note. As it has been confirmed with the actual application case using TI PMICLOADBOARD EVM (SLUUC92), the design operates properly and provides accurate output voltage regulation. The key point is a negative output voltage (-9V) is achieved by using two additional diodes while a positive output voltage (9V) is achieved by a typical application with Boost topology from 3V to 8V input voltage range. This method is simpler and offers cost advantages compared to using two different circuit topologies in parallel to generate the positive and negative supply rails. This application note demonstrates that the proposed application method performs well, as verified through simulation and experimental validation.

6 References

1. Texas Instruments, [TPS61170 1.2A High-Voltage Boost Converter in 2mm × 2mm² QFN Package](#), datasheet.
2. Texas Instruments, [TPS61170EVM-280 Evaluation Module, User's Guide](#), user's guide.
3. Texas Instruments, [PMICLOADBOARD EVM Evaluation Module User's Guide](#), user's guide.

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