Application Note

Electrical Overstress (EOS) Protection Guidelines for AM26xx and C2000 Microcontrollers

Shivasharan Nagalikar, Tejas Kulkarni, Jason Whiles

ABSTRACT

Electrical Overstress (EOS) protection is critical for ensuring long-term reliability of semiconductor devices in industrial and automotive applications. This application report provides comprehensive EOS protection strategies/guidelines, specifically designed for TI AM26xx (AM263x, AM263P4x, AM261x) and C2000 real-time microcontroller families.

Design examples with detailed calculations, component selection criteria, and board layout guidelines are provided to help engineers implement robust EOS protection in their systems. Representative case studies illustrate common EOS scenarios and their prevention methods.

Table of Contents

Copyright © 2026 Texas Instruments Incorporated

Trademarks

All trademarks are the property of their respective owners.

Copyright © 2026 Texas Instruments Incorporated

1 Introduction

1.1 Purpose and Scope

This application note provides comprehensive guidance for protecting Texas Instruments AM26xx (AM263x, AM263Px, AM261x) and C2000 family devices from Electrical Overstress (EOS) events in industrial, automotive, and control applications. The document is intended for:

- Hardware design engineers developing embedded systems
- PCB layout designers implementing EOS-robust boards
- Test engineers performing In-Circuit Testing (ICT)
- Quality and reliability engineers analyzing field failures

The recommendations and design guidelines in this document are based on device datasheets, reliability data, failure analysis reports, and industry best practices. While focused on AM26xx and C2000 devices, many principles apply broadly to other microcontroller families.

1.2 EOS Definition and Importance

Electrical Overstress (EOS) occurs when a device is subjected to voltage, current, or power levels that exceed its specified absolute maximum ratings, resulting in immediate or latent damage to the semiconductor device. Unlike Electrostatic Discharge (ESD), which involves brief, high-voltage pulses, EOS events typically involve:

Table 1-1. EOS Definition

Characteristic	EOS Event Description
Voltage Level	2-3× normal operating voltage (not kV-level like ESD)
Duration	Microseconds to continuous (much longer than ESD)
Energy	Higher total energy than ESD events

Industry field return data consistently shows that 30-40% of semiconductor device failures are attributed to EOS events. These failures can occur during:

- Manufacturing and assembly processes
- In-Circuit Testing (ICT) and functional testing
- System power-up and power-down sequences
- Hot-plugging of cables and connectors
- Transient events from inductive loads or switching

WARNING: EOS damage can be latent, meaning devices may appear functional initially but fail prematurely in the field due to degraded internal structures. This makes root cause analysis difficult and emphasizes the importance of prevention.

1.3 EOS vs ESD

It is critical to understand the difference between EOS and ESD, as protection strategies differ significantly:

Parameter	ESD Events	EOS Events
Voltage Level	kV range (typically 1-8kV)	V range (typically 5-50V)
Duration	Nanoseconds (< 100ns)	Microseconds to continuous
Peak Current	Amperes (brief spike)	Milliamps to Amps (sustained)
Total Energy	Low (brief duration)	High (longer duration)
Protection	On-chip ESD structures	External components + design
Testing Standard	HBM, CDM (JEDEC)	IEC 61000-4-2, system-level

Table 2; EOS Vs ESD

Note: While all AM26xx and C2000 devices include on-chip ESD protection structures rated for HBM and CDM testing, these structures have limited current-handling capability (typically ±2mA continuous) and cannot protect against sustained EOS events without external protection.

Copyright © 2026 Texas Instruments Incorporated

2 Device Overview and EOS Susceptibility

2.1 AM26xx Series Overview

The AM26xx family includes AM263, AM263P, and AM261 real-time microcontrollers targeting automotive, industrial automation, motor control, and Industrial Ethernet applications. Key features include:

- ARMs Cortex-R5F cores up to 400 MHz
- Industrial Ethernet (EtherCAT, PROFINET, EtherNet/IP)
- High-speed ADCs and PWM modules for motor control
- OSPI/QSPI flash interfaces\
- Multiple power domains: VDD_CORE (1.2V), VDDSHV (3.3V), VDDA (3.3V)
- Temperature range: -40°C to 125°C (industrial) or -40°C to 150°C (automotive)

The AM26x devices are available in 256-pin, 293, 304 and 324-pin BGA packages, providing extensive I/O options for complex automotive and industrial systems.

2.2 C2000 Series Overview

The C2000 real-time microcontroller family (F28004x, F2837x, F2838x) is optimized for power electronics and motor control applications. Key features include:

- C28x DSP cores up to 200MHz
- Control Law Accelerator (CLA) co-processor
- High-resolution PWM with 150 ps resolution
- 16-bit ADCs with differential inputs and simultaneous sampling
- Integrated comparators for cycle-by-cycle current limiting
- Power domains: VDD (1.2V), VDDA (3.3V), VDDIO (3.3V or 1.8V), VDDPLL
- Bootstrap circuit support for high-side gate drivers

C2000 devices are available in 64-pin to 337-pin packages, supporting applications from single-phase inverters to complex three-phase motor drives.

2.3 Critical Pins and Interfaces

Certain pins and interfaces are particularly susceptible to EOS damage and require careful protection:

2.3.1 Power Supply Pins

- VDD_CORE / VDD: Core logic supply (1.2V)
- VDDSHV / VDDIO: I/O supply (typically 3.3V, some support 1.8V)
- VDDA / VDDAPLL: Analog supply for ADC and PLL (3.3V)
- VSS / VSSA: Ground references

Critical Considerations

- Power pins must be properly sequenced during power-up and power-down
- Decoupling capacitors must be placed close to device (within 10mm)
- Each power domain/rail requires separate monitoring and protection

2.3.2 Reset and Configuration Pins:

- PORz (Power-On Reset): Power on reset (logic low enable) pin
- WARMRSTn: Warm reset (logic low enable) input and reset status output pin
- Boot mode [SOP – Sense On Power] configuration pins

EOS Risks

- Applying signal voltage before VDD is valid can cause latch-up
- Slow rise times on PORz (>1ms) can leave device in undefined state
- Diodes in PORz path can cause premature release before power rails stabilize

2.3.3 Communication Interface Pins:

- Ethernet (AM26xx): RMII/RGMII interfaces to external PHY

Copyright © 2026 Texas Instruments Incorporated

- SPI, I2C, UART: Standard communication peripherals
- CAN/MCAN: Automotive and industrial bus interfaces

External Connections Make These Pins Vulnerable To:

- ESD events from cable connections
- Ground potential differences between systems
- Hot-plugging during system integration or service

2.3.4 Analog Input Pins (ADC):

- Single-ended or differential analog inputs
- Typically designed for 0-3.3V input range
- Some C2000 devices support 0-5V input

Protection Requirements:

- Series resistors to limit current during overvoltage
- Clamping diodes or TVS for transient suppression
- RC filtering for noise immunity

2.3.5 PWM Output Pins (C2000):

- High-speed switching outputs for gate drivers
- May interface to bootstrap circuits at high voltages
- Fast edge rates increase susceptibility to EMI-induced EOS

2.4 Power Domains and Sequencing Requirements

Both AM26xx and C2000 devices have multiple power domains that must be sequenced correctly to prevent EOS damage.

2.4.1 AM26xx Power Domains:

- VDD_CORE (1.2V): Core logic and memory
- VDDSHV (3.3V): High-voltage I/O including Ethernet PHY interface
- VDDA (3.3V): Analog circuits (ADC, oscillators)

2.4.2 Sequencing requirements:

- VDD_CORE/VDDSHV must be stable before releasing PORZ
- All supplies must ramp monotonically (no dips or reversal)
- During power-down, order may be reversed
- Please refer to device specific datasheet

2.4.3 C2000 Power Domains:

- VDD (1.2V): Core logic, flash memory, peripherals
- VDDA (3.3V): Analog circuits (ADC, PLL, oscillators)
- VDDIO (3.3V or 1.8V): I/O buffers
- VDDPLL: PLL analog supply (typically connected to VDDA)
- Please refer to device specific datasheet

2.4.4 Consequences of Sequencing Violations:

1. **Shoot-Through Current**:

   When I/O buffers receive input signals before their power supply is valid, both NMOS and PMOS output transistors may be partially on simultaneously, causing high current flow from VDDIO to VSS through the output stage.
2. **ESD Diode Stress**:

   Signal pins driven high while VDD is not yet valid will forward-bias the ESD protection diode from signal pin to VDD, injecting current into the unpowered VDD rail.
3. **Undefined Device State**:

Copyright © 2026 Texas Instruments Incorporated

Premature release of reset (PORz going high) before power supplies stabilize can cause the device to begin operation with invalid supply voltages. This can corrupt internal registers, flash memory programming, or cause erratic behavior difficult to debug.

Copyright © 2026 Texas Instruments Incorporated

3 EOS Fundamentals and Failure Mechanisms

3.1 ESD Diode Current Specification

Most AM26xx and C2000 microcontrollers specify a maximum ESD diode current of ±2mA in the Absolute Maximum Ratings section of their datasheets. This specification is critical for proper system design and is often misunderstood.

3.1.1 Understanding the Specification

The ±2mA ESD diode current specification represents the maximum CONTINUOUS current that can safely flow through the on-chip ESD protection structures to the supply rails (VDD or VSS). These ESD structures are triggered when:

- A signal voltage exceeds VDD + 0.3V (upper ESD diode conducts to VDD)
- A signal voltage falls below VSS - 0.3V (lower ESD diode conducts to VSS)

Key points about this specification:

• The ±2mA limit applies to CONTINUOUS or long-duration current flow (milliseconds or longer)

• The ESD structures can withstand much higher currents during actual ESD events (amperes for nanoseconds) as specified by HBM/CDM ratings

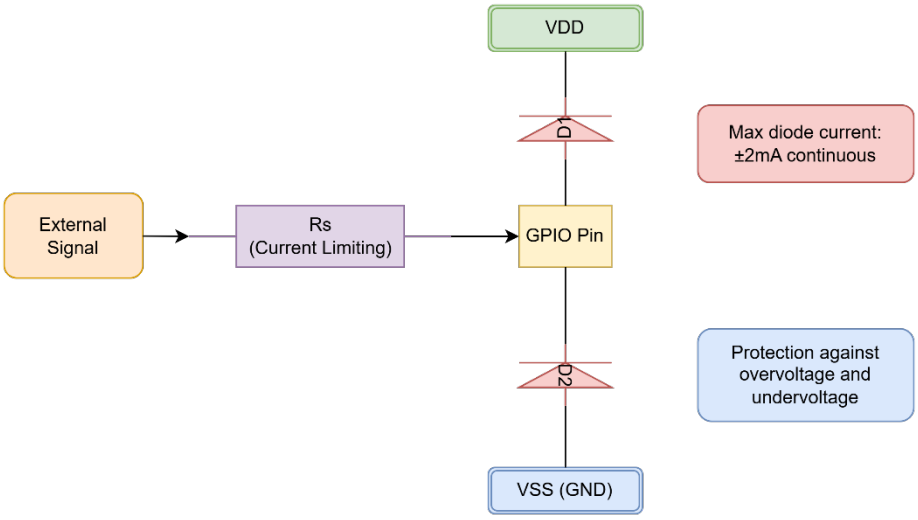
• The limit is thermal in nature - continuous current causes heating that can damage the structure

• Application design must limit current through external resistors or prevent overvoltage conditions

3.1.2 ESD Diode Protection Structure

The on-chip ESD protection on each I/O pin typically consists of:

- Upper clamp diode from I/O pin to VDD rail
- Lower clamp diode from VSS rail to I/O pin
- Internal resistances and parasitics



Typical ESD Diode Protection Structure

Figure 1; ESD Diode Structure

3.1.3 Important Side Effects During Power Cycling

CRITICAL WARNING: The ESD diode specification methods do NOT apply when the main supply (VDD/ DVCC) is unpowered and voltage is applied to a GPIO pin. This can cause unintended power sourcing to the MCU through ESD structures, leading to:

Copyright © 2026 Texas Instruments Incorporated

- Device back-powering through I/O pins
- Unpredictable device behavior and code execution
- Memory corruption
- Potential physical damage to the device

To prevent back-powering issues:

- Ensure main supply powers up before or simultaneously with any I/O signals
- Account for LDO delays and inline capacitance in power sequencing

3.2 System Design EOS Sources

Beyond component-level and PCB-level protection, system-level design decisions significantly impact EOS susceptibility.

3.2.1 Bus Contention

Bus contention occurs when multiple drivers attempt to control the same signal line simultaneously, creating high current flow between outputs. This is particularly damaging during power sequencing or mode transitions.

Common Scenarios

- Multiple devices driving a shared SPI bus without proper chip select control
- I2C bus contention during address conflicts
- GPIO pins configured as outputs on multiple devices connected to same net
- Bidirectional level shifters with improper enable sequencing

Prevention Strategies

- Implement strict chip select protocols for shared buses
- Use tri-state buffers with enable controls for multi-master systems
- Configure all GPIOs as inputs (high-impedance) during power-up
- Add series resistors (22-100Ω) on potentially contended signals to limit current

3.2.2 Incorrect Voltage Levels

Applying incorrect voltage to device pins is a direct cause of EOS. This can occur through:

• Level Shifter Failures: When level shifters fail or are incorrectly configured, 5V signals can reach 3.3V-rated pins.

• Hot-Plug Events: When boards are connected to powered systems, voltage transients can occur. Implement hot-plug protection with series resistors, TVS diodes, and controlled slew rates.

• Backpowering: Current flowing through I/O pins into powered-down voltage domains can cause phantom powering and latchup. Use isolation buffers or series diodes to prevent back powering paths.

• Verify that all voltage measurements remain within datasheet specifications under all operating conditions. Perform measurements across multiple production units to account for component tolerances and board-to-board variations.

• Use power supplies equipped with overvoltage protection (OVP) and undervoltage protection (UVP). These safeguards automatically disable the supply when voltage exceeds safe thresholds, preventing electrical overstress (EOS) from voltage spikes and brownout conditions from voltage sags.

3.2.3 Impedance Mismatch and Signal Integrity

Transmission line effects become significant for signals above 50MHz or trace lengths exceeding 6 inches. Impedance mismatches cause reflections that can double the signal voltage at the receiving end.

For high-speed interfaces on AM26xx (RGMII, OSPI/QSPI) and C2000 (eQEP, high-speed PWM):

• Match trace impedance to driver/receiver specifications (typically 50Ω single-ended, 100Ω differential)

• Provide proper termination: series termination at driver, parallel termination at receiver, or AC termination for bidirectional signals

Copyright © 2026 Texas Instruments Incorporated

• Keep trace lengths matched for differential pairs (within 5 mils)

• Avoid stubs longer than λ/10 at maximum operating frequency

Without proper termination, reflected voltage can reach 2× times IO Voltage, potentially activating or exceeding ESD diode ratings.

3.2.4 Inadequate Filtering and Grounding

Power supply noise and ground bounce can cause transient overstress events. High-frequency transients may couple through ESD protection diodes, causing localized heating and gradual degradation.

Filtering requirements:

- Bulk decoupling: 10-100µF per power domain within 2cm of device
- High-frequency decoupling: 0.1µF and 0.01µF within 5mm of each power pin
- Ferrite beads on analog supply pins: 100-300Ω @ 100MHz
- Common-mode chokes on communication interfaces exposed to external connections

Grounding best practices:

- Continuous ground plane under device with minimal cutouts
- Multiple ground vias adjacent to each VSS pin (target <1mΩ to plane)
- Separate analog and digital ground regions, connected at single point near device
- Shield grounded to chassis at cable entry, not at PCB
- During power-down, disable or tri-state I/O pins or put pins into input mode before removing main power
- Consider external protection circuits for I/O pins that remain powered when MCU is off

Copyright © 2026 Texas Instruments Incorporated

4 I/O Interface Protection

4.1 Digital I/O Protection

Digital I/O pins on AM26xx and C2000 devices typically have internal ESD protection diodes to VDD and VSS. However, external protection is often required when:

- Pins are exposed to external connectors
- Signals traverse long cables or PCB traces
- Interface voltages may exceed device ratings
- Fast transients from inductive loads are present

For example, TVS diode and clamping diodes can be used for protecting digital and analog input pins respectively.

4.2 Communication Interface Protection

4.2.1 Industrial Ethernet (AM26xx RMII/RGMII):

Ethernet PHY interfaces require protection as they connect to external cables that can experience ESD from cable insertion/removal, lightning-induced surges, and ground potential differences.

Protection strategy:

- Place TVS diodes at connector (before magnetics if present)
- Series resistors (22Ω to 33Ω) on all signal lines between MCU and PHY
- Common-mode chokes for differential pairs
- Chassis ground connection through high-voltage capacitor (1nF / 2kV)

4.2.2 CAN Bus:

CAN transceivers typically have built-in ESD protection, but additional protection may be needed:

- TVS diode (24V standoff for 12V systems, 48V for 24V systems) across CAN_H and CAN_L
- Common-mode choke for EMI immunity
- Galvanic isolation using isolated CAN transceivers for harsh environments

4.2.3 SPI, I2C, UART:

For short on-board traces: Series resistors (22Ω to 47Ω) usually sufficient

For external connectors: Add TVS diodes (5V or 6V standoff) to ground

4.3 PWM Output Protection (C2000)

PWM outputs driving external gate drivers or power stages require protection against inductive kickback from motor winding, bootstrap circuit coupling, and shoot-through events in power stage.

Basic Protection:

Rs = 22Ω to 47Ω, D1, D2 = Fast Schottky diodes (BAT54)

For high-side drivers with bootstrap:

- Ensure series resistor can handle bootstrap charging current
- Add Zener clamp if bootstrap voltage can exceed MCU VDDIO during faults

Isolation:

For high-voltage motor drives (>100V DC bus), use isolated gate drivers to prevent ground-referenced PWM signals from being stressed by power stage transients.

Copyright © 2026 Texas Instruments Incorporated

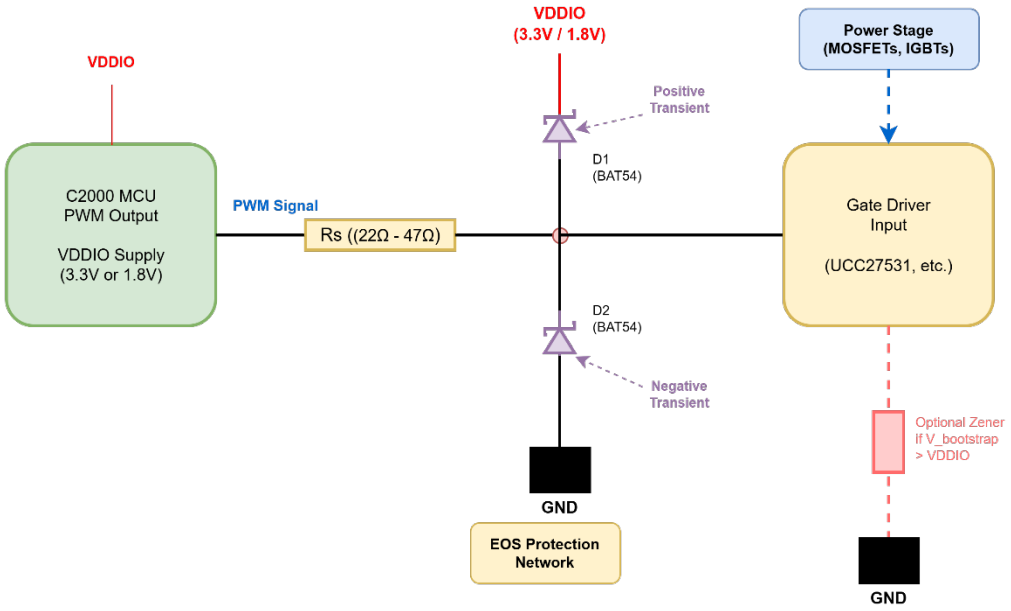


Figure 2; Basic Protection for C2000 PWM Outputs Driving Gate Drivers

Copyright © 2026 Texas Instruments Incorporated

5 PCB Design Guidelines

5.1 Component Placement

Proper placement of components relative to the microcontroller is critical for EOS protection:

Decoupling Capacitors:

- Place 100nF ceramic capacitors within 5mm of each VDD pin
- Use low-ESL packages (0402 or 0603 X7R/X5R ceramic)
- Bulk capacitors (10µF to 47µF) can be placed within 10mm

Protection Components:

- TVS diodes at connectors: Place as close as possible to connector (generally within 10mm)
- Filter capacitors: Place on MCU side of series resistors

High-Current Paths:

- Minimize loop area for PWM outputs and gate driver returns
- Place gate driver ICs close to power MOSFETs
- Use ground plane stitching vias near high di/dt paths

5.2 Routing

Power Supply Traces:

- Use wide traces or copper pours for VDD and VSS
- Use multiple vias (preferable one per ball pin) for transitions between layers

Return Current Paths:

- Provide continuous ground plane under signal traces
- Avoid splits in ground plane under high-speed signals
- Place stitching vias along ground plane edges

5.3 Ground Plane Design

A solid, continuous ground plane is essential for EOS protection as it provides low-impedance return path for transient currents, shielding for sensitive signals, and heat dissipation for power components.

Ground Plane Best Practices:

- Use dedicated ground layer(s) in multilayer PCBs
- Minimize cutouts and splits in ground plane
- Keep clearance around vias to ground plane minimal (5-10 mils) to maximize copper area
- Use ground plane as reference for all high-speed and analog signals

Ground Connections:

- Connect all VSS pins of MCU directly to ground plane with multiple vias
- Use via stitching (grounded vias) around perimeter of MCU footprint
- Provide separate low-inductance path from power supply ground to MCU VSS
- Chassis ground (if present) connects to PCB ground through high-voltage capacitor (1nF/2kV) and parallel spark gap or TVS

5.4 EOS-Specific Layout Considerations

Power Sequencing Support:

- Route power supply enable signals with low impedance to minimize delay
- Place power sequencing IC close to regulators
- Use separate traces for each power domain to monitoring circuitry

Connector Design:

- Implement VSS-first connection by using longer ground pins in connector
- Place ground pins at corners/ends of connector

Copyright © 2026 Texas Instruments Incorporated

- Use dual ground pins at entry points

5.5 Manufacturing and Assembly EOS Prevention

EOS events can occur during board assembly and manufacturing processes. Understanding these risks and implementing proper controls is essential for high-volume production.

5.5.1 Board Assembly EOS Sources

Common EOS sources during PCB assembly include:

• **Incorrect Component Assembly:** Misaligned components, reversed polarity, or wrong component placement can create overstress conditions. Use silk-screen markings clearly showing pin 1 orientation, polarity indicators for capacitors and diodes, and component outlines matching actual footprints.

• **Equipment Filtering Issues:** Soldering equipment, reflow ovens, and heat guns can introduce electrical fast transients (EFTs) onto power lines. These transients can couple into sensitive circuits during assembly. Use filtered AC power for all assembly equipment, especially soldering irons and heat guns.

• **Equipment Grounding:** Open ground connections in assembly equipment can result in floating voltages appearing on tool tips. A case study found 60VAC on a soldering iron tip due to an open ground connection, causing repeated device failures. Verify proper grounding of all equipment before use.

• **Reflow Temperature Excursions:** Overheating during reflow can cause EOS damage through several mechanisms:, package delamination creating stress on bond wires, and junction temperature excursions. Monitor actual board temperatures during reflow profiling.

• **Charged Capacitors:** Discrete capacitors may retain charge from previous test or assembly steps. When installed on boards, this residual voltage can discharge into sensitive pins. Implement capacitor discharge procedures as necessary.

5.5.2 What to Look For During Manufacturing

To identify and prevent assembly-related EOS:

1. Equipment Inspection:

- Verify AC power filtering on all soldering equipment
- Test ground continuity on tool tips (should be <1Ω to earth ground)
- Use industrial-grade outlets with verified grounding
- Inspect power cables for damage

2. Assembly Process Verification:

- AOI (Automated Optical Inspection) for component polarity
- X-ray inspection for BGA/QFN alignment
- RPI (Reflow Process Inspection) for solder joint quality
- Verify silk-screen markings match component orientation

3. Temperature Monitoring:

- Attach thermocouples to representative boards during profiling
- Verify peak temperatures stay within component specifications
- Check for hot spots indicating inadequate thermal design

4. Incoming Component Inspection:

- Discharge capacitors before placement
- Verify component markings match BOM
- Inspect for physical damage or contamination

Copyright © 2026 Texas Instruments Incorporated

6 In-Circuit Test (ICT) EOS Mitigation

In-Circuit Test (ICT) is a critical step in PCB manufacturing that establishes temporary electrical connections to the PCB for programming MCU flash, conducting electrical tests, or performing quality control checks. However, ICT poses significant EOS risks that can lead to Electrically-Induced Physical Damage (EIPD) if not properly managed.

6.1 Hot-Plugging Risks

Hot-plugging refers to connecting or disconnecting electrical devices while power or signals are active on either side. This is a significant cause of EOS during ICT operations.

6.1.1 Hot-Plugging Failure Mechanisms

When connectors are mated with active signals present, several failure mechanisms can occur:

- Signal pins make contact before ground/power, causing transient currents
- Charge transfer between systems at different potentials (Charged Board Events)
- Current injection into powered-down devices through I/O pins
- Voltage spikes exceeding device absolute maximum ratings

6.1.2 Hot-Plugging Prevention

Best Practices:

- Ensure connectors are de-energized: Always de-energize and ground connectors before mating
- Use ICT equipment with controlled power sequencing
- Add series resistors (100Ω typical) on test points to limit transient currents

6.2 Power Sequencing During ICT

AM26xx and C2000 devices have specific power sequencing requirements that must be followed during ICT to prevent EOS damage.

6.2.1 Key Sequencing Requirements

- **Supply power before signals:** Always apply power to the device before applying signals to I/O pins. This ensures the device is properly powered and ESD protection structures are functional.
- **Follow device-specific sequencing:** Refer to device datasheet for proper power domain sequencing (core, I/O, analog domains)
- **Avoid floating inputs:** Ensure all I/O pins have defined logic levels or are tri-stated during power transitions

6.2.2 ICT Power Sequencing Violations

WARNING: ICT may power systems differently than operational design. For example:

- ICT powers only low-voltage components while high-voltage regulator normally provides power
- Different power rail activation order during ICT vs. normal operation
- Partial system power-up for specific test sequences

These scenarios can cause unintended power sequencing violations. Mitigation strategies:

- Analyze ICT power delivery paths vs. operational paths
- Ensure consistent voltage application sequence
- Implement sequencing delays in ICT software if needed
- Use voltage supervisors to monitor proper sequencing

6.3 Charged Board Events (CBE)

Charged Board Events (CBE) occur when static voltage potential exists between physically isolated electrical systems. When these systems are connected, a surge of current flows between the boards. The magnitude depends on the voltage difference and capacitance of components.

6.3.1 CBE Mechanism

CBE can cause significant damage because:

Copyright © 2026 Texas Instruments Incorporated

- Current magnitude can exceed ampere levels instantaneously
- Signal pins have limited current-handling capability
- Damage can occur even with relatively small voltage differences (< 10V)
- Board capacitance stores significant energy (C = nF to µF range)

Energy stored in capacitance: $E = ½CV^2$

For a board with 100nF capacitance at 5V potential difference:

$E = ½ \times 100 \times 10^{-9} \times 5^2 = 1.25\mu J$

This energy, though seemingly small, discharges in nanoseconds through connection pins, creating high peak currents that can damage sensitive I/O structures.

6.3.2 Mitigating High-Capacitance Charge Dissipation

High-capacitance nodes, such as power supply networks (VDD3V3) present a Charged Board Event (CBE) risk due to their capacity to store and discharge significant energy.

6.3.2.1 Reverse Charging Mechanism

- VSS quickly equalizes to the station's common ground voltage.
- VDD3V3 remains temporarily held at a large negative voltage due to its high node capacitance.
- MCU internal parasitic structures and ESD diodes forward-bias from VSS to VDD3V3.
- High surge currents rush through these sensitive internal paths, exceeding their current-handling capability and causing permanent silicon damage.

6.3.2.2 Board-Level Shunt Protection

To protect internal IC structures, designers should provide a low-impedance external bypass path to safely absorb the CBE current.

- Implementation: Place a board-level protection diode directly between VSS and the high-capacitance power rail VDD3V3
- Orientation: Connect the anode to VSS and the cathode to VDD3V3
- Diode Selection: The external clamp must feature a low turn-on forward voltage, such as a high-power Schottky barrier diode
- Operation: During a negative CBE, the external Schottky diode turns on before the internal silicon ESD structures. This shunts the destructive surge current away from the IC, safely dissipating the energy across the board-level component.

6.4 VSS-First Connection Strategy

The primary mitigation strategy for CBE and general ICT EOS protection is implementing VSS-first (ground-first) connections. This ensures ground reference is established before signal or power pins make contact.

6.4.1 VSS-First Design Principle

Fundamental Principle:

VSS (ground) pins should make contact FIRST during connector mating because:

- Ground planes can handle large surge currents without damage
- Establishes common reference potential before signal transfer
- Minimizes voltage difference between systems
- Provides return path for transient currents
- Reduces risk of signal pin damage during CBE

6.4.2 Implementation Methods

Several physical design approaches can implement VSS-first connections:

Method	Implementation Details
Longer VSS Pins	Design connector with VSS pins 1-2mm longer than signal/power pins
Bed-of-Nails Fixtures	Use taller VSS test points (0.5-1mm taller) in ICT fixtures

Copyright © 2026 Texas Instruments Incorporated

Method	Implementation Details
Dual VSS Placement	Place VSS pins at both ends of connector (corners/ends contact first)
Recessed Signal Pins	Slightly recess signal/power pins relative to VSS pins

Table 3; ICT Implementation methods

6.5 Manual Connector Protection

Manual connectors and exposed headers are particularly vulnerable to ESD and EOS events during handling and connection. These require additional protection beyond VSS-first design.

6.5.1 Protection Techniques

- ESD protection diodes: Place TVS diodes at connector entry points
- Series resistors: Add 100-330Ω resistors on exposed signal lines
- RC filters: Implement RC low-pass filters for slower signals
- Conformal coating: Apply protective coating over exposed headers
- Connector shields: Use metal shells connected to ground

✓ Recommendation: For field-accessible connectors on AM26xx and C2000 systems, implement multi-layer protection: VSS-first mechanical design + series resistors + TVS diodes.

Copyright © 2026 Texas Instruments Incorporated

7 External Protection Components

7.1 TVS Diode Selection

Transient Voltage Suppressor (TVS) diodes are the primary protection device for fast transients and ESD events.

7.1.1 Key Parameters:

1. Standoff Voltage (V_standoff or V_RWM): Maximum voltage where TVS remains non-conducting. Must be greater than maximum signal or supply voltage. Typically choose 20-30% above operating voltage.

2. Breakdown Voltage (V_BR): Voltage where TVS begins to conduct significantly. Specified at test current (usually 1mA). Should be below absolute maximum rating of protected pin.

3. Clamping Voltage (V_clamp): Actual voltage across TVS during surge event. Specified at peak pulse current (often 1A or 8A for ESD events). Critical parameter: must be less than abs max rating.

4. Peak Pulse Current (I_PP): Maximum surge current TVS can handle. 8/20µs pulse for power surges, 1ns rise for ESD. Choose based on expected transient energy.

5. Capacitance: Junction capacitance affects high-speed signals. Low-capacitance types available for >10MHz applications. Typical: 15pF to 150pF depending on voltage rating.

7.1.2 Unidirectional vs Bidirectional Usage:

- Unidirectional: For signals that are always positive relative to ground (e.g., power supplies)
- Bidirectional: For signals that can swing positive and negative (e.g., differential interfaces, AC-coupled signals)

7.1.3 Placement:

- Mount as close as possible to protected pin or connector **(<10mm**)
- Keep trace inductance low (short, wide traces)
- Connect directly to ground plane with multiple vias **(at least 2x**)

7.2 Filter Design

RC filters provide both EOS protection and EMI immunity by limiting slew rate and attenuating high-frequency transients.

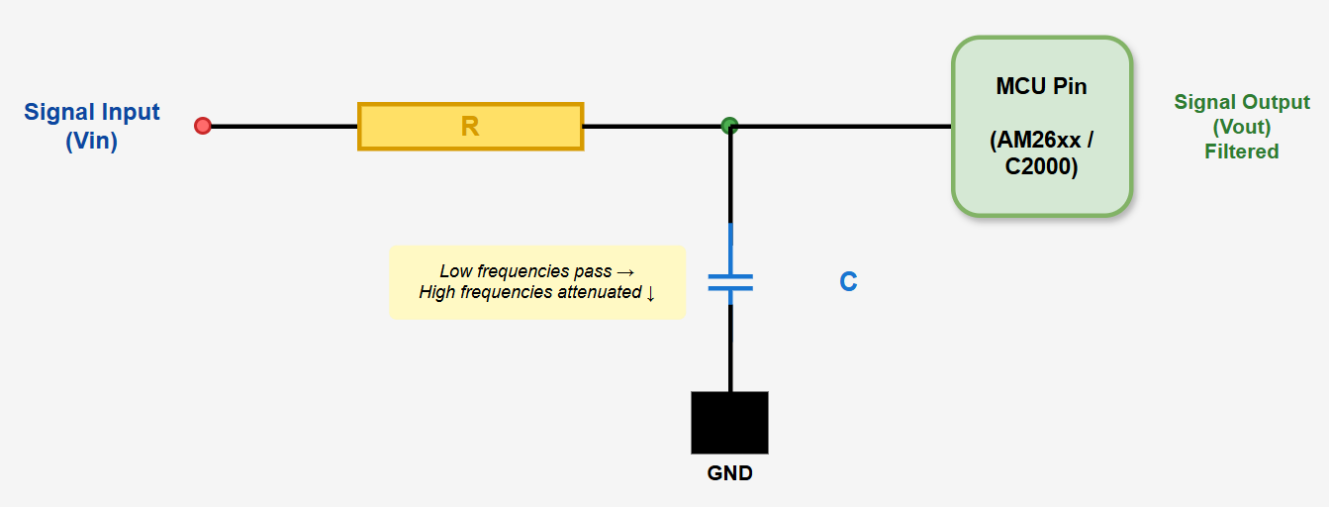


Figure 3; Filter Design

Cutoff frequency: f_c = 1 / (2π × R × C)

Design Considerations:

1. Cutoff Frequency Selection:

- Should be 3-10x higher than maximum signal frequency

Copyright © 2026 Texas Instruments Incorporated

- For digital signals: f_c > 10 × f_signal
- For analog signals: f_c = 2-3 × f_signal (to preserve bandwidth)

2. Resistor Value:

- Limited by acceptable voltage drop during logic transitions
- For 3.3V logic with 4mA drive: R < (3.3V - 2.4V) / 4mA = 225Ω
- Typical range: 22Ω to 100Ω for digital signals, 1kΩ to 10kΩ for analog inputs

3. Capacitor Value:

- C7R or X7R ceramic for stability over temperature
- Typical range: 100pF to 10nF
- Consider input capacitance of MCU pin (typically 5-10pF)

7.3 Voltage Clamping Solutions

When ESD diode current limits are likely to be exceeded (e.g., during power cycling with external signals active), external voltage clamping is required.

Zener Diode Clamping:

Placed across power supply rail to clamp voltage during back-powering.

Zener voltage selection: V_Z = Nominal VDD + 10-20%

Example: For 3.3V rail, use 3.6V or 3.9V Zener

Example calculation:

If external circuit can source 10mA into VDD through ESD diodes:

P_zener = V_Z × I = 3.6V × 10mA = 36mW

Choose Zener rated for 200mW (SOD-323 package) for safety margin

Shunt Regulator Clamping:

For higher currents or tighter voltage regulation, use shunt regulator (e.g., TLV431).

Advantages over Zener:

- Tighter voltage tolerance (±0.5% vs ±5%)
- Lower dynamic impedance
- Can handle higher currents (up to 100mA)

Set clamp voltage with resistor divider: V_clamp = V_ref × (1 + R1/R2)

Where V_ref = 1.24V for TLV431

For 3.45V clamp: 3.45V = 1.24V × (1 + R1/R2), R1/R2 = 1.78

Choose R2 = 10kΩ, R1 = 17.8kΩ (use 18kΩ standard value)

Parameter	TVS Diode	Zener Diode	Shunt Regulator
Response time	<1ns	<1ns	~1µs
Peak current	Very high (A)	Moderate (mA)	Moderate (mA-100mA)
Voltage tolerance	±5-10%	±5%	±0.5-2%
Best for	Fast transients	DC clamping	Precision clamping

Table – 4 ; Clamping Solutions

Copyright © 2026 Texas Instruments Incorporated

8 Design Examples and Case Studies

8.1 Case Study: Insufficient VDD/VSS Plane Connections

Device: AM2634

Failure Mode: VDDS33 shorts to VSS in multiple I/O cells and power rail capacitors

Problem:

Physical failure analysis confirmed similar failure signatures showing VDDS33 shorts in similar areas of the die. Optical and IR imaging showed metal flashover on VDD (R9), VDDS33 (R15), VDDA33 (P9) versus VSS.

Root Cause Investigation:

The customer PCB design had insufficient copper connections to VSS (PGND) and VDD (VCC1V2LV) planes underneath the AM2634. The planes connecting from outside the AM2634 area to inside had inadequate copper width, insufficient to reliably handle >2A inrush current required by AM2634. During power-up, large inrush current created unexpected voltage differentials and ringing transients in power planes, impacting supply voltages and causing voltage stress on I/O cells. Comparison with TI EVM (TMDSCNCD263) showed customer board had significantly less copper area for current distribution.

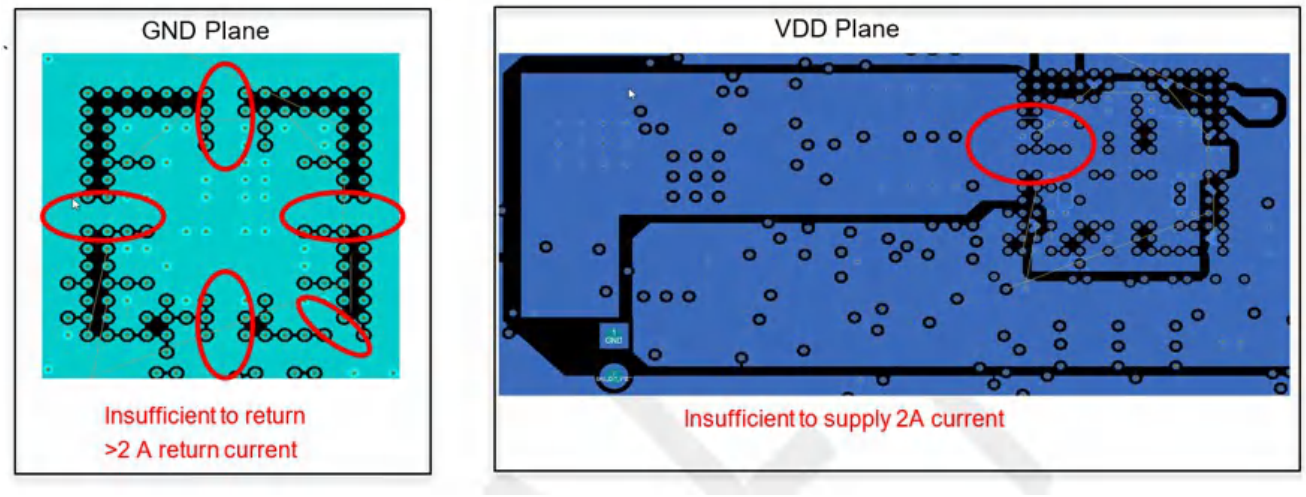


Figure 4; Layout with Issues

Corrective Actions:

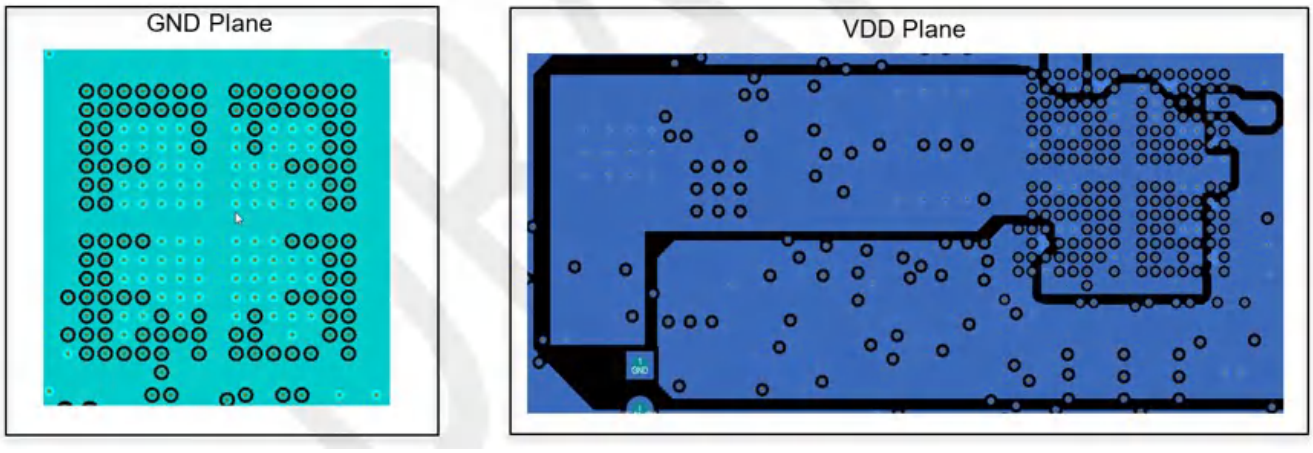


Figure 5; Reference EVM Layout

Copyright © 2026 Texas Instruments Incorporated

Decreased clearance between vias and planes to allow copper to spread between vias. Flooded as much area as possible with copper in VDD and VSS planes under device. Redesigned PCB to match TI EVM reference design copper distribution patterns. Verified current-carrying capability >2A for both VDD and VSS connections.

Results:

This case demonstrates the critical importance of adequate power distribution network design. EOS experts confirmed that insufficient grounding can account for failures observed. The failure location consistency (similar areas in multiple returns) indicated environmental stress rather than manufacturing defect.

Design Lesson: Power plane copper must be sized for worst-case inrush current, not just steady-state current. Reference designs from TI EVMs provide proven power distribution layouts.

8.2 Case Study: Invalid PORz Sequencing Causing I/O Buffer Shoot-Through

Device: AM2634

Failure Mode: VDDS33 and VDDS18 shorts to VSS

Problem:

The PORz (Power-On Reset) signal violated AM263x datasheet requirements in two ways.

Problem 1 - Diode on PORz Path: A diode placed between POW_RESET signal and PORz pin allowed PORz to rise >0.5V before VCC1V2LV (VDD) fully ramped to 1.2V. Per AM263x datasheet, PORz V_IL (maximum) = 0.5V, meaning PORz had potential to be read as logic high before AM2634 VDD reached valid 1.2V level.

Problem 2 - Slow PORz Rise Time: PORz signal had very slow rise time (multiple milliseconds), spending extended time in unknown state between V_IL (max) and V_IH (min): 0.5V to 1.35V.

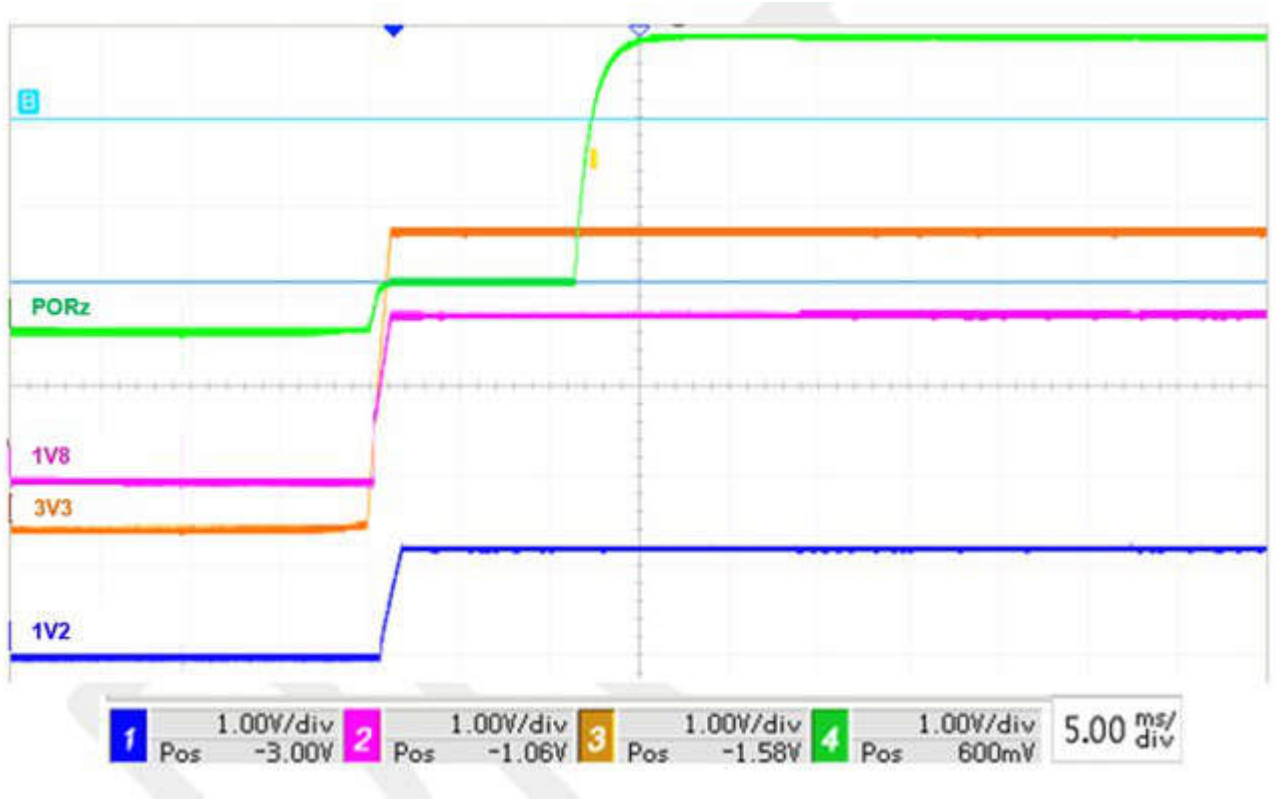


Figure 6;Power Up Sequence

Root Cause Investigation:

The TX block diagram shows: Level Shifter (1.8V) to Pre-driver (1.8V) to I/O Driver (VDDIO).

Copyright © 2026 Texas Instruments Incorporated

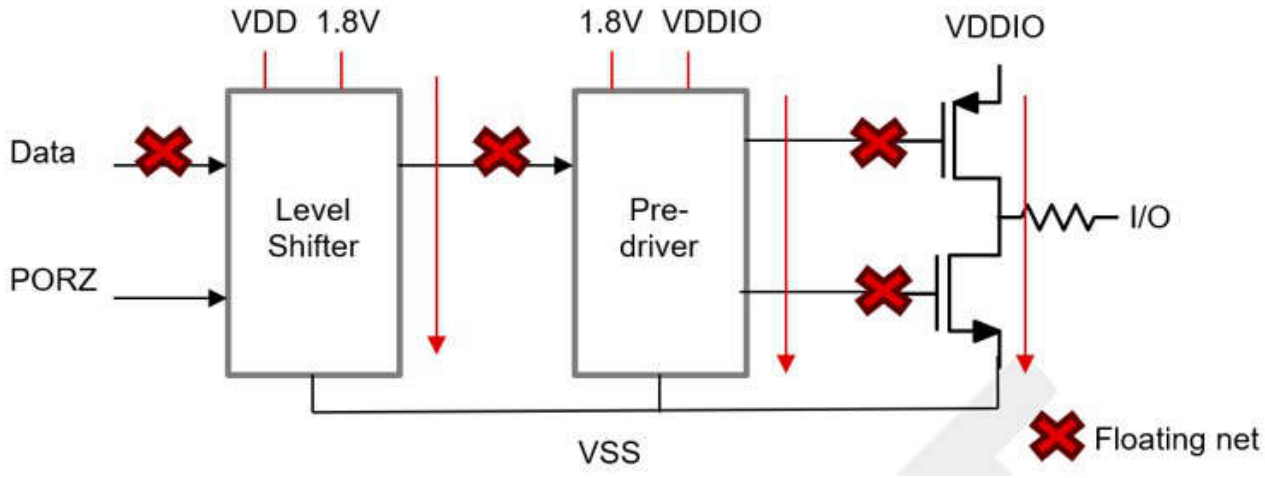


Figure 7; Internal Gate Driver Circuit

When PORz rises before VDD is valid, level shifters become un-gated with floating inputs causing short circuit current (VDDS18 to VSS).

Level shifter outputs reach intermediate levels, driver gates float causing short circuit current (VDDIO to VSS). These shoot-through currents are transients, but poor PDN (Power Distribution Network) causes voltage buildup.

Combined with insufficient copper voltage stress leads to EOS failure.

When PORZ gates the level shifter before VDD is valid, all stages enter unknown states with high current flow.

Corrective Actions:

Remove diode between POW_RESET and PORz pin. If POW_RESET is 3.3V logic, connect directly to PORz. If multiple Power Good signals combined, use logic AND gate to ensure all signals high before PORz assertion. Use driven signal for PORz with stronger/faster rise time to minimize time in indeterminate voltage range.

8.3 Case Study: Isolator Output Enable Causing Signal Before Valid Reset

Device: AM2634

Failure Mode: Shoot-through current on I/O NMOS/PMOS transistors causing VDDS33/VDDS18 shorts to VSS

Problem:

Pin A7 (UART RX input to AM2634) received active signal before valid PORz release. A7 was connected through ISO7741 digital isolator. ISO7741 Side 1 powered by VCC3V3LV (AM2634 3.3V rail), Side 2 powered by P3V3s. Both sides output enables (EN1, EN2) connected directly to respective power rails. A7 is NOT a fail-safe I/O pin on AM2634.

Root Cause Investigation:

Power sequencing violation occurred during board power-up:

- VCC3V3LV ramps before VCC1V2LV (AM2634 core VDD reaches 1.2V),
- ISO7741 EN1 tied to VCC3V3LV, so output driver (OUTD) enabled immediately when VCC3V3LV present,
- Nothing prevents ISO7741 from driving BATMCI_AC_LV_SCI_RX high, applying 3.3V to AM2634 pad A7,
- This occurs BEFORE AM2634 power rails valid and BEFORE PORz released,
- AM2634 I/O buffers in unknown state (not properly reset), leading to shoot-through current,
- Shoot-through current flows through NMOS/PMOS driver transistors: VDDS33 and/or VDDS18 to VSS.

Physical failure analysis confirmed NMOS/PMOS driver damage at the transistor level, consistent with shoot-through current during invalid reset conditions.

Corrective Actions:

- Connect ISO7741 Side 1 Enable (EN1) to valid AM2634 PORz signal instead of VCC3V3LV.

Copyright © 2026 Texas Instruments Incorporated

- This ensures AM2634 I/O buffers in known state (turned off) before ISO7741 activates UART signal.
- PORz will only go high after all power rails valid, preventing premature signal assertion.
- Apply same principle to all isolators and buffers driving AM2634 inputs.
- By gating the isolator enable with PORz, signals cannot reach AM2634 pins until the device has completed power-on reset with valid supply voltages.

This eliminates the shoot-through current path that caused I/O driver damage.

8.4 Case Study: Manufacturing Test Process Improvements

Device Family: F280025 - C2000 Real-Time MCU

Failure Mode: EOS/EIPD damage during ICT/FCT (In-Circuit Test / Functional Circuit Test)

Problem:

One of the customers experienced EOS/EIPD failures with F280025. Failure analysis confirmed device damage on VDD/VSS or signal pins consistent with EIPD due to EOS events.

Issue was root-caused to board design and manufacturing test process issues.

Board Design Issues:

1. VDD connections with current load limitations (insufficient copper)
2. VSS connections with current load limitations,
3. PORz sequencing issues
4. Output enables signals tied to PORz without proper validation.
5. Manufacturing Test Issues: Hot plugging (connecting test fixtures while power/signals active),
6. Power sequencing violations during ICT/FCT not matching datasheet requirements,
7. Insufficient VSS-first connections (test fixture ground pins not extended),
8. Charged Board Events (CBE) during fixture connection.

Corrective Actions:

Two primary manufacturing line improvements:

(1) Ground Pin Extension - Extended ground pin on connector for manufacturing testers to application board.

- Ensures VSS-first connection during fixture attachment. Mitigates Charged Board Event (CBE) damage.

(2) Power Sequence Correction - Updated power sequence to eliminate hot-plugging. Corrected power-up/down sequence to match TI datasheet requirements.

- Ensured solid ground connection before applying power. Applied power to connector power pins before applying signals to other pins.

Manufacturing test processes are a critical EOS risk factor. Hot-plugging, power sequencing violations, and inadequate grounding during ICT/FCT can cause device damage even when application board design is correct. Test fixture design deserves same attention as product design. Improvements proven on one product line must be systematically applied across all products to prevent repeated failures.

Copyright © 2026 Texas Instruments Incorporated

9 Summary and Recommendations

Electrical Overstress (EOS) protection for AM26xx and C2000 microcontrollers requires a comprehensive, multi-layer approach addressing power supply design, I/O interface protection, PCB layout, and manufacturing test procedures.

9.1 Key Takeaways

1. ESD Diode Current Specification: The ±2mA maximum continuous current through on-chip ESD diodes is a thermal limit. External protection must prevent this limit from being exceeded.
2. Power Supply Interactions: LDO selection must consider current sink capability. Ultra-low power LDOs require external voltage clamping to prevent supply voltage boost from ESD diode conduction.
3. Power Sequencing: Strict adherence to device-specific power sequencing prevents latch-up and EOS during power transitions. Core voltage must establish before or simultaneously with I/O voltage.
4. ICT Protection: In-Circuit Testing requires VSS-first connections, controlled power sequencing, and elimination of hot-plug conditions to prevent Charged Board Events (CBE) and related EOS.
5. Multi-Layer Defense: No single protection method is sufficient. Combine series resistors, TVS diodes, filters, and proper PCB layout for robust EOS immunity.

9.2 Design Checklist for AM26xx/C2000 Systems

Power Supply:

- Power sequencing verified per datasheet requirements
- External voltage clamp added if using ultra-low power LDO
- Voltage supervisor circuits monitor all power rails

I/O Interfaces:

- Series resistors on signals that can exceed supply voltage
- TVS diodes at connector entry points
- RC filters on analog inputs
- Communication interfaces properly terminated

PCB Layout:

- Protection components placed at board boundaries
- Solid ground planes implemented
- Current loops minimized
- Guard rings around sensitive analog sections

ICT Procedures:

- VSS-first connector design implemented
- Hot-plug conditions eliminated
- ICT power sequencing matches operational sequencing
- Test fixtures include series resistors on signal paths

Copyright © 2026 Texas Instruments Incorporated

10 References

1. Texas Instruments, *AM263x Sitara™ Microcontrollers with Real-Time Control*, datasheet.
2. Texas Instruments, *AM261x Sitara™ Microcontrollers*, datasheet.
3. Texas Instruments, *TMS320F2838x Real-Time Microcontrollers*, datasheet.
4. Texas Instruments, *TMS320F28004x Real-Time Microcontrollers*, datasheet.
5. Texas Instruments, *ESD Diode Current Specification*, application report.
6. JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing - Human Body Model (HBM)
7. JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method
8. IEC 61000-4-2, Electromagnetic compatibility - Testing and measurement techniques - Electrostatic discharge immunity test
9. Texas Instruments, *System-Level ESD Considerations Application Report* , application report.
10. Boxleitner, W., Electrostatic Discharge and Electronic Equipment, IEEE Press, 1988

Copyright © 2026 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025