Application Note

Understanding Polling Mode Operation and Interrupt Behavior of the TIC12400-Q1

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Abstract

The TIC12400-Q1 is a 24-channel multi-switch detection interface designed for 12V automotive applications. This application report addresses two aspects of device operation that are not fully elaborated in the datasheet alone: the internal polling cycle architecture, including its timing, sequencing, and register update behavior — and the /INT pin leakage current characteristics relevant to spurious-interrupt risk assessment. The information presented here is derived from field application discussions and TI engineering evaluations, and is intended to supplement the TIC12400-Q1 datasheet.

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1 Introduction

The TIC12400-Q1 provides 24 configurable input channels (IN0–IN23). Each channel can be independently assigned to digital switch detection (comparator mode) or analog voltage measurement (ADC mode). In either mode the device operates on a periodic polling cycle: wetting current is applied to all enabled channels, each channel is sampled in sequence, and the results are stored in on-chip status registers. The host microcontroller reads these registers via SPI and optionally receives an interrupt on the /INT pin when a state change is detected.

The device supports two primary operating modes:

- Polling Mode: The device samples all enabled channels once per configurable polling interval and then remains idle until the next interval begins.
- Continuous Mode: The device continuously samples all enabled channels with no idle period between cycles.

This document focuses on Polling Mode, which is the most commonly used configuration in automotive body electronics applications.

NOTE: Unless otherwise noted, all timing values referenced in this document apply to Polling Mode operation.

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2 Polling Mode Operation

2.1 Polling Cycle Architecture

Each polling cycle consists of three distinct phases, executed in order:

Phase	Name	Description
1	Wetting Current Active	At the start of the polling interval, wetting current is simultaneously enabled on all channels that have a non-zero wetting current setting. The current remains active for the programmed polling active time.
2	Sequential Sampling	After the wetting current active time, the internal MUX connects each enabled INx channel to the ADC or Comparator one at a time. Each channel is sampled for Tadc or Tcomp respectively, and its result register is updated immediately. Channels are sampled in order from IN0 to IN23, skipping disabled channels.
3	Idle	Once all enabled channels have been sampled, the wetting current is disabled and the device remains idle until the next polling interval begins. The duration of the idle phase equals the programmed polling period minus the time consumed by phases 1 and 2.

Table 1. TIC12400-Q1 Polling Cycle Phase Sequence

An important consequence of this architecture is that the wetting current is not active during the idle phase. External loads driven by the wetting current source see a pulsed stimulus, not a DC stimulus. System-level designs that rely on wetting current for sensor excitation must account for this duty cycle.

2.2 Polling Timing Parameters

Table 2 summarizes the key timing parameters governing the polling cycle.

Parameter	Symbol	Min	Typ	Max
Polling period (configurable)	T_{POLL}	—	8 ms (default)	—
ADC measurement time per channel	T_{ADC}	—	18 µs	25 µs
Comparator measurement time per channel	T_{COMP}	—	10 µs	18 µs
Time from TRIGGER bit set to first polling cycle start	T_{start}	200 µs	300 µs	400 µs

Table 2. TIC12400-Q1 Key Polling Timing Parameters

With a default polling period of 8 ms and up to 24 channels configured for ADC measurement (Tadc = 18 µs typical), the maximum time consumed by the sequential sampling phase is approximately 24 × 18 µs = 432 µs. This means the device is in the idle phase for the majority of each polling interval at the default setting.

NOTE: The polling period timer counts independently of the number of enabled channels. Enabling fewer channels shortens the sampling phase but does not change the programmed polling period.

2.3 Register Update Behavior During a Polling Cycle

The ADC_STATx registers hold the most recently sampled value for each INx channel. Understanding when these registers are updated is important for SPI read timing.

The following clarifications apply:

- Per-channel update: Each INx channel's ADC_STATx register is updated immediately after that channel is sampled within the current polling cycle — not at the end of the full cycle. Channels sampled earlier in the sequence will have current-cycle values while channels not yet sampled still hold the previous-cycle value.
- Atomic register reads: A SPI read always returns the complete, most recently stored register value. It is not possible to read a partially updated register. If a read occurs in the middle of a polling cycle, the host will receive a mix of current-cycle and previous-cycle values across different channels, depending on which channels have been sampled at the time of the read.

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- Register retention (R vs. RC types): Register bits with access type "R" retain their value after a SPI read. Register bits with access type "RC" (Read-Clear) are reset to their default value immediately after the read. Refer to the TIC12400-Q1 datasheet register map for the specific type of each bit.

NOTE: If the application requires all channels to reflect the same polling cycle, the SPI read should be timed to occur after the INT assertion that marks the end of a complete polling cycle, and before the start of the next cycle's sampling phase.

2.4 Device Startup Sequence and First Polling Cycle

After a device reset (hardware or software), the TIC12400-Q1 does not begin polling autonomously. The host microcontroller must first configure all required registers, then set the TRIGGER bit in the CONFIG register to logic 1. The device will start the first polling cycle 200–400 µs after the TRIGGER bit is set.

The startup sequence is as follows:

Step	Action	Notes
1	Apply power; wait for device POR to complete	Verify VS and VDD are within specification before proceeding.
2	Configure all channel and threshold registers via SPI	Set channel mode (ADC or Comparator), wetting current level, polling period, and interrupt configuration.
3	Set TRIGGER bit = 1 in CONFIG register	This activates wetting current and initiates the polling cycle timer.
4	Wait T_{start} (200–400 µs) for first polling cycle to begin	No valid ADC or comparator data is available until the first complete polling cycle has finished.
5	Wait for /INT assertion signaling end of first complete cycle	The /INT pin is asserted at the end of the first full polling cycle to indicate that baseline switch states have been captured. Valid data can be read from the ADC_STATx and SWITCH_STATx registers after this point.

Table 3. TIC12400-Q1 Device Startup Sequence

NOTE: The TIC12400-Q1 interrupt is state-change based, not edge-triggered. The "state" established at the end of the first polling cycle becomes the baseline for all subsequent interrupt comparisons. If an input has already transitioned to its active state before the first polling cycle completes, that active state will be stored as the baseline and no interrupt will be generated for that transition.

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3 /INT Pin Leakage Current and Interrupt Handling

3.1 /INT Pin Leakage Specification

The /INT pin is an active-low, open-drain output. It is normally held high by an external pull-up resistor connected to VDD and pulled low by the TIC12400-Q1 to assert an interrupt.

A common application concern is whether leakage current on the /INT pin could cause spurious triggering when the pin is in the de-asserted (high) state. The relevant datasheet parameter is the /INT output leakage current, tested with /INT pulled up to VDD:

Parameter	Min	Max	Unit
/INT output leakage current (pin pulled up to VDD)	−1	+1	µA

Table 4. /INT Pin Leakage Current Specification

The ±1 µA specification is a passing ATE parameter. In practice, the leakage current on the /INT pin is well within this range and is not a source of spurious interrupt triggering under normal operating conditions. The leakage current is three orders of magnitude smaller than the INx pin leakage (up to ±110 µA) and should not be confused with it.

NOTE: The ±110 µA leakage specification applies to the INx input pins only, not to the /INT output pin. These two specifications are independent and serve different design purposes.

3.2 Interrupt Generation and Configuration

The TIC12400-Q1 interrupt system is state-change based. The /INT pin is asserted when the device detects that the current sampled state of one or more monitored channels differs from the previously stored state. The interrupt is not generated by a signal edge on the INx pin directly, but by a difference between two consecutive polling cycle results.

Key behavioral characteristics:

- Configurable polarity: The interrupt can be configured to trigger on a low-to-high transition, a high-to-low transition, or either transition, on a per-channel basis.
- /INT assertion timing: The /INT pin is asserted at the end of a polling cycle in which a qualifying state change has been detected. It is de-asserted after the host performs a SPI read of the relevant status register (RC-type bits are cleared on read).
- First polling cycle behavior: The /INT pin is always asserted at the end of the first complete polling cycle after the TRIGGER bit is set. This is by design: the device has no prior state to compare against, so the first cycle's result is stored as the baseline and the interrupt is issued to notify the host that valid baseline data is now available.
- No analog edge detection: Signal rise time and fall time on the INx pins do not directly influence interrupt generation. What matters is the logic state (above or below the comparator threshold) at the moment the channel is sampled. A slow transition will be detected correctly provided the signal has settled past the threshold before the sampling window for that channel.

3.3 Startup Interrupt Behavior and Wakeup Signal Timing

A specific edge case arises when the TIC12400-Q1 is used to detect a wakeup signal that may have already occurred before or during the device startup sequence. Because the first polling cycle establishes the baseline, any INx pin that is already in its "active" state when the first polling cycle completes will have that active state stored as the baseline value. No interrupt will be generated for a transition that was captured as the initial state.

Consider a case where a wake signal drives an INx pin HIGH during the period between power-on and the first polling cycle completing. The TIC12400-Q1 will store HIGH as the baseline for that channel. If the signal is later removed (going LOW), the device will detect the HIGH-to-LOW transition and assert /INT as expected. However, the initial HIGH-to-active transition will have been missed from an interrupt perspective.

To avoid missed wakeup signals in latency-sensitive designs, consider the following:

- Ensure the MCU configures and triggers the TIC12400-Q1 before the expected wakeup signal window. The startup time from TRIGGER bit set to first valid data is 200–400 µS plus one complete polling cycle (e.g.,

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8 ms at the default setting). Total time from TRIGGER to first valid interrupt is therefore typically less than 10 ms at default settings.

- Read the SWITCH_STATx registers after the first /INT assertion to determine the current state of all channels. If a channel is already in the active state at startup, the application software should respond accordingly rather than waiting for an interrupt.
- Do not rely solely on interrupt-driven handling for wakeup detection. A register read following device initialization provides the ground-truth channel state and should be included in the startup routine.

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4 Summary

The TIC12400-Q1 polling cycle consists of three sequential phases: wetting current activation, channel-by-channel sampling, and an idle period. Wetting current is only active during the first phase and is off for the remainder of the interval. The polling period timer runs independently of the number of enabled channels, so reducing the active channel count lengthens the idle phase without changing the programmed period.

Each INx channel's result register is updated immediately after that channel is sampled, not at the end of the full cycle. A SPI read performed mid-cycle will therefore return a mix of current-cycle and previous-cycle values depending on where in the sequence the read falls. Register bits designated type RC are cleared on read; type R bits retain their value.

The device does not begin polling after reset until the host sets the TRIGGER bit in the CONFIG register. The first polling cycle starts 200–400 µS after that bit is set. The /INT pin is asserted at the end of the first complete cycle to signal that a valid baseline state has been captured. Because the interrupt system is state-change based, any input that is already in its active state when the first cycle completes will be stored as baseline and will not produce an interrupt for that initial transition. Applications with strict wakeup detection requirements should read the SWITCH_STATx registers after the first /INT assertion rather than relying on interrupt generation alone.

The /INT pin leakage current is specified at ±1 µA maximum (ATE-verified, pin pulled to VDD). This is not a risk for spurious interrupt triggering and should not be confused with the INx pin leakage specification of ±110 µA, which is a separate parameter applying to the input channels only.

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5 References

1. https://www.ti.com/lit/gpn/tic12400-q1

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