Application Note

Split LCD Configuration Using MSPM0L211x Microcontrollers

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Abstract

This application note describes the design and implementation of a primary and secondary liquid-crystal display (LCD) configuration using two MSPM0L211x microcontrollers (MCUs). This topology enables designers to drive high-segment-count displays that exceed the segment-driving capability of a single device, by synchronizing two MCUs over a simple three-signal interface. The Primary MCU generates all LCD timing signals; the Secondary MCU locks to those signals and drives additional LCD segments in perfect phase alignment with the Primary. Maintaining AC waveform integrity across both devices is critical to prevent DC bias on the LCD glass, which causes irreversible damage. The primary/secondary approach achieves this at a system cost approximately 20% lower than alternatives such as a dedicated LCD driver IC or a higher pin-count MCU.

Table of Contents

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1 Introduction

Many embedded applications require liquid crystal displays (LCDs) that show more information than a single low-pin-count microcontroller can drive. Examples include:

- Industrial energy meters with multi-tariff segment arrays
- Advanced thermostats displaying zone status, schedule, and fault indicators simultaneously
- Medical devices presenting patient data, waveform status, and alarm state on one glass panel
- Automotive instrument clusters combining speed, fuel, and telltale icons on a single display

The MSPM0L211x family integrates a hardware LCD controller capable of driving up to 4-mux or 8-mux displays. For systems that exceed this segment budget, the most straightforward designs — a higher pin-count MCU, a standalone LCD driver IC, or an I^2C/SPI LCD expander — each add cost, PCB area, or firmware complexity.

This application report presents an alternative: connecting two MSPM0L211x devices in a Primary/Secondary topology. The Primary MCU drives one portion of the display and generates all synchronization signals. The Secondary MCU receives those signals and drives the remaining segments in phase with the Primary, doubling the available segment count while adding only the cost of a second MSPM0L211x and three PCB traces.

2 Key Features

- Extends segment count beyond the physical limit of a single MSPM0L211x device
- Preserves AC waveform integrity and zero net DC bias across all COM/SEG pairs
- Uses only three GPIO signals for full inter-device synchronization
- No external oscillator or clock source required on the Secondary device
- Compatible with the MSPM0 SDK DriverLib initialization model

2.1 Scope

This document covers:

- System-level architecture and signal description
- Launchpad Hardware pin connections
- Software initialization sequence using MSPM0 DriverLib
- Timing of Synchronization signals

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3 Detailed Description

3.1 MSPM0L211x LCD Controller Overview

The MSPM0L222x integrates a full-featured LCD controller with the following characteristics:

- Supports static, 2-mux, 3-mux, 4-mux, 5-mux, 6-mux, 7-mux and 8-mux drive modes
- Internal charge pump for contrast control independent of VDD
- Low-power waveform mode practical for always-on display applications
- Internal low-frequency clock (LFCLK) sourced from the 32kHz oscillator or LFOSC
- Hardware-generated COM and SEG drive waveforms with no CPU intervention

In a standalone design the LCD controller generates *LCD_LFCLK*, *LCDSON* (frame start), and *LCD_EN* internally. In the primary and secondary configuration described here, those same signals are routed externally from the primary MCU to the secondary MCU, replacing the internal timing source of the secondary with that of the primary, thereby verifying synchronization.

3.2 Primary and Secondary Topology

3.3 Primary MCU

- Generates *LCD_LFCLK* — the low-frequency clock that clocks the LCD state machine (typically 32.768kHz or a divided submultiple)
- Asserts *LCDSON* — the frame synchronization pulse that marks the start of each LCD frame
- Drives *LCD_EN* — the peripheral enable signal that gates LCD operation on both devices
- Acts as the sole timing reference for the entire display system

3.3.1 Secondary MCU

- Bypasses its internal LFCLK source and accepts `LCD_LFCLK` from the Primary as an external clock input
- Locks its internal frame counter to the `LCDSON` pulse from the Primary
- Uses the `LCD_EN` signal from the Primary to enable and disable its LCD peripheral in step with the Primary
- Drives a separate set of segment pins connected to additional LCD glass segments

3.4 Why Synchronization is Critical

An LCD is a capacitive AC load. If the COM and SEG waveforms driven from two independent controllers are not in phase, a net DC voltage appears across some LCD cells. Even a small DC offset sustained over hours causes electrochemical degradation of the liquid crystal material, permanently reducing contrast and eventually destroying the display. The Primary/Secondary approach eliminates this risk by verifying that COM and SEG transitions on both devices occur on the same clock edge, producing zero net DC bias across every cell.

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4 System Architecture

4.1 Block Diagram

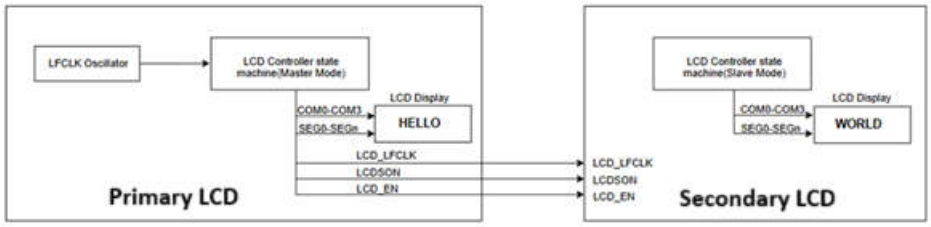

Figure 4-1. System Block Diagram of Split LCD Configuration

4.2 Signal Flow Diagram

The Primary MCU produces `LCD_LFCLK`. The LCD peripheral uses this clock to sequence the COM pins and generate `LCDSON` at the start of each frame. All three signals — `LCD_LFCLK`, `LCDSON`, and `LCD_EN` — are routed to GPIO output pins and connected directly to the corresponding input pins on the Secondary MCU.

The Secondary MCU's LCD peripheral is configured to accept an external clock and external frame synchronization. It never enables its internal oscillator for LCD timing. As a result, both LCD state machines advance on identical clock edges, and every COM/SEG waveform transition is simultaneous across both devices.

5 Hardware Implementation

5.1 Signal Interconnections

Table 5-1 details the signal connections between Primary and Secondary MCUs:

Table 5-1. Primary and Secondary MCU Pin Assignments

Signal Name	Primary Function	Secondary Function	Direction	Description
LCD_LFCLK	Output	Input	Primary -> Secondary	Low-frequency clock that drives the LCD state machine. Typically 32.768kHz
LCDSON	Output	Input	Primary -> Secondary	LCD Segment ON signal. Indicates the start of a new LCD frame and synchronizes the frame timing.
LCD_EN	Output	Input	Primary -> Secondary	LCD Enable signal. Controls the overall enable state of the LCD peripheral.
VSS (GND)	Common	Common	Bidirectional	Shared ground reference. Mandatory for proper signal integrity and timing accuracy.

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6 Theory of Operation

6.1 Clock Synchronization

The Secondary's LCD peripheral is configured to source its clock from the `LCD_LFCLK` input pin rather than the internal LFOSC. This makes the Secondary's LCD state machine a direct frequency Secondary of the Primary. Both devices advance one LCD clock cycle per rising edge of `LCD_LFCLK`. Because the clock is sourced from a single oscillator, there is no frequency deviation or phase accumulation between the two LCD controllers over time.

6.2 Frame Synchronization

`LCDSON` is a periodic pulse generated once per LCD frame by the Primary's LCD controller.

Both Primary and Secondary use this pulse to:

- Reset their internal frame counters to zero
- Begin the COM0 drive phase simultaneously
- Ensure that COM0, COM1, COM2, and COM3 transitions occur on the same LCD clock edge on both devices

Without `LCDSON` synchronization, even perfectly matched clock frequencies would allow the two COM sequencers to drift in phase over power cycles or temperature changes, eventually introducing DC bias.

6.3 Enable Synchronization

`LCD_EN` controls when each device's LCD peripheral is active. Using a single `LCD_EN` signal from the Primary verifies that:

- Both MCUs assert their LCD drive outputs simultaneously at startup, preventing any partial frame during which only one device is driving the glass
- Both MCUs de-assert simultaneously at shutdown, leaving no residual charge on the LCD glass
- The Secondary cannot inadvertently enable its LCD peripheral before the synchronization signals from the Primary are valid

6.4 COM and SEG Waveform Phase Relationship

When the three synchronization signals are correctly connected and the configuration parameters match (see Section 7.4), the COM waveforms from the Primary and Secondary are cycle-aligned. Any SEG pin on either device transitions only during the assigned COM phase, producing the correct biphasic AC drive waveform across every LCD cell. The net DC component across each cell is zero.

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7 Software Configuration

7.1 Recommended Start-Up Sequence

The initialization order is critical. The Secondary must be fully initialized and waiting for synchronization signals before the Primary's LCD peripheral is enabled. If the Primary is enabled first, the Secondary can miss the first `LCDSON` pulse and begin driving from an arbitrary frame offset, introducing a one-frame DC bias.

Recommended sequence:

1. Power up both MCUs (simultaneous power-on preferred; the Secondary's LCD peripheral remains disabled until `LCD_EN` is asserted by the Primary)
2. **On the Secondary:** configure and initialize the LCD peripheral in external clock mode; load segment memory; do **not** set the *LCDSON* or *LCD_EN* control bits in the Secondary's LCD registers — those are driven by the Primary's outputs
3. **On the Primary:** configure the LCD peripheral (do not enable yet); enable the LCD module which asserts *LCD_EN* and begins generating *LCD_LFCLK* and *LCDSON*.
4. Both devices are now running synchronized.

The Secondary's segment memory must be loaded with valid data before step 3. Once the Primary enables the LCD, both devices begin driving the glass immediately. Any uninitialized segment memory on the Secondary appears as display artifacts during the first frame.

7.2 Secondary Initialization Code

```
/* Configure IOs for Synchronization signals shared between master and slave, slaves gets synchronized these signals */
DL_GPIO_initPeripheralInputFunction(IOMUX_PINCM38, IOMUX_PINCM38_PF_LCD_LCDSON); //LCDSON -PA16
DL_GPIO_initPeripheralInputFunction(IOMUX_PINCM39, IOMUX_PINCM39_PF_LCD_LCDLFCLK); //LCDLFCLK -PA17
DL_GPIO_initPeripheralInputFunction(IOMUX_PINCM40, IOMUX_PINCM40_PF_LCD_LCDEN); //LCDEN -PA18

/* Enable slave mode  */
DL_LCD_enableExternalSync(LCD);

/* Write slave contents into MMRs */
LCD_showChar(LCD, 'W', gLCDPinPosition1);
LCD_showChar(LCD, 'O', gLCDPinPosition2);
LCD_showChar(LCD, 'R', gLCDPinPosition3);
LCD_showChar(LCD, 'L', gLCDPinPosition4);
LCD_showChar(LCD, 'D', gLCDPinPosition5);
```

7.3 Primary Initialization Code

```
/* Configure IOs for Synchronization signals shared between master and slave, master drives these signals */
DL_GPIO_initPeripheralOutputFunction(IOMUX_PINCM38,IOMUX_PINCM38_PF_LCD_LCDSON); //LCDSON -PA16
DL_GPIO_initPeripheralOutputFunction(IOMUX_PINCM39,IOMUX_PINCM39_PF_LCD_LCDLFCLK); //LCDLFCLK -PA17
DL_GPIO_initPeripheralOutputFunction(IOMUX_PINCM40,IOMUX_PINCM40_PF_LCD_LCDEN); //LCDEN -PA18

/* Write master contents into MMRs */
LCD_showChar(LCD, 'H', gLCDPinPosition1);
LCD_showChar(LCD, 'E', gLCDPinPosition2);
LCD_showChar(LCD, 'L', gLCDPinPosition3);
LCD_showChar(LCD, 'L', gLCDPinPosition4);
LCD_showChar(LCD, 'O', gLCDPinPosition5);

/* Master controls turn ON LCD Segments for both Master and slave */
DL_LCD_turnSegmentsOn(LCD);
/* Master controls the LCD Enable for both master and slave */
DL_LCD_enable(LCD);
```


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7.4 Updating the Display at Run Time

To update segment content at runtime, write to each MCU's segment memory independently over the normal application firmware path (for example, from a UART receive ISR or a periodic timer callback). The LCD hardware reads segment memory once per frame during the appropriate COM phase; no additional synchronization between the two MCUs is required for content updates. Each MCU manages its own segment data autonomously after the initial clock synchronization is established.

7.5 Configuration Parameters Must Match

The parameters in Table 7-1 must be identical between the Primary and Secondary. A mismatch on any of these fields causes COM sequencing or voltage-level incompatibilities that produce visible display artifacts or DC bias.

Table 7-1. Configuration Parameters - Must Match Between Primary and Secondary

Parameter	Primary Value	Secondary Value	Impact if Mis-match
muxRate	DL_LCD_MUX_RATE_4	DL_LCD_MUX_RATE_4	COM sequencing out of sync
biasMode	DL_LCD_BIAS_MODE_3	DL_LCD_BIAS_MODE_3	Voltage levels incompatible
waveMode	DL_LCD_WAVE_MODE_LOW_POWER	DL_LCD_WAVE_MODE_LOW_POWER	Waveform shape mismatch

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8 Launchpad Connections

Figure 8-1 shows the LCD Primary-Secondary connections using two MSPM0L211x launchpads, where the Primary MCU displays "HELLO" and the Secondary MCU displays "WORLD" on its LCD.

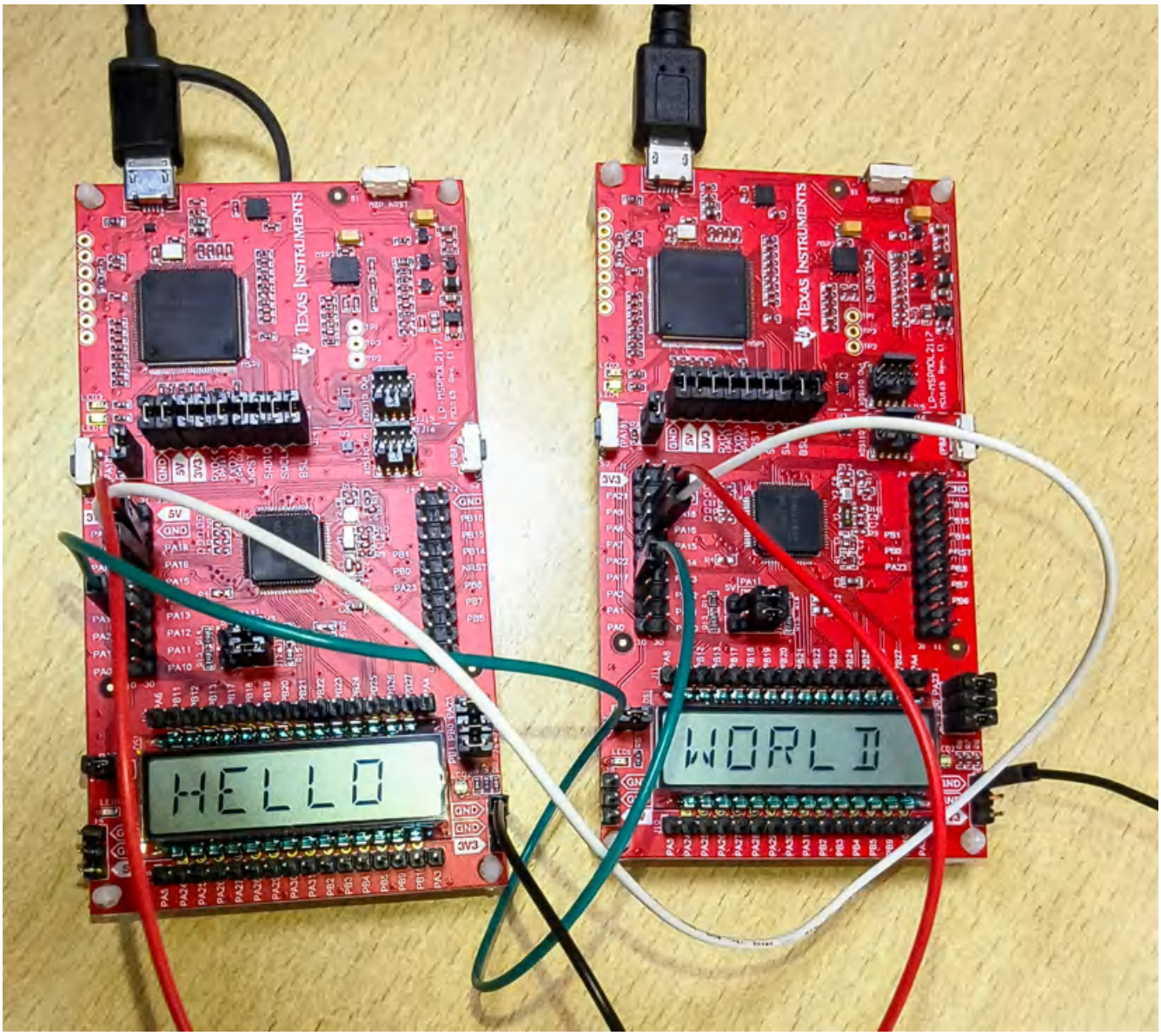

Figure 8-1. Launchpad Connections of Primary and Secondary MCU

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9 Timing of Synchronization Signals

Figure 9-1 shows the oscilloscope capture of `LCD_LFCLK`, `LCDSON`, and `LCD_EN` from the Primary output to Secondary MCU input.

Figure 9-1. Synchronization Signals Timing Waveform

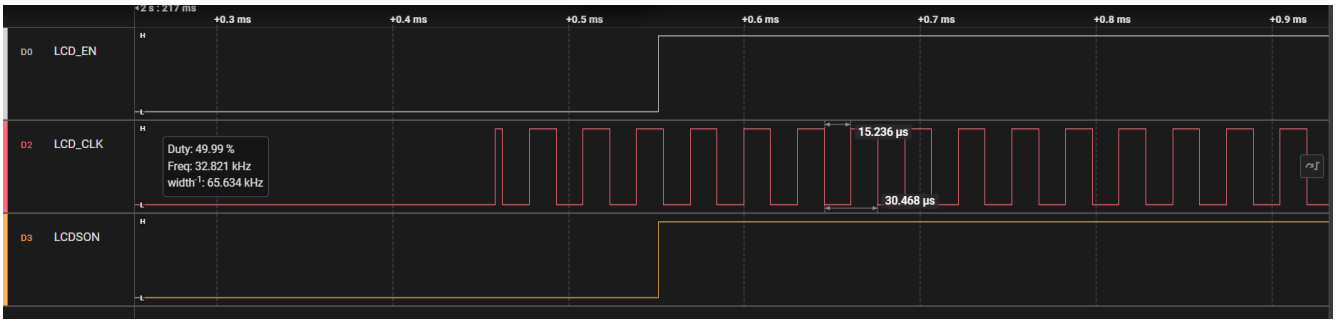

Figure 9-2. Zoom in Capture of Synchronization Signals

10 Cost Analysis

The Primary/Secondary approach achieves the same effective segment count as higher-cost alternatives at a lower total bill-of-materials (BOM) cost. Table 10-1 compares relative system cost normalized to the single MCU baseline.

Table 10-1.

Approach	Components	Relative Cost
Single MCU	1× MSPM0L211x	1.0×
Primary/Secondary	2× MSPM0L211x	1.8×
Larger MCU	1× Higher pin count	>2.0×

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11 Summary

The Primary/Secondary LCD configuration using two MSPM0L211x MCUs provides a cost effective, reliable method for driving high-segment-count LCD glass beyond the capability of a single device.

The critical success factors for this design are:

1. **Initialization order**: The Secondary must be fully configured and waiting before the Primary enables its LCD peripheral.
2. **Matched configuration**: muxRate, biasMode, and waveMode must be identical on both devices.
3. **Correct pin-mux**: Both devices must have their LCD synchronization pins routed to the correct IOMUX channels before the LCD peripheral is enabled.

When these conditions are met, the Primary/Secondary topology delivers cycle-exact phase synchronization, zero net DC bias on all LCD cells, and a system cost approximately 20% lower than the next most common alternative.

12 References

1. Texas Instruments, *MSPM0L2116/7 and MSPM0L1126/7 Mixed-Signal Microcontrollers*, datasheet.
2. Texas Instruments, *MSPM0L211x Technical Reference Manual*, technical reference manual.
3. Texas Instruments, *MSPM0L211x Evaluation Module*, user's guide.
4. Texas Instruments, *MSPM0L211x SDK DriverLib*, software development kit.

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