

Design Guidelines for UCC23711 Isolated IGBT/SiC-FET Gate Driver with Opto-Compatible Input and DESAT



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Abstract

In industrial drive design for industrial robots and servo drives robustness is non-negotiable. This application note delivers circuit design guidelines for the UCC23711 isolated single-channel gate driver, specifically tailored for engineers developing high-reliability 3-phase IGBT inverters. Beyond a foundational overview of the UCC23711 key parameters, this guide dives into optimizing input resistor configurations under component tolerance constraints, shows an implementation of desaturation (DESAT) protection and examines how to configure the DESAT protection time. Furthermore, the guide addresses gate drive optimization through active Miller clamping and configurable gate drive peak source and sink current settings, alongside considerations for supply decoupling and power consumption in both unipolar and bipolar gate drive supply configurations. The key design parameters are validated via empirical measurement data from a 3-phase IGBT inverter prototype at 550V DC bus voltage, providing detailed performance data on input current thresholds and hysteresis, propagation delays, IGBT switching slew rates, fault response timing with soft shut-down and gate drive supply currents.

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Trademarks

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2 Opto-Input Isolated Protection Gate Driver for SiC and IGBT

The UCC23711 and UCC23710 are galvanic isolated single channel gate drivers designed for SiC MOSFETs and IGBTs up to 1500VDC operating voltage. The input side is isolated from the output side with SiO₂ isolation technology, supporting up to 1.5kV_{PK} working voltage, 10kV_{PK} surge immunity and >300V/ns common-mode transient immunity. The UCC23711 and UCC23710 have up to ±5A peak source and sink current. Both devices include overcurrent protection and soft shut down, active Miller clamp, fault diagnostics and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness.

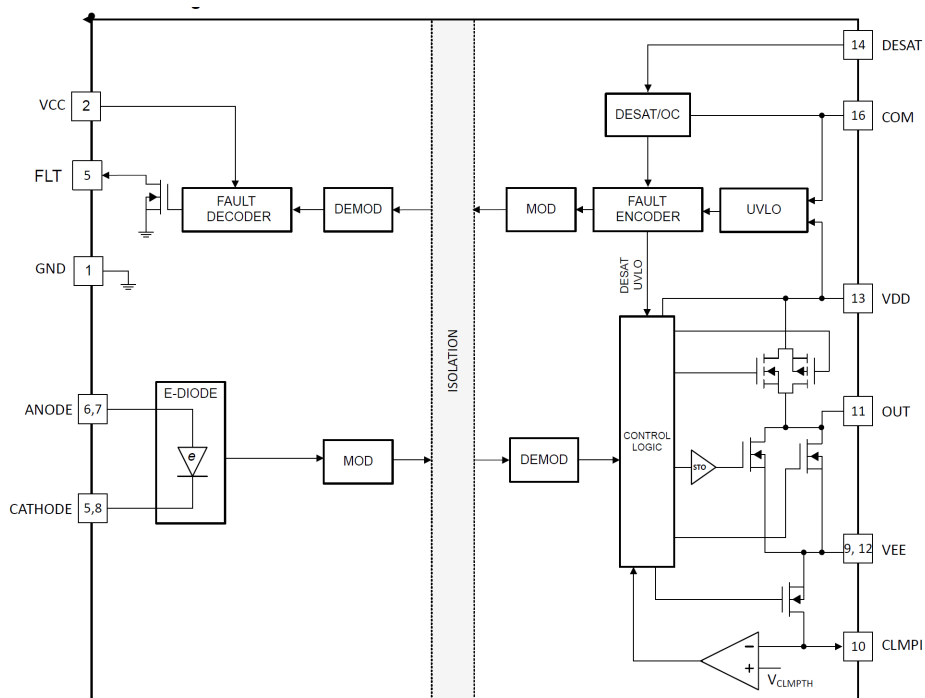


Figure 2-1. Block Diagram of UCC23711

The UCC23711 and UCC23710 devices feature state-of-the-art desaturation (DESAT) detection, with a fast detection time, and a fault reporting function to the low-voltage side MCU. In the event of a DESAT fault, the device triggers a soft turn-off, minimizing short-circuit energy and reducing overshoot voltage on the power switches. The UCC23711 offers a DESAT threshold of 6.5V, the UCC23710 offers a threshold of 9V to support a wide range of power switches. The DESAT function helps protect 3-phase inverters for applications like robotics and servo drives from short-circuits such as half-bridge shoot through, motor phase to phase short or a phase to Earth GND short.

The UCC23711 and UCC23710 low propagation delay (100ns maximum) and the 30ns (maximum) pulse/part skew help reduce dead time with 3-phase inverters to optimize power efficiency.

3 Three Phase IGBT Inverter Design Guidelines for UCC23711

3.1 Overview

The following figures show the schematic of the UCC23711 (U1) gate driver and the 1200V IGBT power module (Q1) used for testing and validation of the UCC23711.

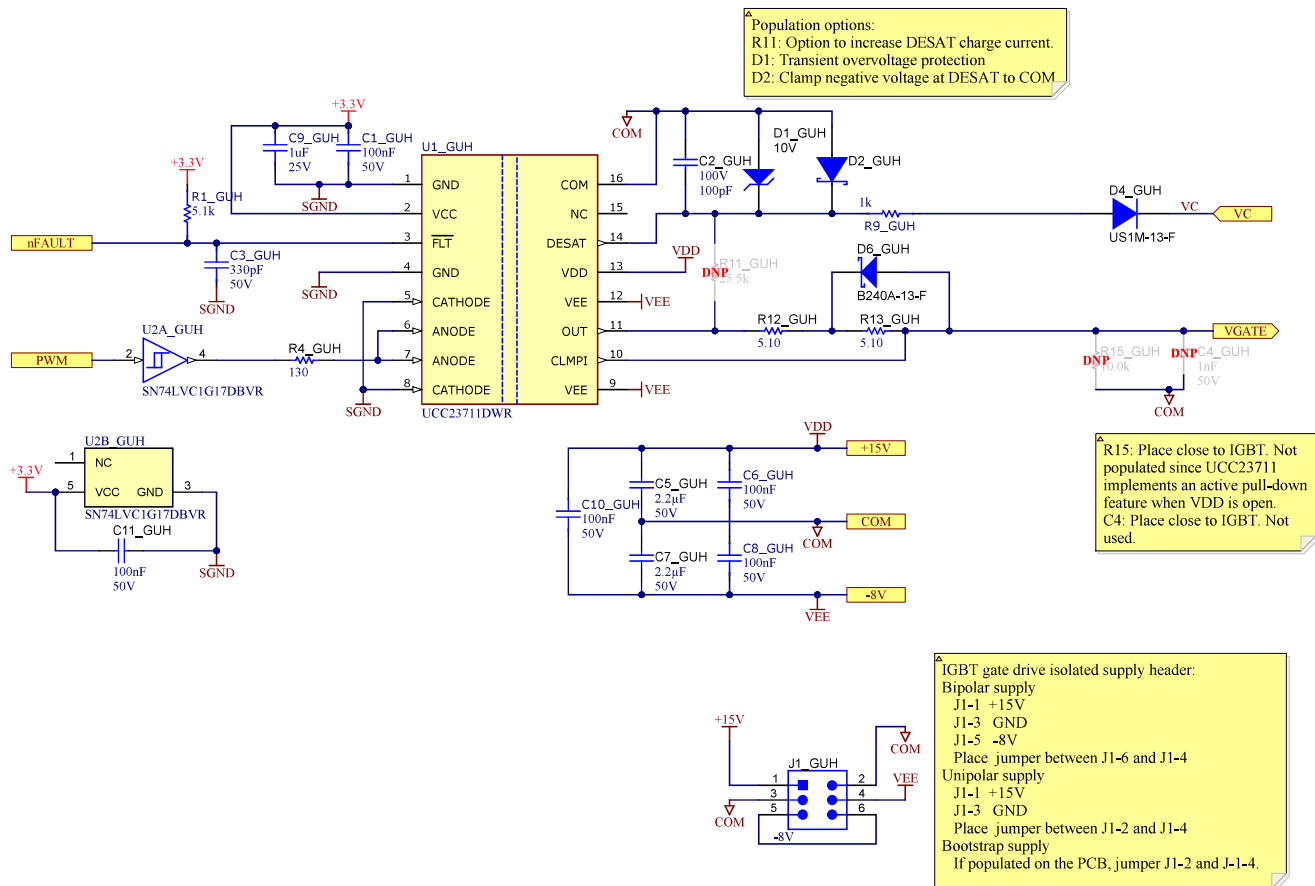


Figure 3-1. UCC23711 Schematic Phase U Top Gate Driver Example

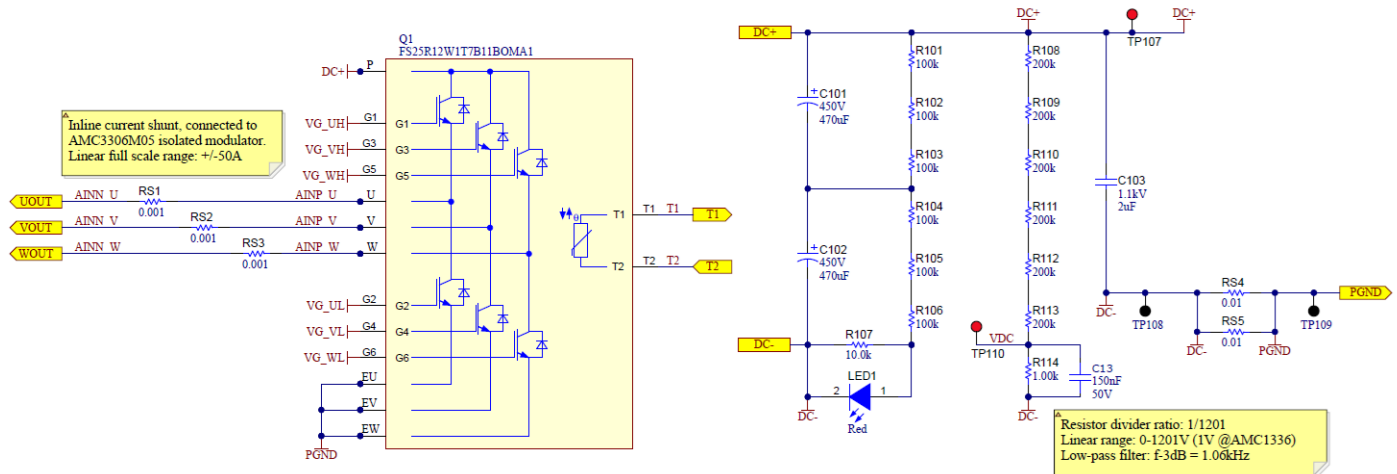


Figure 3-2. IGBT Module and DC Bus Schematic

A 1200V 6-pack IGBT power module Q1 in a 3-phase half bridge topology without a brake IGBT and with NTC was used. The IGBT module supports 25A continuous current and 50A peak current was used for the tests. The typical collector-emitter saturation voltage at 25°C is 1.6V at 15V across V_{GE} and 25A current. The typical gate threshold voltage is 5.8V, the gate charge is 0.395μC at 600V and V_{GE}=±15V, the internal gate resistor is typically 0Ω. When using a bipolar supply with 15V and -8V supply the corresponding gate charge is around 0.3μC, for a unipolar 15V supply is around 0.2μC. The gate charge impacts the bias supply power rating and decoupling caps. The turn-on delay time at 25°C is 35ns, the turn-off delay time is 190ns. This must be considered for the complementary PWM dead time setting.

In this design, the UCC23711 is selected due to the 6.5V DESAT threshold.

3.2 UCC23711 Input Current Resistor Configuration

The UCC23711 input resistor limits the current that flows into the e-diode when it is forward biased. The recommended operating range for the forward current is 5mA to 20mA (e-diode ON). The threshold current I_{FLH} is 1mA typ.

The UCC23711 operates with a single input resistor R4 at the anode, reducing BOM while still achieving high common mode transient immunity (CMTI) of minimum 300V/ns. The cathode is directly connected to the logic ground for best noise immunity. The input resistor R4 is chosen to 130Ω and meets UCC23711 minimum, typical and maximum forward current specifications at 3.3V nominal supply using the SN74LVC1G17 single Schmitt-Trigger buffer (U2). See the following table.

Table 3-1. UCC23711 Input Current Tolerances

Parameter	Unit	MIN	TYP	MAX	Notes
I _F	mA	5.4	10.8	15.8	Meets UCC23711 recommended forward current specs
R _{EXT}	Ω	128.7	130	131.3	1% tolerance
VCC	V	3.15	3.30	3.45	±5% tolerance
VOH _{LVC1G17} at VCC	V	2.7	3.1	3.45	VOH(MIN) at VCC(MIN) estimated at 4mA
V _F at I _F =10mA	V	1.4	1.7	2	UCC23711 datasheet SLVSKN4 – DECEMBER 2025

3.3 UCC23711 Gate Drive Turn-on and Turn-off Peak Current

The gate drive output resistors R12, R13 and the Schottky diode D6, placed in parallel to R13, as shown in the following figure. This allows a configurable turn-on and turn-off peak current. With the default configuration R12=R13=5.1kΩ and D6 populated the UCC23711 source and sink peak currents can be estimated for a bipolar supply bipolar +15V and -8V supply with VDD-VEE=23V:

$$I_{OUT, SOURCE} = \min \left[5A, \frac{VDD - VEE}{R_{OUTH} + R12 + R13 + R_{Gint}} \right] = 2.1A \quad (1)$$

where R_{Gint}=0 is the selected IGBT's internal gate resistance and R_{OUTH}=0.7Ω the UCC23711 output pull-up resistance for sourcing current.

$$I_{OUT, SINK} = \min \left[5A, \frac{VDD - VEE - V_F(D6)}{R_{OUTL} + R12 + R_{Gint}} \right] = 3.9A \quad (2)$$

where V_F(D6)=0.3V, R_{GINT,IGBT}=0 and R_{OUTL}=0.7Ω the UCC23711 output pull-down resistance for sinking current.

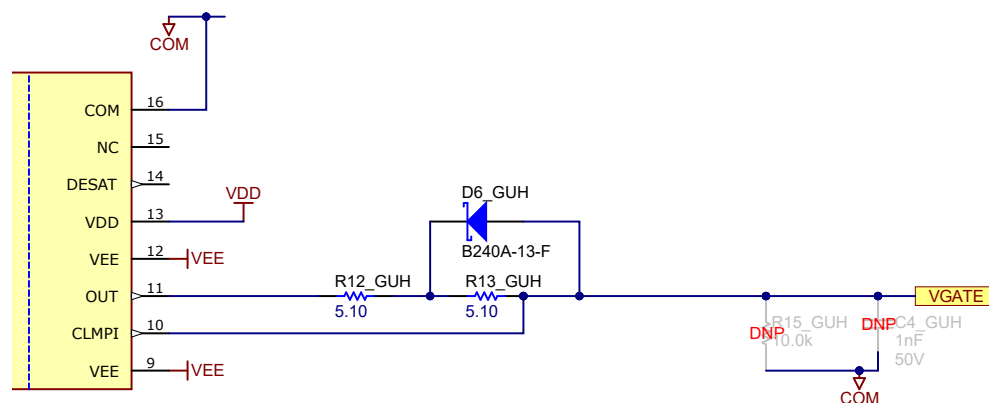


Figure 3-3. UCC23711 Gate Drive Circuit

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, the gate-driver current loop to the IGBT should be minimized.

The UCC23711 gate driver output stage implements an active pulldown feature to ensure the gate driver output pin is clamped to VEE when VDD is open. An optional 10k pull-down resistor R15 is placed close to the IGBT gate and emitter to discharge stray charges, for example when the connection between the gate driver and the IGBT fails, or when the gate drive supply powers up. Since the UCC23711 offers an active pull-down feature when VDD is off, R15 was not populated for the tests.

An option to place a capacitor C4 close to the IGBT gate and emitter has been provided to sink the additional charge originating from the Miller capacitance during the turn-on of top IGBT. Due to the additional capacitance, the effective input capacitance of the IGBT is $C4 || C_{GE}$, the gate charge required to reach the threshold voltage will be increased and the turn-on and off-times are slower. Since the UCC23711 offers an active Miller clamp, C4 is not populated.

3.4 UCC23711 Active Miller Clamp

The UCC23711 has an active Miller clamp function to add an additional low impedance path to prevent unintentional turn-on while the driver is in the OFF state. The IGBT gate potential is directly connected to the CLMPI pin.

3.5 UCC23711 Supply Decoupling and Requirements

3.5.1 Input Side

The supply voltage at VCC can range from 3V to 5.5V with respect to GND, thus supporting a direct interface for the UCC23711 fault feedback (FLT) to 3.3 V microcontrollers as well as a 5V legacy microcontrollers. A 100nF and a 1μF decoupling cap (C1 and C9) are placed close to the UCC23711 VCC and GND.

3.5.2 Output Side

A positive V_{GE} of typically 15 V is used to switch the IGBT well into saturation. For low power IGBTs, the Miller clamp functionality of the gate driver enables it to be operated with unipolar voltage (VEE connected to COM). For higher power IGBTs, negative values of V_{GE} such as -8V as used in the design are used to keep the IGBT turned off and to prevent it from unintentional conducting due to noise transients, particularly during short circuit faults.

100nF caps C10, C6 and C8 are placed close to VDD-VEE, VDD-COM and VEE-COM to filter out high frequency noise.

The capacitors C5 and C7 are chosen to 2.2μF 50V, intentionally lower than the recommended 10μF 50V MLCC capacitors per UCC23711 datasheet. The reason is that the gate charge of the selected IGBT (U1) is rather low 0.3μC along with a maximum desired PWM switching frequency of 16kHz. The minimum capacitance of C5 (X7R, 0805) assuming a negative 10% tolerance and 15V DC bias is around 1.2μF, for C7 (X7R, 0805) at -8V DC bias the minimum capacitance is around 1.7μF. The maximum voltage drop across C5 is 0.25V (15V bias)

and 0.17V (-8V bias) for C7, which is around 2% and within the tolerances of the 15V and -8V supply. For IGBTs with higher gate charges and tighter tolerances increase the decoupling capacitors respectively.

3.5.3 Output Supply Current

The power specification for a 15V unipolar and a bipolar +15V and -8V supply can be estimated from the UCC23711 VDD quiescent current and the IGBT's gate charge.

The UCC23711 VDD quiescent current is 2.3mA (TYP) and 4mA (MAX) for OUT=high and 2mA (TYP) and 3mA (MAX) for OUT=low. The VEE quiescent current is -1.8mA (TYP) at OUT=High and -1.5mA at OUT=Low.

The IGBT (Q1) gate charge Q_G at 600V DC-link and a bipolar 15V and -8V supply is around 0.3 μ C. The estimated average charge current is 4.8mA at 16kHz PWM and 2.4mA at 8kHz PWM. The total typical VDD supply current estimate is 6.95mA at 16kHz PWM and 50% duty cycle.

For a unipolar 15V supply the gate charge is around 0.2 μ C and the total supply current estimated at 16kHz PWM and 50% duty cycle is 5.35mA.

The maximum average supply current depends on maximum PWM, the maximum gate charge and the gate driver power supply and must be designed with enough margin.

3.6 DESAT Circuit Configuration

The DESAT pin threshold, $V_{DESATTH}$, is with respect to the UCC23711 COM pin, connected to emitter of the IGBT. The UCC23711 DESAT threshold is 6.5V typical. When the drive is in off state, the DESAT pin is pulled down by an internal MOSFET to prevent DESAT from triggering falsely, hence a pull-down resistor from the DESAT pin to the COM pin is typically not required.

When the driver is in the on state, an internal current source is activated to charge an external capacitor. The UCC23711 features an internal leading edge blanking time after the gate driver output (OUT pin) switches to the on state to avoid false triggers from transient noise during the switching. When the driver turns off, the internal pulldown MOSFET discharges the voltage of the DESAT pin.

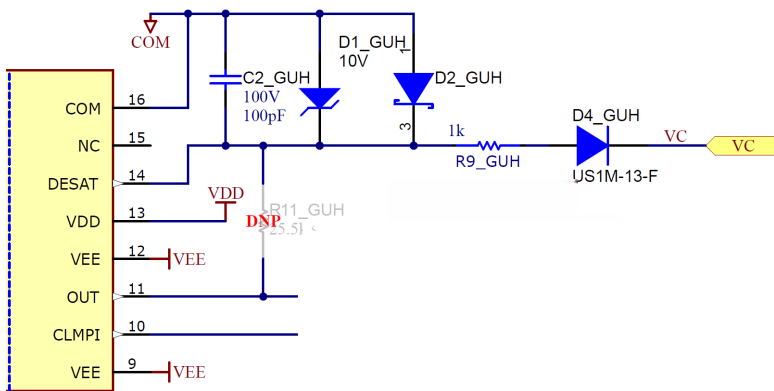


Figure 3-4. UCC23711 DESAT Circuit

The key passive components are the high voltage blocking diode D4, the current-limiting resistor R9 (1k Ω) and the blanking capacitor C2. The 1000V, 1A blocking diode D4 has an ultra-fast reverse recovery time of 75ns and minimal junction capacitance of 10pF to reduce transient charge currents during fast transients of the IGBT collector to emitter voltage, hence avoid false DESAT detection. The current-limiting resistor R9 also helps to adjust the DESAT detection threshold and acts as a low-pass filter together with the blanking capacitor C4 (100pF) and the D1 Zener diode parasitic capacitance (65pF) to improve noise immunity. The cut-off frequency is around 1MHz.

The 10V Zener diode D1 protects the DESAT from voltages greater than VDD and is optional, depending on the system conditions. The Schottky diode D2 is important and protects the DESAT pin from negative voltages versus the COM pin, which could occur due to high dv/dt switching, coupling through D4 junction capacitance.

The UCC23711 blanking capacitor charge current is typically 250μA. The charge current can be increased by adding a resistor R11 from the VOUT pin to the DESAT pin, when a higher charge current or a faster response time is desired. It is critical to place a fast Schottky diode D2 in series with the resistor R11 to block reverse current to the DESAT pin and avoid a negative voltage versus the COM pin. This is the case when a bipolar supply +15V/-8V is used. For more details, see [How can we increase the DESAT charging current?](#)

The effective blanking time and the response to an over-current depends on the IGBT's collector to emitter voltage at the time the over-current occurs, as shown in the following figure for two different timings depending on when the overcurrent occurred.

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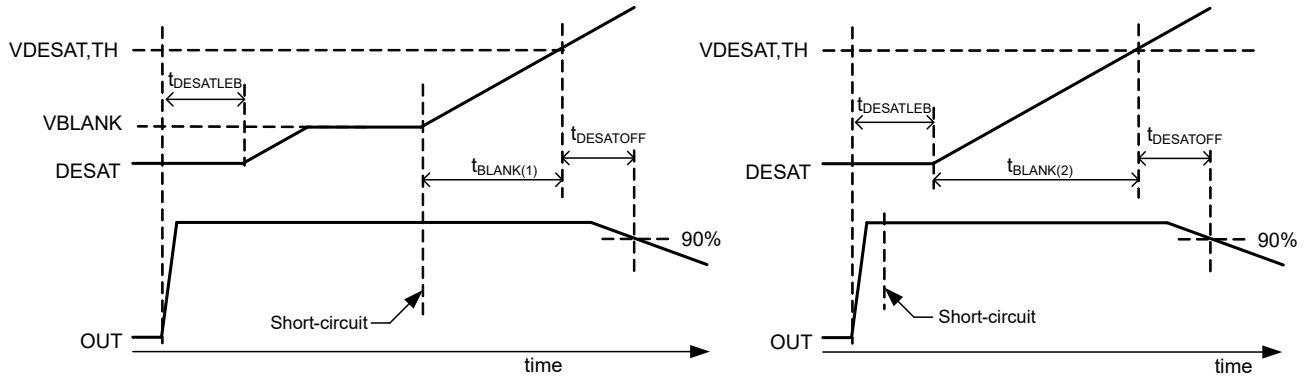


Figure 3-5. UCC23711 DESAT Protection Timing

The timing on the left shows an example, where the overcurrent occurs after the IGBT was turned on. After the IGBT turns on at normal operating and the UCC23711 leading edge blanking delay is expired, the blanking capacitor C2 is charged until it reaches the blanking voltage:

$$V_{BLANK} = V_F(D4) + R9 \times I_{CHG} + V_{CE(Sat)} = 2.15V, \quad (3)$$

where $V_{CE(Sat)}$ is the Q1 IGBT's typical saturation voltage of 1.6V.

Then the effective blanking time after an over-current occurs can be estimated per:

$$t_{BLANK(1)} = \frac{C_{BLANK} \times I_{CHG}}{V_{DESAT,TH} - V_{BLANK}} \quad (4)$$

where $V_{DESAT,TH}$ is the UCC23711 typical DESAT threshold of 6.5V, I_{CHG} the charging current 250μA typical and C_{BLANK} the blanking capacitor C2 in parallel to the parasitic capacitance of the 10V Zener diode D1 and V_{BLANK} as shown above.

The timing on the right shows an example where the IGBT is turned on creating a short-circuit and the collector to emitter voltage is larger than the UCC23711 DESAT threshold minus the voltage drop V_F across D4 and R9.

$$V_C \geq V_{DESAT,TH} - V_F(D4) - R9 \times I_{CHG}. \quad (5)$$

With a typical UCC23711 charging current I_{CHG} of 0.250mA, and $V_C \geq 5.45V$, the effective blanking time after the UCC23711 gate driver output is turned-on and the leading-edge blanking time expired can be estimated per:

$$t_{BLANK(2)} = \frac{C_{BLANK} \times I_{CHG}}{V_{DESAT,TH}} \quad (6)$$

The following table lists an estimate of the protection time until the gate drive output declines to 90% for both cases, based on effective blanking capacitance is $C2 = 100pF$ and $C(D1) = 60pF$.

Table 3-2. Estimated DESAT Protection Timing

Parameter	t_{DESATLEB} (TYP)	t_{BLANK} (TYP)	t_{DESATOFF} (TYP)	t_{TOTAL} (TYP)
Example 1	N/A	2.5us	0.2us	2.7us
Example 2	0.47us	4.1us	0.2us	4.8us

3.7 UCC23711 Fault (FLT) Feedback

The FLT pin is an open drain, active low. The FLT pin is pulled down to GND after a DESAT fault is detected. It is held low until the device is reset. To reset the device, the device must see a low to high PWM input transition after t_{FLTMUTE} mute time of 22us (TYP). Low to high PWM transitions before the mute time expires do not reset.

The FLT pull-up resistor R1 is 5.1kΩ. To improve noise immunity and avoid false FLT signals a 330pF capacitor C3 is added which provides a low-pass filter with a 100kHz cut-off frequency. The high to low transition with the active FLT pull-down is faster. The maximum input current of 20mA discharges the 330pF capacitor in less than 55ns.

4 System Test Results

4.1 Three-Phase IGBT Inverter under Test

The following figure shows the PCB of 3-phase IGBT inverter under test. An TMS320F28379 MCU Launchpad was used to provide the 3-phase complementary PWM to the control board interface. An external bipolar supply with six isolated bipolar 15V and -8V supplies was connected to the six reinforced isolated gate drivers UCC23711. The DC-link voltage was 550VDC, equivalent to a rectified 3-phase 400VAC input voltage.

The tests of the UCC23711 gate driver in this chapter were done with the phase U half-bridge of the IGBT six pack module with a nominal 550V DC bus voltage. The complementary PWM signals were generated by a TMS320F28379D Launchpad.

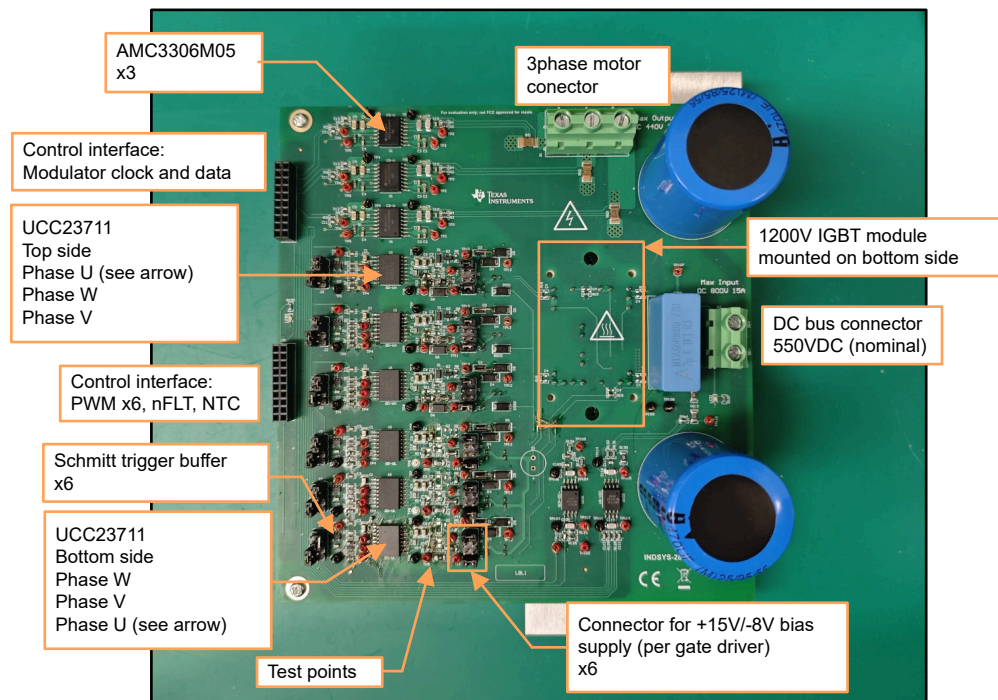


Figure 4-1. Three-Phase IGBT Inverter with UCC23711

4.2 UCC23711 Input Current Thresholds and Hysteresis

To validate the input threshold and hysteresis the slew rate of the octal buffer output was slowed down to around 150mV/ μ s by adding a 1 μ F capacitor to the Schmitt trigger inverter output as shown in Figure 4-2.

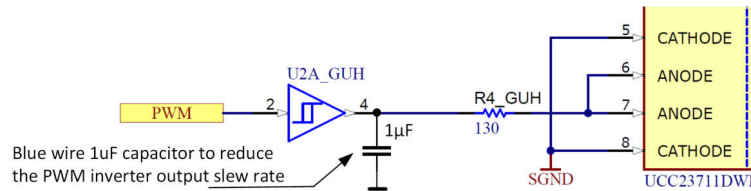


Figure 4-2. UCC23711 Input Current Threshold Test Circuit

Figure 4-3 shows the input turn on voltages and current. The current threshold is measured indirectly through the voltage drop with the current limit resistor R4. Figure 4-4 shows the input turn off. To increase the resolution to measure the turn off current, the current limit resistor R4 was replaced with 680 Ω only for this test.

The turn off threshold is around 0.4mA. The hysteresis between the turn on and turn off threshold is 0.4mA.

The steady state input current around 10.6mA, matching the calculated value from Table 3-1.

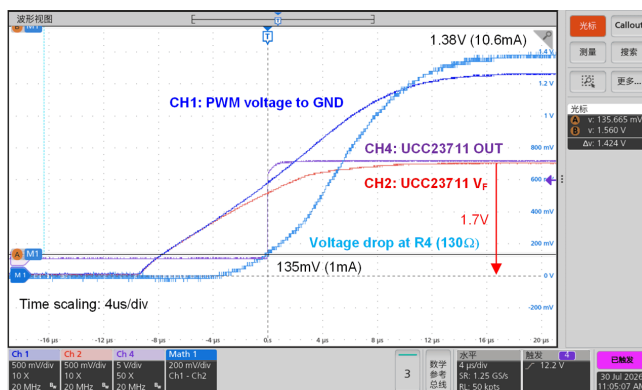


Figure 4-3. UCC23711 Input Turn Off

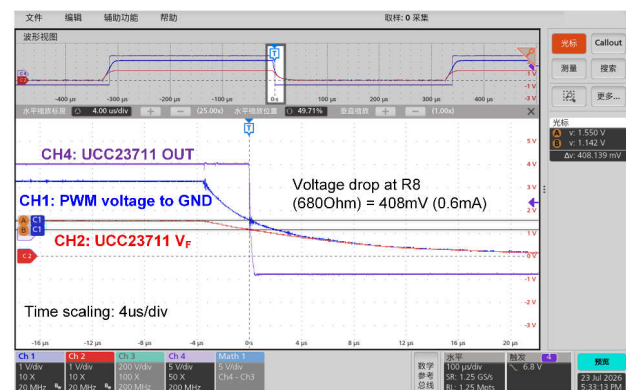


Figure 4-4. UCC23711 Input Turn Off

4.3 UCC23711 Propagation Delay

Figure 4-5 and Figure 4-6 show the propagation delay t_{PDH} and t_{PDH} between the UCC23711 input forward current I_F and the gate output voltage. The UCC23711 input current was measured indirectly through the voltage drop across the input resistor $R4 = 130\Omega$. The measured rising edge delay is t_{PDH} is around 68ns, the falling edge delay is around 64ns.

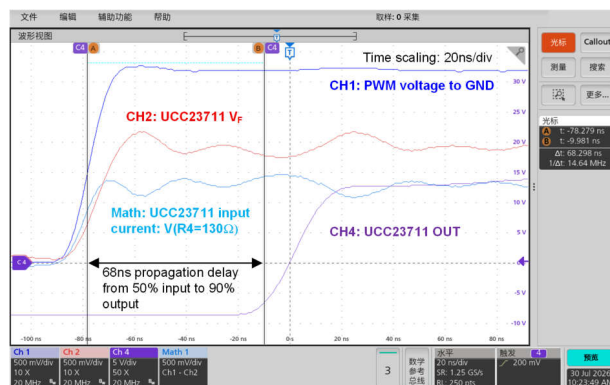


Figure 4-5. UCC23711 Rising Edge Delay

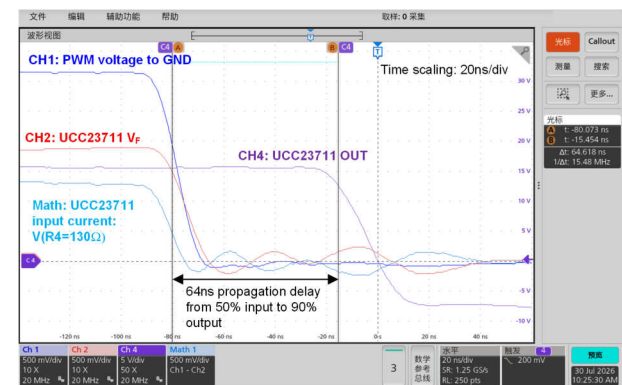


Figure 4-6. UCC23711 Falling Edge Delay

4.4 Phase U Turn-On and Turn-Off Slew Rates

The following figures show the phase U switch node rising and falling edges at positive 3.5A, figures 4-9 and 4-10 for egative -3.5A phase current. The PWM dead-time was set to 2.5us, the DC-link voltage to 550VDC.

The phase U switch node voltage slew rate is around 5.5V/us when the IGBT is hard switched on. When the IGBT is soft turned off (zero voltage switching) the slew rate depends on the phase current magnitude. At a magnitude of 3.5A, the slew rate was between 1.2V/ns to 1.3Vns. The effective switch node parasitic capacitance can be estimated from $C_{SW}=I_U/(dV_U/dt)$, which is around 2.6nF to 2.9nF.

The time to charge the IGBT gate V_{GE} from -8V to 15V with the gate current limit resistor $R12+R13=10.2\Omega$ is around 520ns, the discharge time from 15V to -8V is around 360ns with the gate current limit resistor $R12=5.1\Omega$.

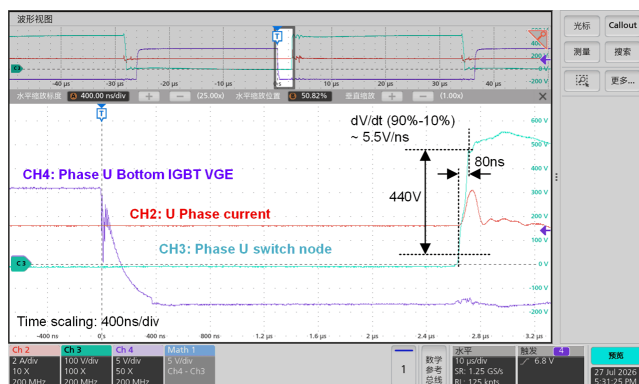


Figure 4-7. Phase U Rising Edge at 3.5A

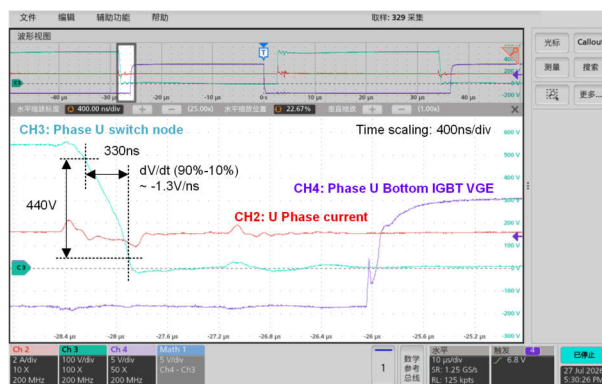


Figure 4-8. Phase U Falling Edge at 3.5A

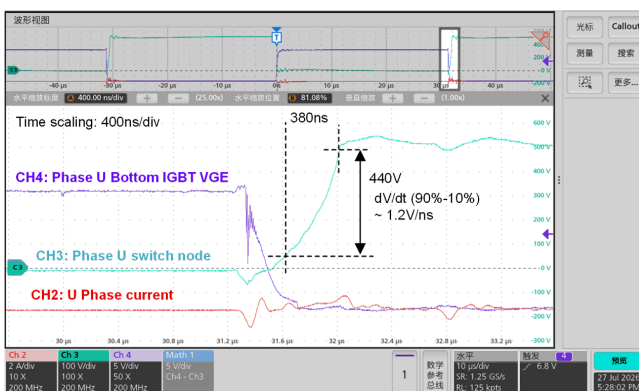


Figure 4-9. Phase U Rising Edge at -3.5A

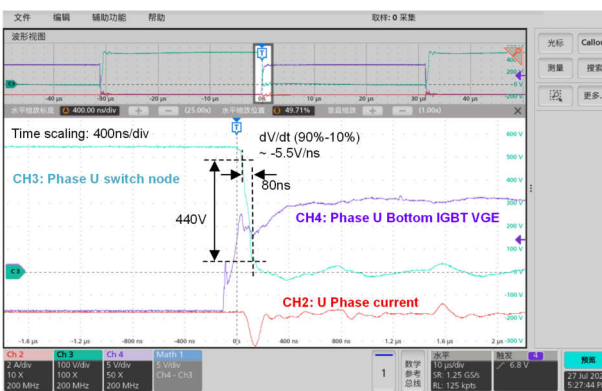


Figure 4-10. Phase U Falling Edge at -3.5A

4.5 UCC23711 Miller Clamp and Unipolar 15V Supply

The Miller clamp activation always turns on when the IGBT gate voltage V_{GE} falls below the Miller clamp threshold voltage $V_{CLMP_{TH}}$ of 2.1V (TYP) referenced to the VEE pin. The Miller clamp turn on response time is typically 38ns and has a pull-down resistance of 0.8Ω typically.

Figure 4-11 shows the effect of the Miller clamp when the gate driver turns off using a bipolar supply with $V_{EE} = -8V$. As soon as the V_{GE} is less than $V_{EE} + V_{CLMP_{TH}}$, the Miller clamp gets activated. Considering the delay of 38ns, the drop is visible at around $V_{GE} = -6V$.

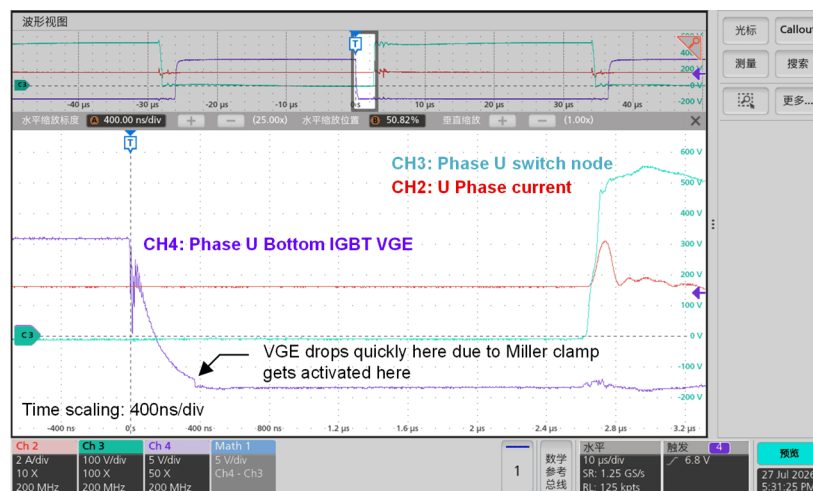


Figure 4-11. Effect of Miller Clamp at Bottom-side IGBT V_{GE} with Bipolar Supply During Turn-Off

To validate the Miller clamp, the 3-phase inverter was operated with a unipolar supply at a nominal DC link voltage of 550V. To obtain the highest slew rate of the phase voltage the output current zero. Figure 4-12 shows the bottom side IGBT gate to emitter voltage V_{GE} in off state, when the top side IGBT is hard turned on at a slew rate of around 10V/ns.

While the Miller clamp is active, the bottom side V_{GE} only increased to around 2.4V for less than 25ns due to the high slew rate of the V_{CE} and remained well below the IGBT's gate threshold voltage of 5.8V.

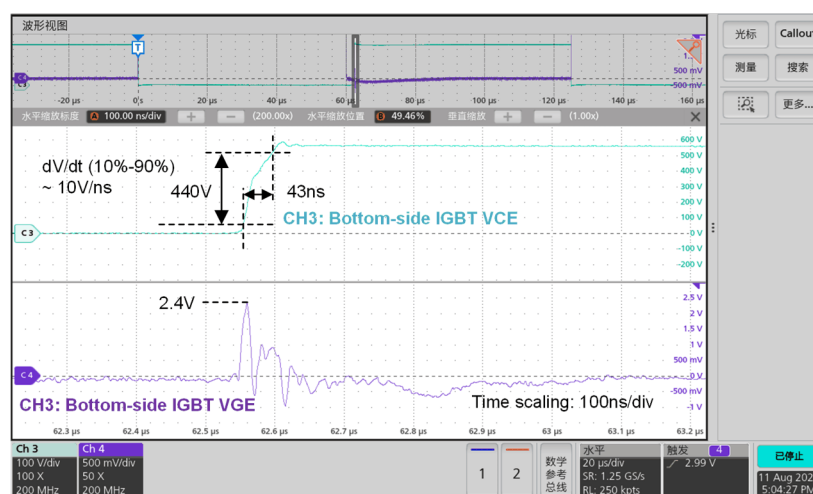


Figure 4-12. Bottom-Side IGBT V_{GE} with Unipolar 15V Supply

4.6 UCC23711 DESAT Response and Soft Shut Down

For the DESAT test, the low-side IGBT was turned on at the full DC-bus voltage of 550V, hence immediately after turning on creating a short-circuit. Since $V_{CE} \gg V_{DESAT,TH}$ the blanking time is defined by:

$$t_{BLANK(2)} = \frac{C_{BLANK} \times I_{CHG}}{V_{DESAT,TH}} \quad (7)$$

The following figure shows the measured blanking time is around 4.1us with a total protection time until the gate drive output declines to 90% of 4.8us.

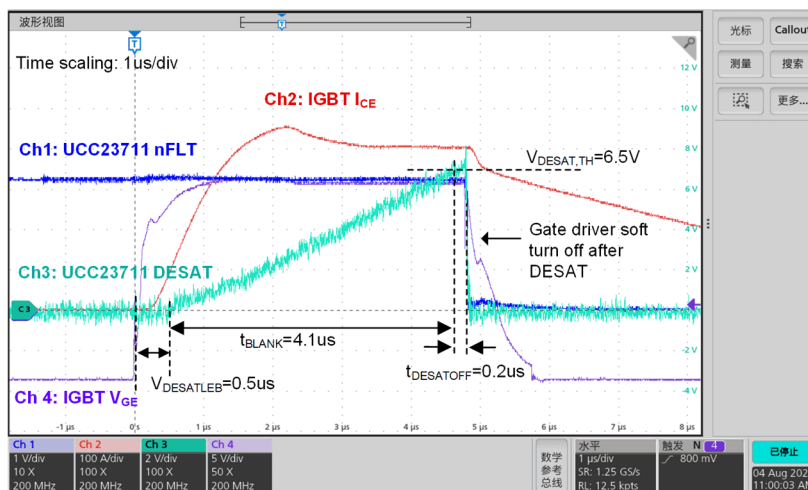


Figure 4-13. DESAT Timing with C4=100pF and D1 in Parallel, R11 DNP

The effective blanking capacitance can be calculated to 160pF, with the blanking capacitor C4=100pF and the remaining parasitic capacitance of 60pF dominated by the Zener diode D1. After DESAT has triggered, the gate driver is soft turned off with a sink current of 0.25A. Figure 4-14 zooms into the soft shutdown.

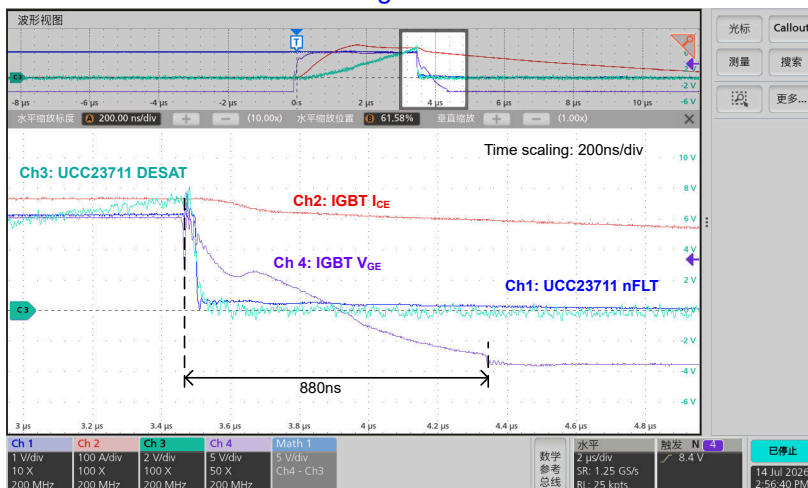


Figure 4-14. Soft Turn Off after DESAT with C4=100pF and D1 in Parallel, R11 DNP

The sink current of the UCC23711 during a soft turn off is 0.25A. The IGBT's gate charge of 0.3μC is discharged from 15V to -8V in around 880ns. This is around 2.5 times slower than in normal mode (360ns), as seen in the previous figure. The drop of V_{GE} from around -6V to -8V after 880ns is due to the Miller clamp gets activated.

4.7 Increasing the DESAT Charge Current

Figure 4-15 shows the DESAT timing with the blanking resistor R11 = 25.5k Ω populated to drive a higher DESAT charging current. The blanking capacitor C4 was replaced with 220pF to further increase transient noise immunity. The effective blanking time is now 2.9 μ s. With an effective blanking capacitance of 220pF (C4) + 60pF (D1) the effective blanking current $I_{CHG} + I_{R11}$ is around 0.6mA.

Adding R11 hence allows to reduce the DESAT protection time with UCC23711 when driving SiC-FETs. Refer to [How can we increase the DESAT charging current?](#)

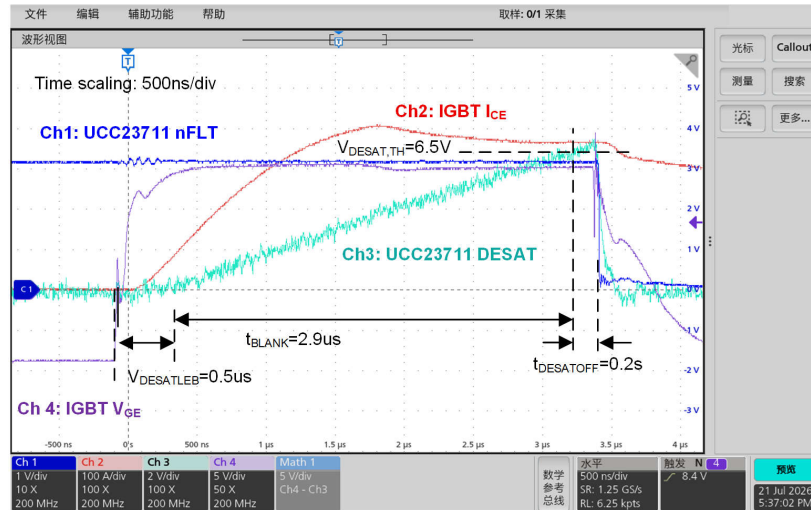


Figure 4-15. DESAT Timing with C4=220pF and D1 in Parallel, R11=25.5k

4.8 UCC23711 VDD UVLO Thresholds and Gate Drive Output

Figure 4-16 and Figure 4-17 show the UCC23711 gate drive output during the ramp up and ramp down of the bipolar supply voltage VDD-COM=15V and VEE-COM=-8V.

The UCC23711 VDD UVLO threshold is measured vs. the IGBT emitter, which is references to the UCC23711 COM pin.

The VDD falling edge threshold is 11V, the VDD rising edge threshold is 12V and matches the specified typical specification in the UCC23711 datasheet.

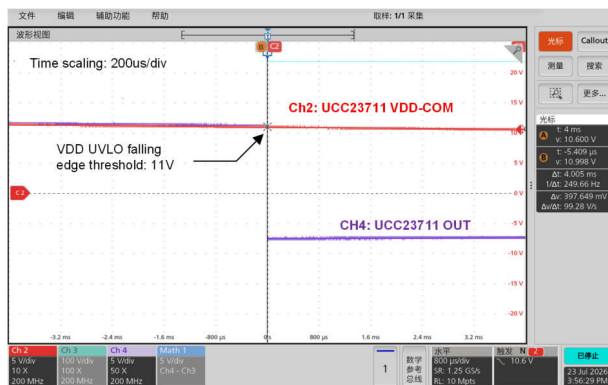


Figure 4-16. VDD UVLO Falling Edge Threshold

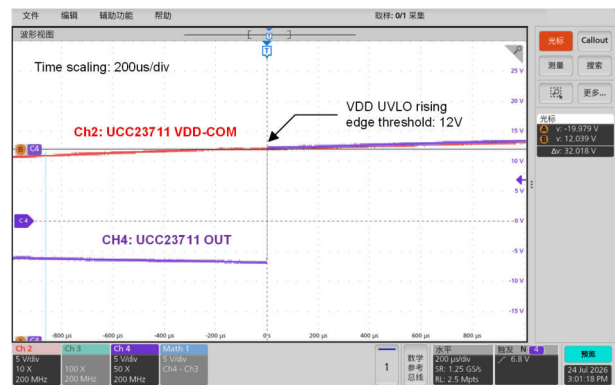


Figure 4-17. VDD UVLO Rising Edge Threshold

4.9 UCC23711 Gate Drive Power Consumption

Table 4-1 shows the measured supply current of the UCC23711 for a unipolar supply $V_{DD}=15V$, Table 4-2 for a bipolar supply $V_{DD}=15V$ and $V_{EE}=-8V$. A multimeter was connected to the gate driver power supply circuit V_{DD} and V_{EE} to measure the current consumption at PWM frequencies of 0Hz, 8kHz and 16kHz driving the IGBT module Q1 with a gate charge of $0.2\mu C$ at a 15V unipolar supply and $0.3\mu C$ with a bipolar +15 and -8V supply. The optional pull-down resistor R15 at the IGBT's gate to emitter was not populated. The measured supply currents are within 5% of the calculated numbers.

Table 4-1. UCC23711 Current Consumption with Unipolar Supply

PWM	0Hz	8kHz	16kHz
I_{VDD} at $V_{DD}-COM=15V^*$	2mA (2mA)	3.56mA (3.75mA)	5.02mA (3.53mA)

Table 4-2. UCC23711 Current Consumption with Bipolar Supply

PWM	0Hz	8kHz	16kHz
I_{VDD} at $V_{DD}-COM=15V^*$	2mA (2mA)	4.39mA (4.55mA)	6.65mA (6.95mA)
I_{VEE} at $V_{EE}-COM=-8V^*$	-1.57mA (-1.5mA)	-3.83mA (-4.05mA)	-6.1mA (-6.45mA)

* The numbers in parenthesis are the calculated numbers.

5 Summary

This document provides circuit design guidelines for enhancing 3-phase IGBT inverter robustness using UCC23711 and UCC23710 isolated gate drivers featuring configurable DESAT (6.5V/9V). It details the optimization of input resistor configurations, peak output currents, DESAT protection, active Miller clamping, and supply decoupling for both unipolar and bipolar setups. All design parameters are validated via empirical testing on a 3-phase IGBT inverter prototype at a 550V DC bus. Leveraging SiO₂ isolation and opto-compatible inputs, the UCC23711 and UCC23710 gate drivers enable seamless integration into legacy optocoupler applications, while offering lower propagation delay and higher CMTI.

6 References

1. Texas Instruments, [UCC23711](#), product page.
2. Texas Instruments, [UCC23710](#), product page.
3. Texas Instruments, [UCC23711DWREVM](#), tool page.
4. Texas Instruments, [Choosing Appropriate Protection Approach for IGBT and SiC Power Modules](#), application note.
5. Texas Instruments, [How can we increase the DESAT charging current?](#), E2E forum.
6. Texas Instruments, [UCC217xx XL Calculator Tool](#), calculation tool.

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Last updated 10/2025