

Design Considerations of LLC in Automotive 800V Battery by UCC256612



Martin Huang, Mingrui Zhu, Jaden Ning, Daniel Gao

Abstract

800V bus systems have become popular for high-power systems. We are looking for an analog LLC controller to support those applications such as the standby (and fan) power in data centers or μ DCDC in electric vehicles, but most LLC controllers only support 650V voltage rating on HV and HS. In this application note, we used an analog LLC controller to transfer the input voltage from 450V to approximately 800V into 48V with 300W output power. We stacked an HV start-up pin with external depletion mode N-channel MOSFET to extend the voltage rating on HV pin to power up the controller. We used a capacitor divider to lower the SW voltage to half for adaptive dead time detection. The high-side FET is driven by the HO signal through an isolated gate driver. We replaced the optocoupler with an opto-emulator to mitigate premature failure and signal degradation caused by current transfer ratio (CTR) degradation over time, thereby extending the overall system lifetime.

Table of Contents

1 Introduction	2
2 Detailed Description	3
2.1 How to Implement an HV Start-Up Circuit	3
2.2 How to Implement Switching Node Detection and Driving Circuit	6
2.3 How to Implement Opto-Emulator for Feedback Circuit	9
2.4 Evaluation Result	10
3 Summary	12
4 References	12

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

For UCC256612, the recommended voltage rating on HV and HS pins is 640V. To implement UCC256612 into an 800V LLC design, there are two key challenges:

1. For better power saving, terminate the start-up current in normal operation state. How does a user implement HV start-up circuit supporting higher input voltage while maintaining low power consumption on the start-up circuitry?
2. Use the HS pin for adaptive dead time control to optimize the performance. How does a user implement switching node detection and driving circuit to support switching voltage higher than the HS pin voltage rating?

For better lifetime, use an opto-emulator to eliminate the decay of the opto-coupler. How does a user implement opto-emulator for the feedback circuit?

Finally, this document combines information together and shows the test results of the reference design.

2 Detailed Description

Figure 2-1 shows the block diagram of the LLC system and the key features which are highlighted in previous sections. The following sections discuss the details.

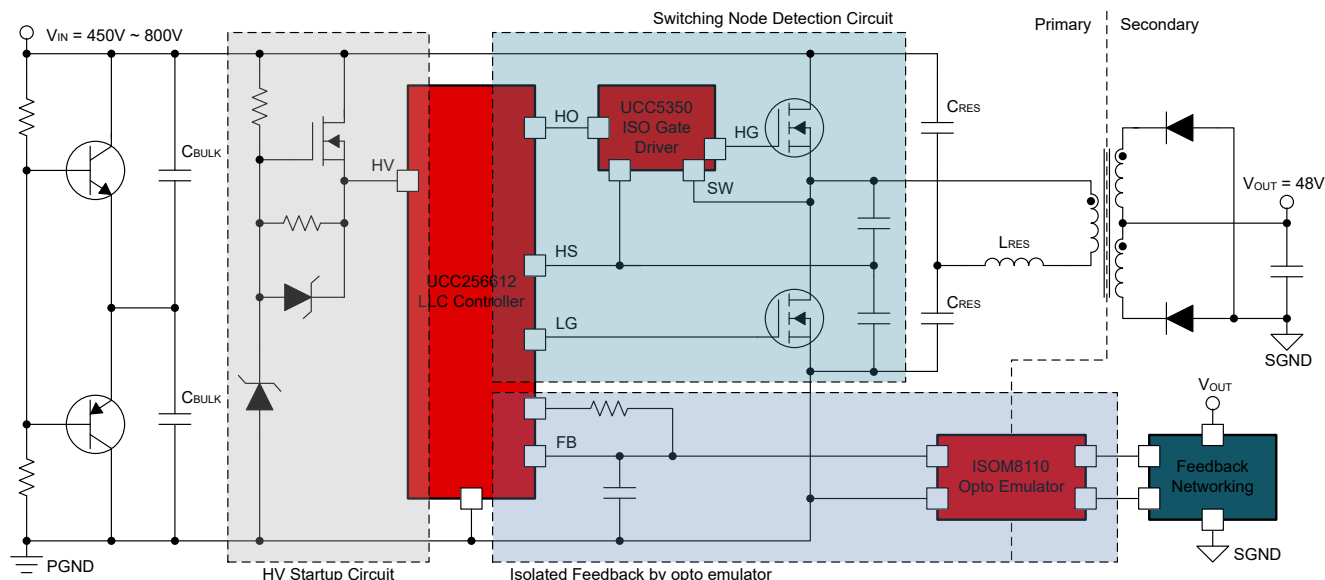


Figure 2-1. Block Diagram of the LLC System

2.1 How to Implement an HV Start-Up Circuit

In the UCC256612 controller, the embedded HV pin supports start-up without X-cap discharge function. The HV pin connects to the DC bus directly (or through two resistors). The internal high voltage current source charges the VCCP pin during system start-up and turns the pin off when the VCCP equals VCCstartSelf (approximately 14V).

To support 800V start-up, the internal 640V rating of the UCC256612 is insufficient. Therefore, an additional high-voltage MOSFET stacked with the HV pin is required to implement high-voltage start-up. By employing a depletion-mode N-channel MOSFET, the system achieves a normally-on configuration, eliminating the need for external start-up bias resistors. We can choose BSS126 (600V depletion MOSFET with SOT-23 package) or BSS135 (same parameters as BSS126 with SOT-223 package) to extend the start-up voltage rating.

As shown in Figure 2-2, during the power-on stage, when VCCP is lower than VCCstartSelf, the internal current source of HV pin pulls the source of BSS126 lower than its gate to turn BSS126 on. The internal high-voltage (HV) current source regulates the charging current of the VCCP capacitor at a maximum of 10mA. When the VCCP triggers the VCCstartSelf, the internal HV current source turns off and leaves the HV pin floating, and the source of BSS126 is higher than its gate to turn BSS126 off until the VCCP is discharged to VCCstopSwitching (9.5V) to turn the HV pin on again.

To protect the system, we need to make sure the Vgs voltage of BSS126 is properly clamped. We have one resistor and a 12V Zener diode in parallel between Vgs of BSS126 to limit the voltage stress between 1V and -12V, which is lower than the maximum Vgs rating of BSS126 which is $\pm 20V$.

The next objective is to make sure the voltage stress on the V_{DS} of BSS126 and HV pin are sufficient. We use a pull-high resistor on the gate of BSS126 and clamp the voltage using a Zener diode. We used three 1206 resistors to support 600V voltage rating and four 130V Zener diodes which clamp the gate voltage to be approximately 520V. We choose approximately total 10M Ω pull-high resistors to lower the power consumption of the resistors.

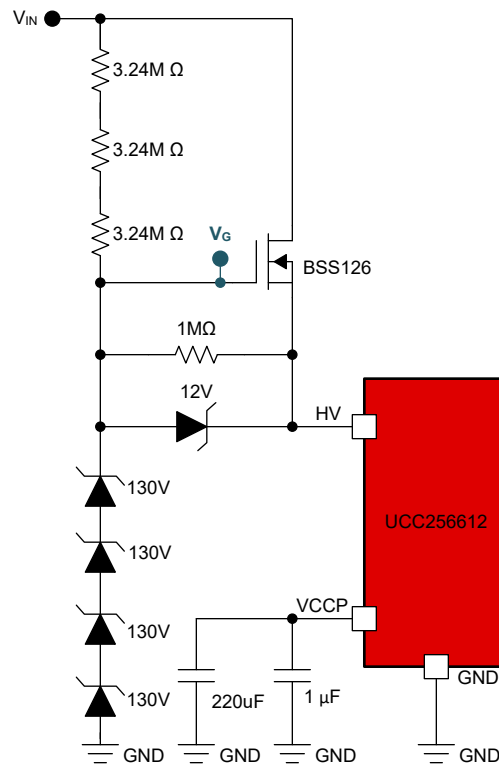


Figure 2-2. Extend Start-Up Capability to 800V, V_G is the Measurement Point for the Start-Up Circuit

Before powering on the system for the first time, lower the input voltage to below the brown-in voltage to check the operation of the start-up circuit without the possibility of damage to the whole system. Figure 2-3 shows the start-up circuit working at $V_{IN} = 50V$. Here, check the VCCP and the V_G :

1. The timing of dip of V_G matches to the charging period in VCCP
2. The voltage of V_G is about half of the V_{IN}

We can incrementally increase the V_{IN} to confirm the start-up circuit.

In practical design, the V_G and HV pins exhibit very high impedance, making them highly susceptible to interference. Therefore, it is critical to maintain a quiet PCB layout around these pins by keeping high di/dt or dv/dt circuits away from the vicinity, thereby minimizing noise coupling.

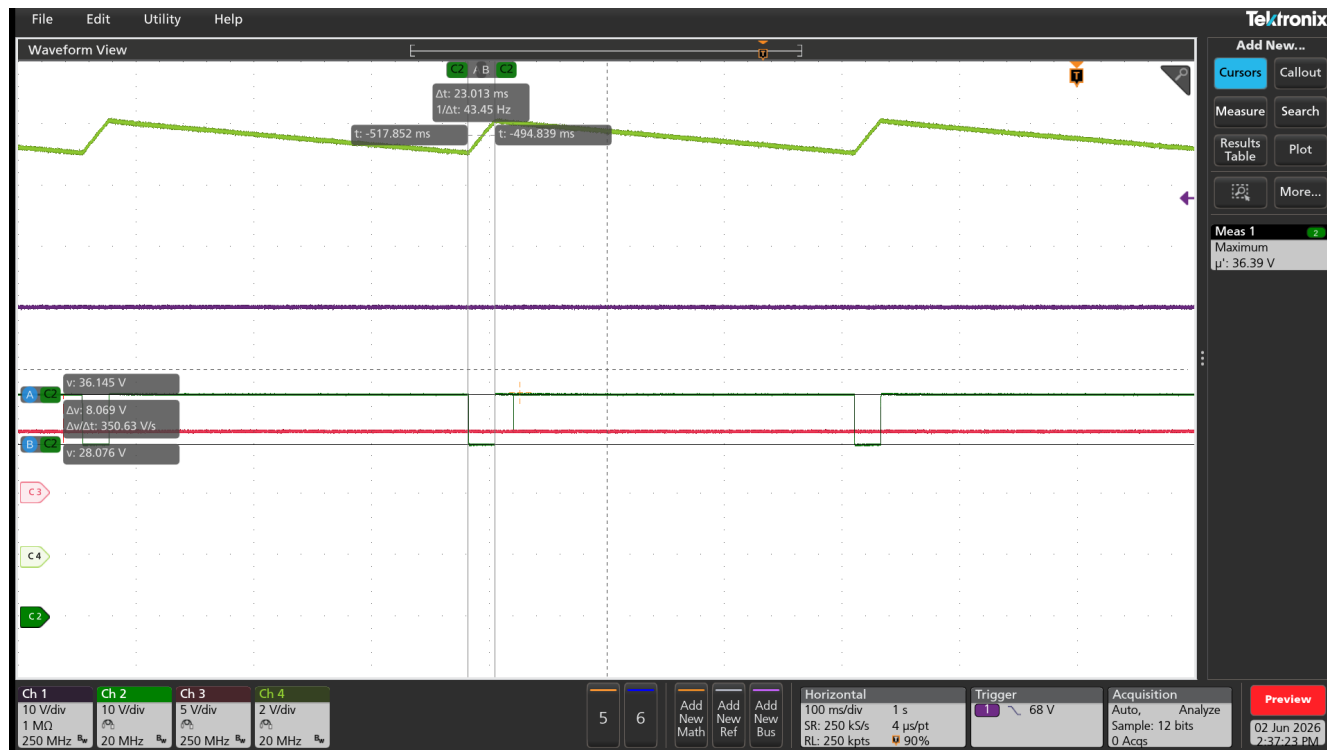


Figure 2-3. Start-Up Waveform at $V_{IN} = 50V$ CH1: V_{IN} , CH2: V_G , CH3: V_{5P} , CH4: V_{CCP}

Figure 2-4 shows the system start-up at 800V. It shows the V_G is clamped at 527V for about 100ms and then reduces to 427V which is around half of V_{IN} , which matches our design target.

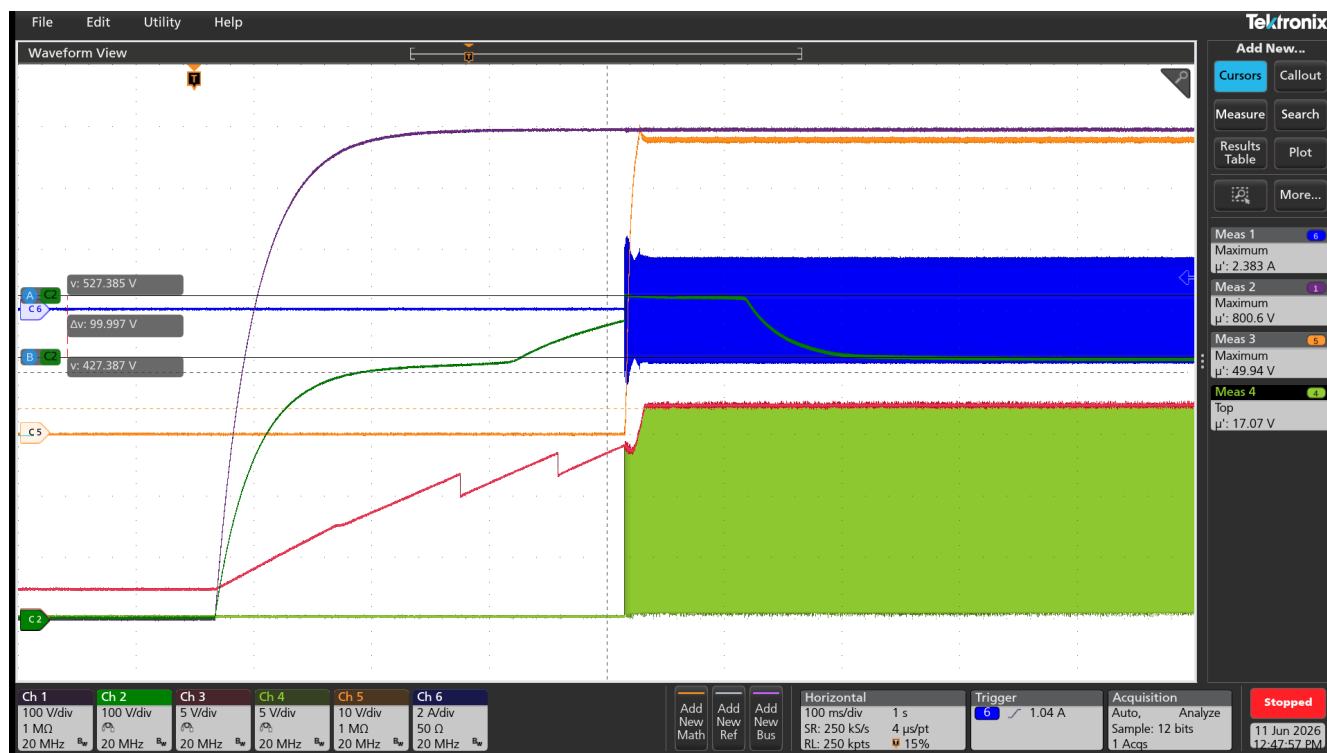


Figure 2-4. Start-Up Waveform at $V_{IN} = 800V$, and $V_{OUT} = 48V - 6.5A$ CH1: V_{IN} , CH2: V_G , CH3: V_{CCP} , CH4: LO , CH5: V_{OUT} , CH6: I_{RES}

2.2 How to Implement Switching Node Detection and Driving Circuit

The internal HS of UCC256612 can only support 640V; this leads to two issues:

1. UCC256612 uses the input of HS pin for adaptive dead time control to optimize the system performance.
2. The internal bootstrap circuit can't drive the high side FET.

Figure 2-5 shows the proposed schematic for those issues. To lower the voltage on HS pin with good response time, use two capacitors as a voltage divider to cut SW voltage into half and send the slew rate of SW into HS pin for adaptive dead time control and prevent HS from being out of the voltage stress. Limit the capacitance values (such as 68pF) to lower the parasitic capacitance, which can degrade the slew rate of the SW node. Use another two ultra-fast diodes in parallel with the capacitors to make sure the HS pin closes to GND when the low side FET turns on. .

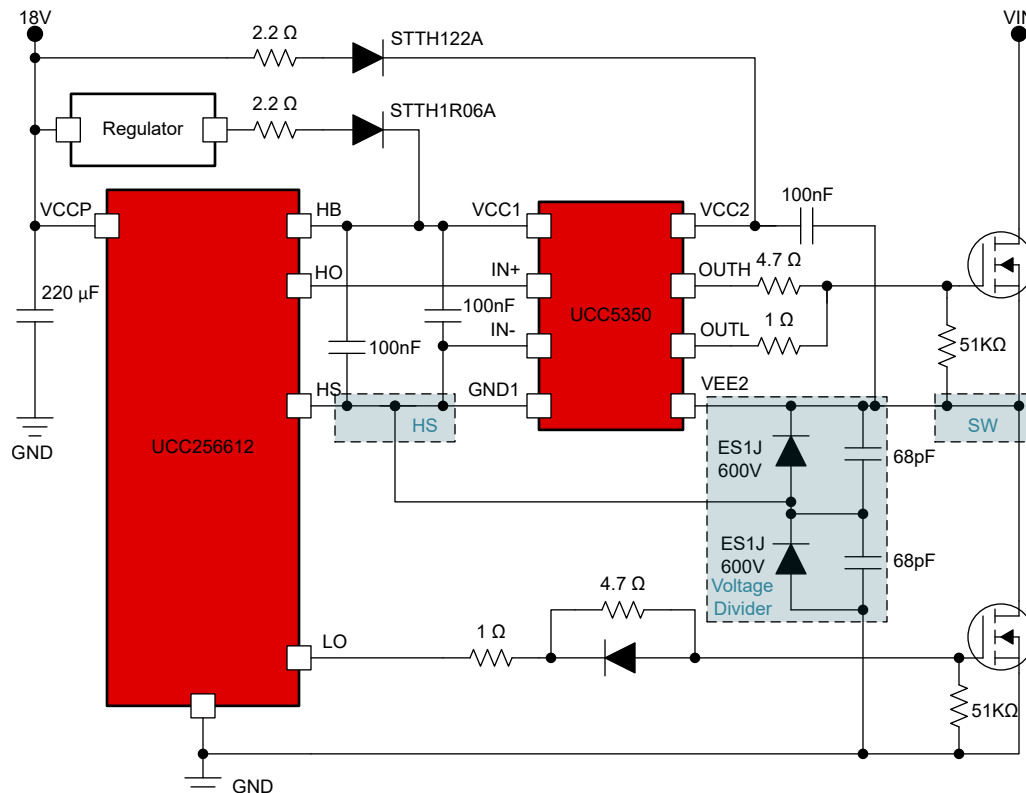


Figure 2-5. SW Node Detection and Driving Circuit

To drive the high side device, use an external isolated gate driver. UCC5350 provides 3KV_{RMS} isolated voltage, 10A peak current drive strength, and 100V/ns CMTI capability which fulfills this application. In the input stage, use the HO signal as IN+ input, and HB for VCC1, and another bootstrap circuit with 1.2KV diode from VCCP to SW node to support VCC2. In UCC256612, the LO turn on voltage, V_{LOH} is:

$$V_{LOH} = V_{VCCP} - V_{DRV\ ON} \quad (1)$$

The V_{VCCP} is the voltage on VCCP pin and V_{DRV_ON} is the V_{DS} voltage on the driver when it turns on, and the maximum voltage is 0.3V. This is very close to the VCCP. This means the user can drive external SiC FETs if we set the VCCP voltage to be about 18V, and 12 to approximately 15V for traditional MOSFETs. For PMP4113 reference design, drive external SiC FET, and set the VCCP to be 18V, but the VCC1 and IN+ of UCC5350 must be lower than 15V in. In this case, a regulator was used which is designed by 2N7002 MOSFET and 15V Zener diode with 200K Ω bias resistor to limit the voltage stress to be $15V - V_{TH}$ with low consumption but keep 18V bootstrap in VCC2 to drive SiC FET directly.

For systems that cannot verify V_{VCCP} above 12V (such as wide output voltage range application), an additional external VDD UVLO protection circuit is recommended to verify reliable SiC FET gate drive operation.

Is there any possibility of making the high and low side FETs shoot through because of more propagation delay on the isolated gate driver? Because of the adaptive dead time control method in UCC256612, the slew rate detector detects the dead time between HO turn off and LO turn on. This dead time is copied and then applied to low-side MOSFET turn off and high-side MOSFET turn on. [Figure 2-6](#) shows the timing diagram of the dead time detection. To simplify the problem, we set the total propagation delay time of high side turn off (including HO from high to low, and OUTL) is t_D . Assume the total propagation delay time of high side turn on is as the same value. Time between SW falling time, t_{SWF} to LO turn on with approximately 40ns detection delay time as t_{DET} . At this moment, the dead time from high side turn off to low side turn on, t_{DEAD} is:

$$t_{DEAD} = t_D + t_{SWF} + t_{DET} \quad (2)$$

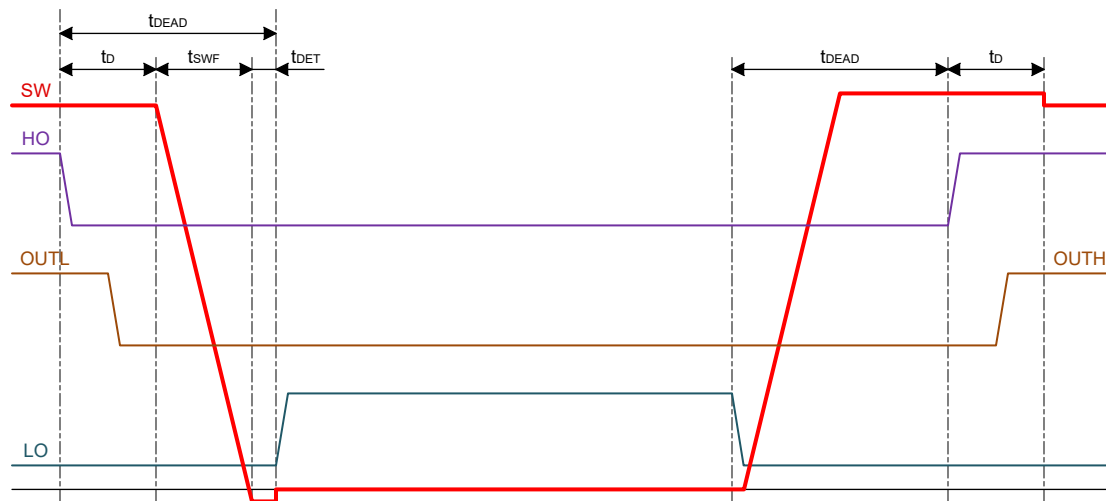


Figure 2-6. Timing Diagram of Dead Time Detection Circuit

Calculate the real dead time from low side turn off to high side turn on to be $t_{DEAD} + t_D$. For the SW pin from high to low, the dead time is detected, and it is not possible to shoot through. For the SW pin from low to high, more time was extended to make sure the system is not overlapping. To reduce the dead time of SW pin from low to high, we may put another isolated gate driver to balance the turn off time on low side FET.

[Figure 2-7](#) shows the waveform of LO turns on. $t_{SWF} + t_{DET}$ is 216ns, and [Figure 2-8](#) shows the waveform of LO turns off and the $t_{SWR} = 161ns$, which is shorter than the t_{DEAD} .

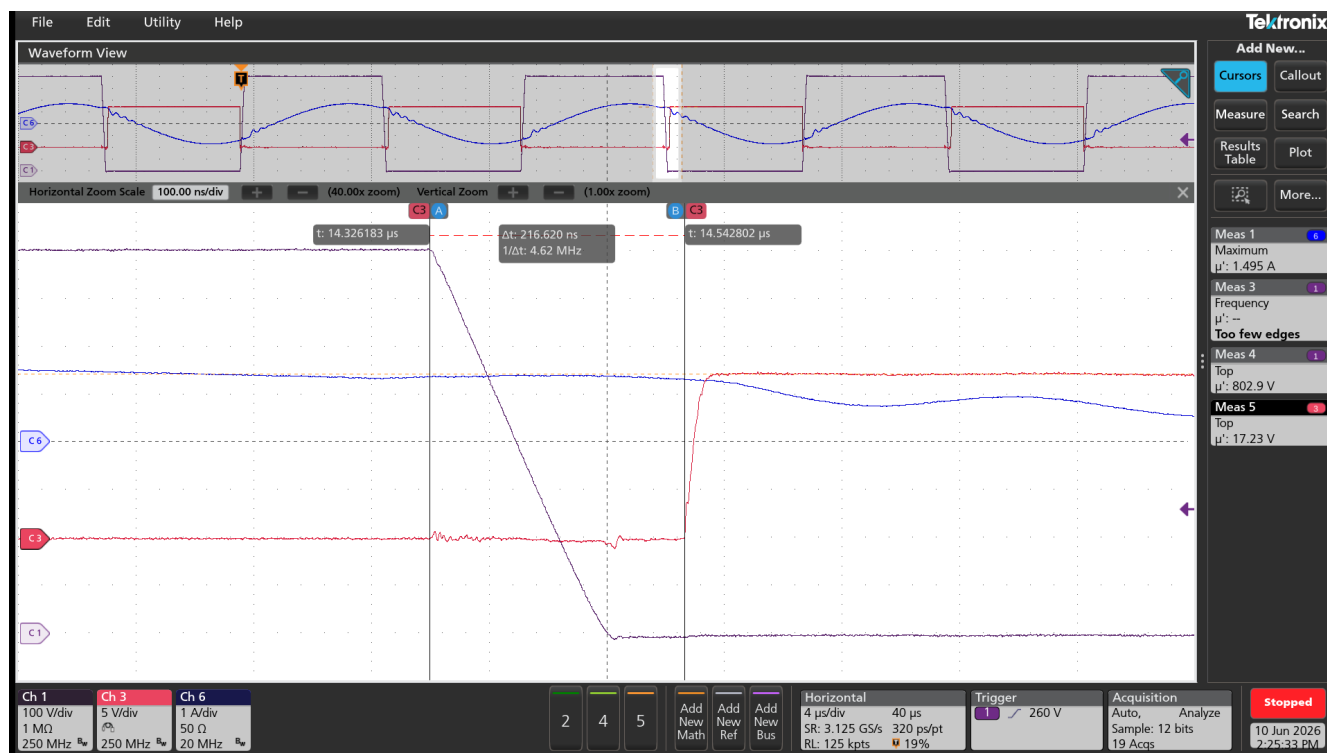


Figure 2-7. LO Turns On Waveform CH1: SW, CH3: LO, CH6: I_{RES}

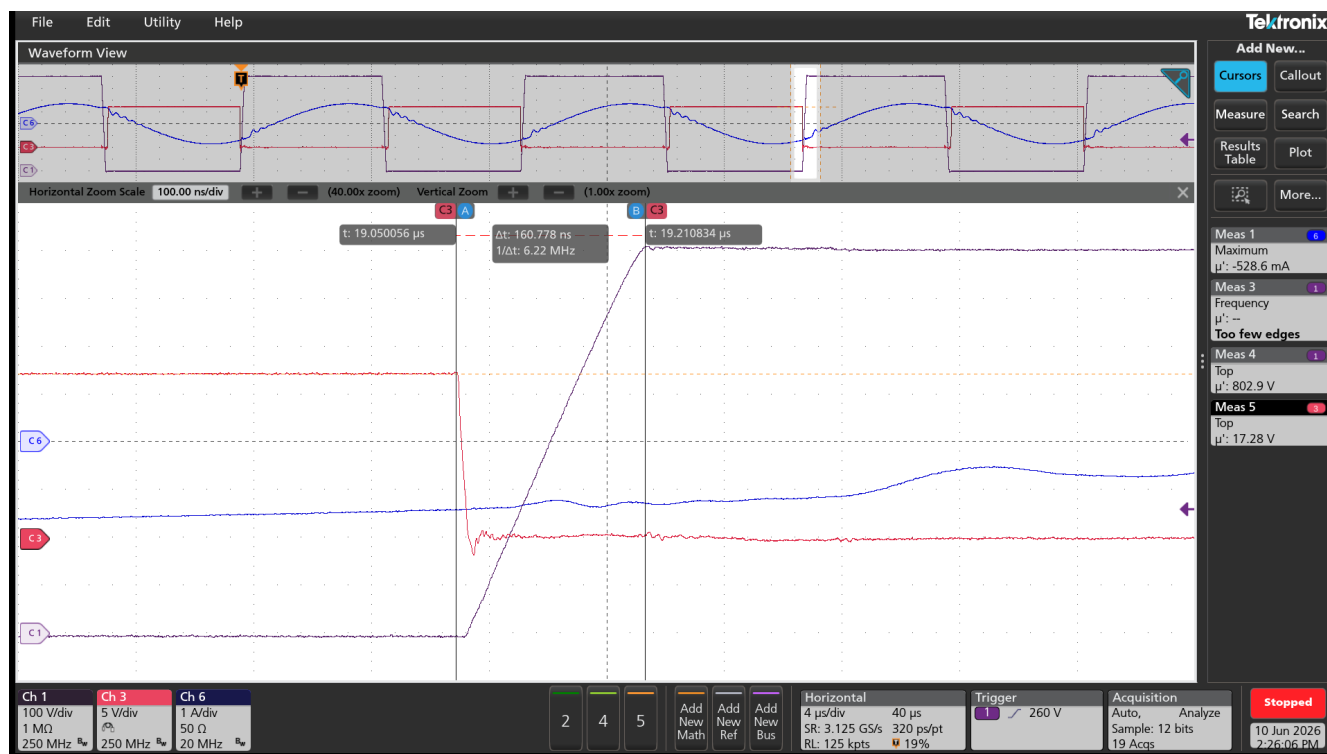


Figure 2-8. LO Turns Off Waveform CH1: SW, CH3: LO, CH6: I_{RES}

2.3 How to Implement Opto-Emulator for Feedback Circuit

The ISOM8110 opto-emulator uses an emulated LED as the input stage, with TI's proprietary silicon dioxide-based (SiO₂) isolation barrier technology to make ISOM8110 resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age. Figure 2-9 shows the typical feedback circuit by using the ISOM8110 device.

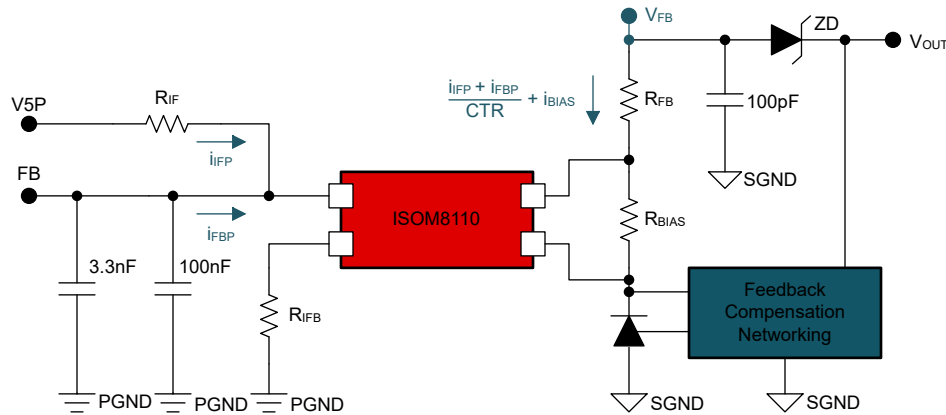


Figure 2-9. Feedback Circuit by ISOM8110 Opto-Emulator

The key difference between opto-emulator and optocoupler is the minimum I_F requirement. The minimum i_F requirement is 0.5mA for ISOM8110 and 0.7mA for ISO8110-Q1. We need to set:

$$i_F = \frac{i_{IFP} + i_{FBP}}{CTR} \geq 0.7\text{mA} \quad (3)$$

In UCC256612, the V5P is 5V, FB voltage is about 3.5V and the i_{FBP} is 60μA to approximately 160μA. The CTR of ISOM8110-Q1 is 80% to approximately 180% with $I_F = 2\text{mA}$. First, we need to calculate the R_{IF} value as:

$$R_{IF} \leq \frac{V_{5P} - FB}{0.7\text{mA} \times CTR_{MAX} - i_{FBP_MIN}} \quad (4)$$

By putting the values with worst-case conditions into the formula, we get $R_{IF} \leq 1.25\text{K}\Omega$. We choose 1.24KΩ for this design and put another 100nF capacitor to make the system more stable..

In the secondary side, select ATL432LI-Q1 which is a low regulation current (max: 80μA). Due to the maximum voltage rating of ATL432LI-Q1 is 36V, an 18V Zener diode was chosen to lower the voltage stress, and V_{FB} is 48V – 18V = 30V. The V_F of ISOM8110-Q1 is 1.2V, $R_{BIAS} = 10\text{K}\Omega$ to provide 120μA regulation current to ATL432LI-Q1. In this case, the maximum feedback current in secondary side is:

$$i_{FBS_MAX} = \frac{i_{IFP} + i_{FBP_MAX}}{CTR_{MIN}} + i_{BIAS} = 1.832\text{mA} \quad (5)$$

With $R_{FB} = 5.11\text{K}\Omega$, the voltage drop on R_{FB} is 9.362V which is good enough for normal operation. The loss on R_{FB} is approximately 17.15mW and Zener diode is about 33mW. In this design, it is possible to remove R_{BIAS} because the i_{FBS_MIN} is higher than the regulation current of ATL432LI-Q1.

2.4 Evaluation Result

We built the reference design PMP41133, which supports $V_{IN} = 450V$ to approximately $800V$, and $V_{OUT} = 48V$ and $6.5A$ design. Secondary winding is designed by center tape with two rectifiers by $150V$ Schottky diodes. [Figure 2-4](#) shows the start-up waveform at $V_{IN} = 800V$ and $V_{OUT} = 48V / 6.5A$. [Figure 2-10](#) shows the switching waveform at $V_{IN} = 450V$ and $V_{OUT} = 48V$ and $6.5A$.

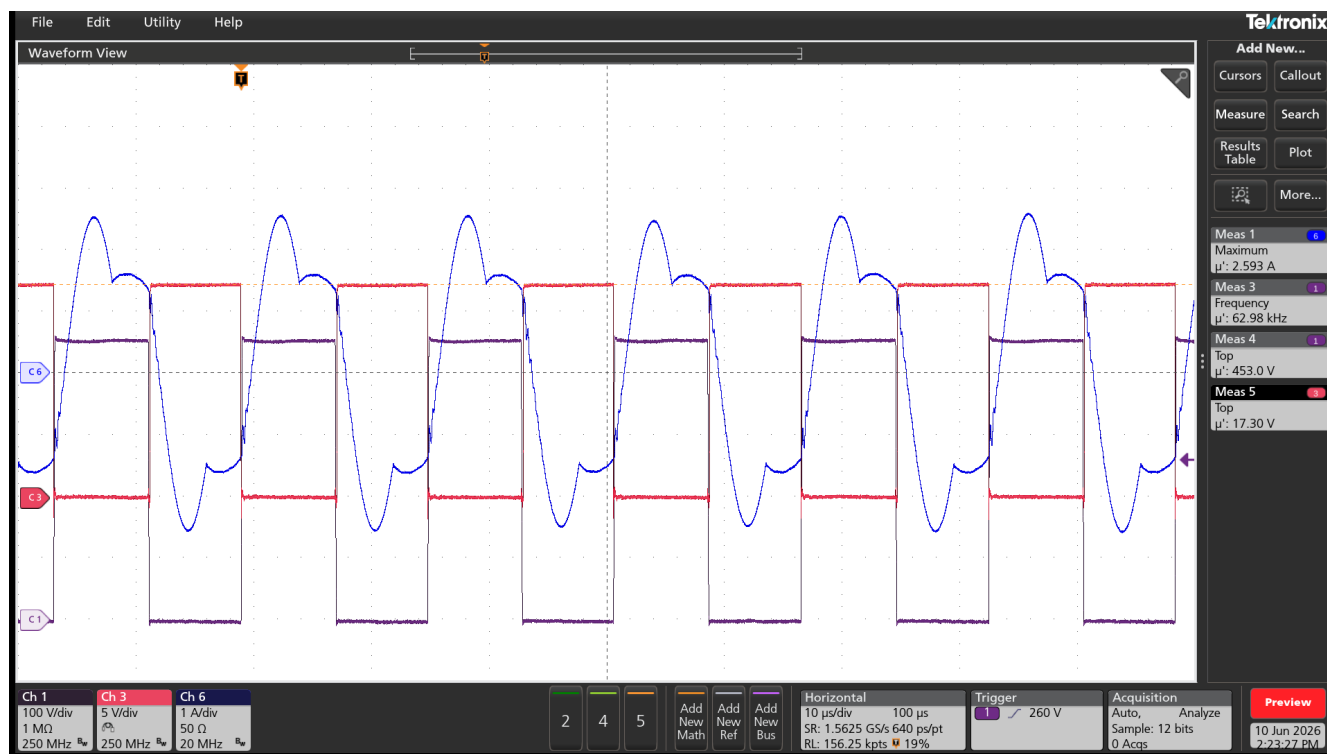


Figure 2-10. Switching Waveform at $V_{IN} = 450V$ and $V_{OUT} = 48V / 6.5A$. Ch1: SW, CH3: LO, CH6: I_{RES}

[Figure 2-11](#) shows the switching waveform at $V_{IN} = 800V$ and $V_{OUT} = 48V / 6.5A$.

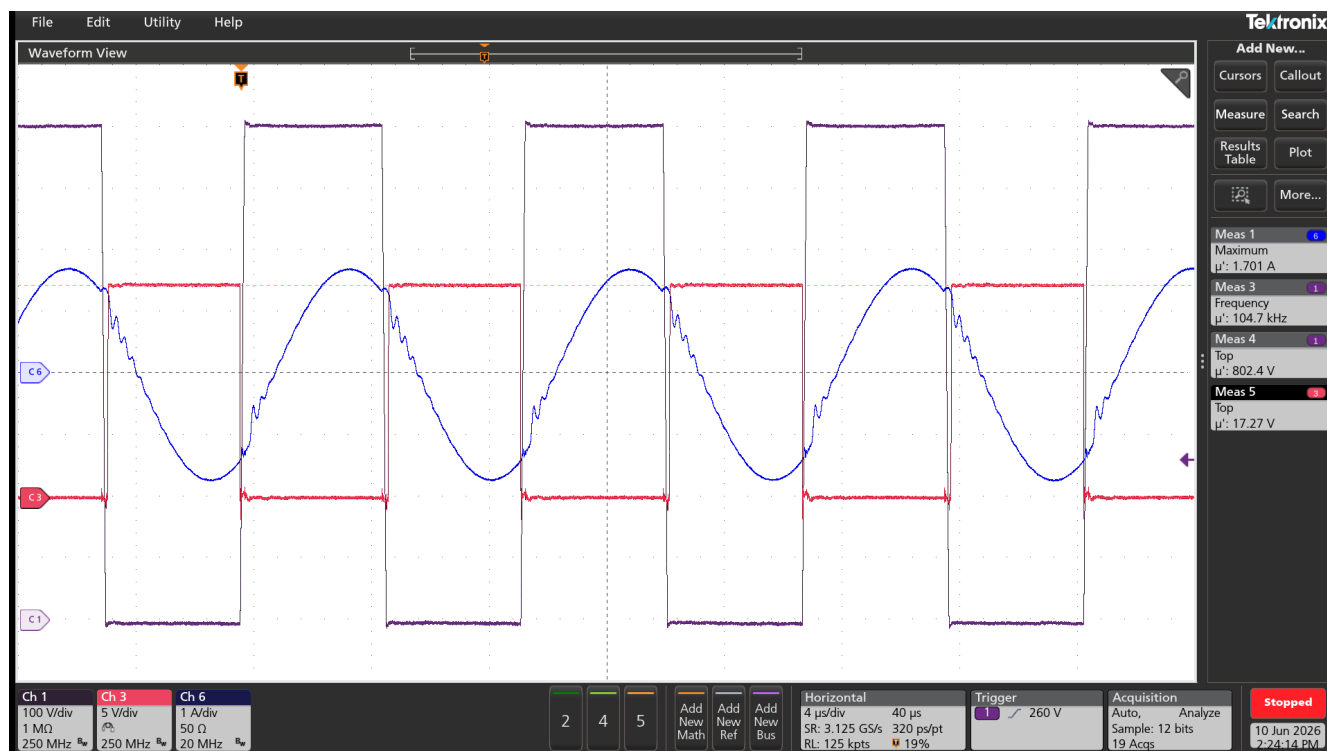


Figure 2-11. Switching Waveform at $V_{IN} = 800V$ and $V_{OUT} = 48V / 6.5A$. Ch1: SW, CH3: LO, CH6: I_{RES}

Figure 2-12 shows the efficiency result of the power transfer P_{out}/P_{in} .

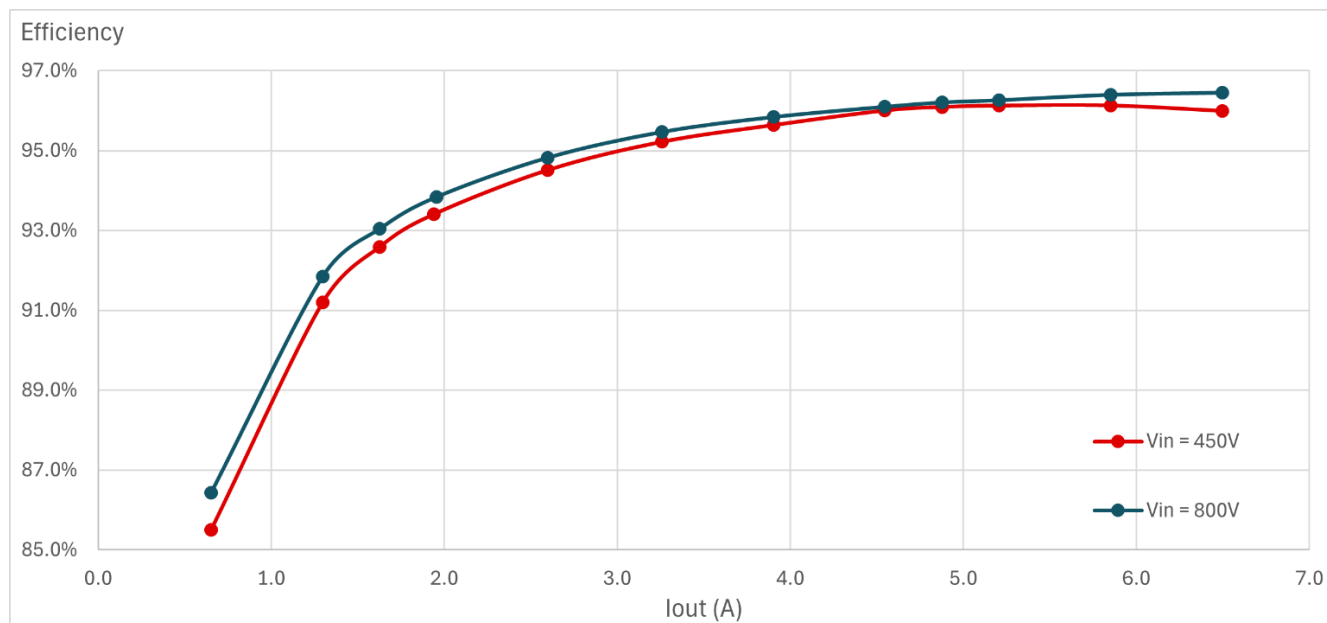


Figure 2-12. The Efficiency Result of PMP41133

3 Summary

When designing an 800V μ DCDC, there are challenges owing to lack of existing parts supporting such high voltage. There are a couple of things to consider: High voltage start-up and control needs to get switching node slew rate detection. To better regulate and extend the lifetime, ISOM8110 is used for feedback. Through this application note, the design concept is introduced and the way to achieve the design goal with good results.

4 References

1. Texas Instruments, [High Density Auxiliary Power Supply Using a SiC MOSFET for 800-V Traction Inverters](#), application note.
2. Texas Instruments, [PMP31342 Automotive 300W \$\mu\$ DC/DC Converter Reference Design Using Half-Bridge LLC](#), reference design.
3. Texas Instruments, [ISOM811x Reinforced Single-Channel Opto-Emulator With Analog Transistor Output](#), datasheet.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025