Application Note

System-Level ASIL B Compliance for MSPM0 MCUs

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ABSTRACT

This application note presents a core voltage monitoring implementation for the ASIL B derivatives of TI's MSPM0 microcontroller family. The described design supports the achievement of ASIL B functional safety integrity in automotive applications, in accordance with the requirements of ISO 26262.

This design fits many automotive applications that require housekeeping or data aggregation for a larger system and ASIL B body electronics and lighting systems. Designed for functional safety engineers, the proposed approach provides reliable voltage anomaly detection, robust fault handling mechanisms, and quantifiable diagnostic coverage metrics. The accompanying implementation guidelines enable engineers to efficiently integrate core voltage monitoring into MSPM0-based designs while meeting automotive safety standards.

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1 Introduction

The MSPM0 microcontroller integrates an LDO for core voltage generation. However, the absence of internal monitoring for the LDO output voltage needs an external monitoring mechanism to support functional safety compliance (ASIL B) in automotive applications. This document presents a cost-effective approach to implementing external monitoring, beginning with safety goal definition for the sub-system. The methodology explains the functional safety concept development and architectural design to meet functional and technical safety requirements. The detailed implementation guidance explains the specific safety mechanisms for voltage monitoring, fault detection, and system response strategies. The document concludes with a Failure Mode and Effects Analysis (FMEA) and Failure Modes, Effects, and Diagnostic Analysis (FMEDA) and presents quantitative safety metrics to demonstrate compliance with target ASIL B requirements.

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2 Detailed Description

2.1 Item definition

The item comprises a complete ASIL B safety-related system consisting of three primary functional elements: sensor subsystem, processing subsystem, and actuation subsystem. This architecture represents a generic safety function implementation applicable to various automotive applications requiring ASIL B integrity level. ASIL B compliance for a specific system depends on the design of the whole system.

2.2 Assumptions

The following assumptions have been made:

1. A power supply rail, V_{IN}, with nominal 3.3V is provided and
   a. not protected against undervoltage (UV) and overvoltage (OV) faults
   b. is also used for sensors and actuators circuits directly interfacing the MCU
2. All circuits connected to the rail have a recommended maximum supply voltage of at least 3.6V
3. V_{IN} does not exceed 42V

2.3 Hazard Analysis and Risk Assessment (HARA)

This document does not focus on hazard analysis and risk assessment. The safety goal requirements are assumed as described below as result of the HARA.

2.3.1 Safety Goal Definition

Safety Goal ID	Safety Goal	ASIL	Safe State	FTTI
SG_01	Avoid wrong MCU program execution	B	Microcontroller power-cycle	10ms

An ASIL B application must meet the following ISO 26262 requirements:

- SPFM ≥ 90%
- LFM ≥ 60%
- PMHF ≤ 100 FIT.

An FTTI of 10ms has been allocated to this safety mechanism. This value can be decreased if system-level timing requirements demand a lower value; however, the windowed watchdog refresh period defines the practical minimum FTTI.

2.3.2 Safe State "Microcontroller Power-Cycle"

Executing a microcontroller power-cycle as a fault reaction can induce a cascading safe state transition in the broader system — such as a temporary loss of communication with the supervising system layer. Once the initiating fault is resolved, the MCU is capable of self-recovery, which the higher-level instance can independently detect and confirm before restoring normal operation.

2.4 Functional Safety Concept

Overvoltage events can result from EMI, inadequate transient response to load dumps or inductive switching, ground shifts, or wiring faults.

When voltage exceeds operating limits, consequences range from temporary malfunction to permanent damage. MCU I/O pins risk exceeding absolute maximum ratings, causing irreversible device damage. The embedded LDO can suffer thermal stress or regulatory breakdown if input-output voltage differential is excessive, resulting in unregulated V_{CORE} and unstable operation. At the core level, overvoltage can trigger latch-up, Flash/EEPROM data corruption, premature memory wear, or complete silicon failure. Undetected overvoltage can cause uncontrolled system behavior, creating functional and safety hazards.

2.4.1 System Architecture

The MCU serves as the central processing unit of the system. All sensor and actuator circuits connect directly to the MCU. A vehicle battery powers the system. A DC/DC converter steps down the battery voltage to a regulated

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3.3V rail (V_{IN}). This unified supply provides power to the MCU and the logic supply for all connected sensors and actuators.

Using one unified supply rail means that all components always operate at the same voltage level. Operating at the same voltage level eliminates logic level mismatches between components and preventing leakage currents between powered and unpowered elements of the system.

Figure 2-1 shows the application sub-system within the scope of this document, indicated by the dotted line.

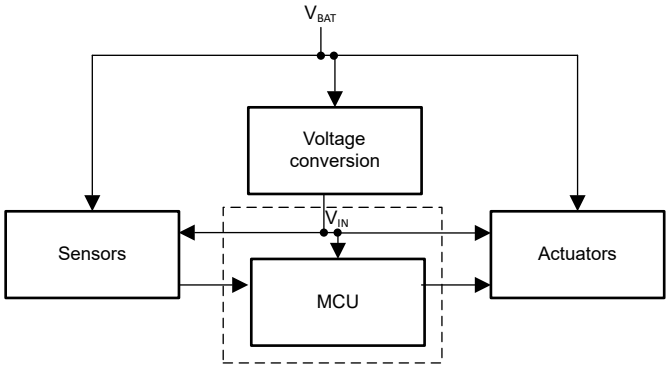

Figure 2-1. System Architectural Design

2.4.2 Safety Architecture

To satisfy safety goal SG_01, the MCU must operate within a well-conditioned environment that mitigates potential hazards. The system must guard against dangerous voltage conditions up to V_{BAT} to prevent hardware damage or erroneous operation, while also maintaining a well-regulated V_{DD} to facilitate reliable MCU operation. In addition, provide a properly driven and monitored reset signal to enable correct MCU initialization and recovery behavior. Furthermore, use a windowed watchdog mechanism to detect erroneous program execution, which can result from a variety of underlying faults.

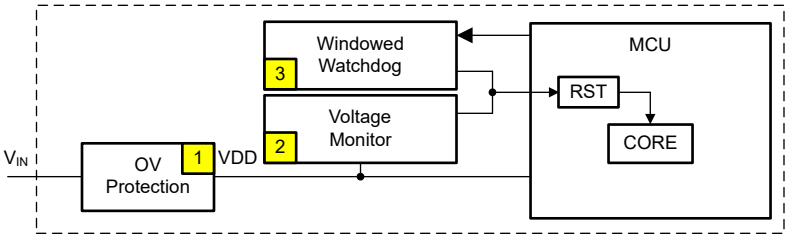

Figure 2-2. Safety Architectural Design

2.5 Technical Safety Concept

The concept presented here represents just one of several possible approaches. A discrete alternative – utilizing a shunt reference, resistor ladder, and comparators – is explored in the MSPM0 External VCore Monitoring for ASIL B Requirements application note.

2.5.1 Device Description

The key component of the design is the MCU, which is implemented using the MSPM03107-Q1. This device, along with all supporting components required to achieve ASIL B compliance, is introduced in the following sections.

2.5.1.1 MSPM0G3107-Q1

The MSPM0G3107-Q1 is an AEC-Q100 Grade 1 qualified automotive-grade microcontroller from TI's MSPM0G family designed for automotive functional safety applications. The device has ISO 26262 systematic and hardware compliance certification up to ASIL B. The device combines a 32-bit Arm® Cortex®-M0+ core running up to 80MHz with ECC-protected flash and parity-protected SRAM for memory integrity. Connectivity includes an integrated CAN-FD controller and four UARTs with hardware flow control. Dual 12-bit ADCs at 4MSPS

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with simultaneous sampling and a 12-bit DAC at 1MSPS deliver high-precision analog capability. Advanced timers with fault handling, dead-band insertion, and QEI/Hall sensor support enable robust motor and lighting drive control. Safety-critical integrity is reinforced by hardware AES-128/256, TRNG, and CRC engines and two watchdogs. The device is available in a 64-pin LQFP package with 5V-tolerant open-drain I/O.

See a list of all MSPM0 products compliant to ISO26262 on the Functional safety webpage.

2.5.1.2 TPS388R0x-Q1

The TPS388R0x-Q1 device family includes 2, 4 and 6 channel window supervisor ICs available in a 16-pin 3 × 3mm WQFN package, designed for systems operating on low-voltage supply rails with narrow margin supply tolerances. Each channel is configurable for OV, UV, or both in a window configuration, with fault outputs selectively mapped to the NRST/NIRQ pins. The device is AEC-Q100 qualified and functionally safety-compliant up to ASIL B (hardware) and ASIL D (systematic) with built-in self-test at startup. The device offers ±6mV threshold accuracy, and a sensing input voltage range from 0.2V to 5.5V with no external resistors required. All parameters are configurable via I2C or factory programmable. Additional features include internal glitch filtering, CRC and Packet Error Checking (PEC) and sequence logging.

Another variant, the TPS388C0x-Q1 family, includes a windowed watchdog.

2.5.1.3 TPS3842C011-Q1

The TPS3842C011-Q1 is an automotive-grade voltage supervisor belonging to the TPS3842-Q1 family, AEC-Q100 qualified for use in demanding automotive environments. The device monitors overvoltage (OV) conditions on a supply rail and asserts a RESET signal when the SENSE pin voltage crosses the defined threshold. The device supports a wide input voltage range from 1.9V to 42V, enabling direct connection to a 12V automotive battery. With ultra-low quiescent current of 850nA and high threshold accuracy, the device can support safety-critical applications. The part is rated functional safety capable, which means basic FIT rates, failure modes and the distribution is provided.

2.5.1.4 TPS22919-Q1

The TPS22919-Q1 is a high-performance load switch that is designed for automotive applications that require low-loss power distribution. The device operates from a 5.5V supply and can handle continuous currents up to 1.5A, while presenting an on-resistance of 100mΩ. These specifications minimize power dissipation and voltage drop across the switch. The device is packaged for robust operation and includes built-in current-limiting and thermal shutdown protection, providing safe operation under fault conditions.

2.5.2 Implementation Details

The application is built around the MSPM0G3107-Q1 microcontroller. This device supports both systematic and random hardware safety capabilities up to ASIL B in accordance with ISO 26262.

A common feature of MCUs in this class is the integrated low-dropout regulator (LDO), which generates the core voltage (V_{CORE}) rail. Since this voltage is typically not monitored internally, external measures must be implemented at the system level. If a UV or OV fault is detected on the V_{CORE} rail, a full MCU power-cycle is required, as the reset logic is dependent on this rail.

V_{DD} must be also continuously monitored for both UV and OV conditions. The MCU incorporates an integrated undervoltage lockout (UVLO) that responds to UV faults by triggering an internal reset. To prevent V_{DD} from exceeding 4.1V (MCU abs max) at the MCU and connected elements, two approaches are possible: voltage clamping, which requires large passive components for power dissipation, or power disconnection. This design adopts the power disconnection approach.

The MSPM0G3107-Q1 integrates two internal watchdog timers – a windowed watchdog and an independent watchdog – which can be used for program flow monitoring. The independent watchdog operates on an alternative clock source, providing sufficient independence from the main system clock.

Figure 2-3 show the implementation block diagram with these considerations.

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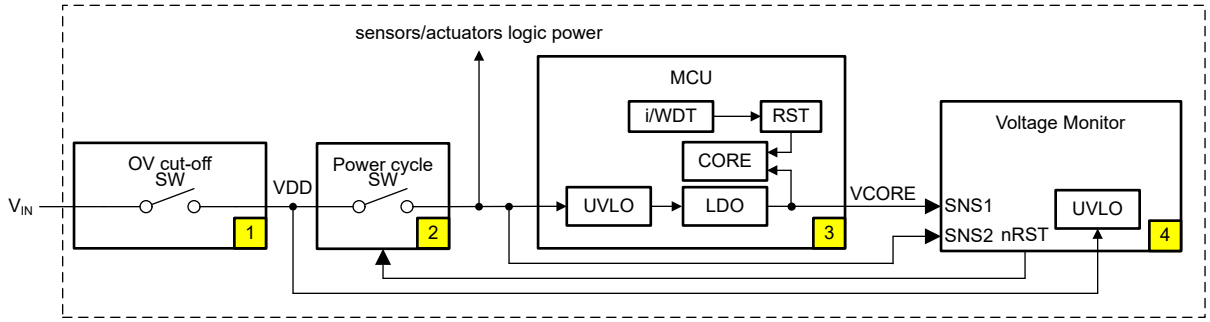

Figure 2-3. Implementation Block Diagram

The table below shows the description of the architectural design elements.

Element ID	Element Name	Description
1	OVP cut-off	Overvoltage monitor with cut-off to disconnect the power source
2	Power cycle cut-off	Power cycle of MCU to respond to V_{CORE} UV/OV faults
3	MCU	Microcontroller executing the program code
4	Voltage Monitor	Monitors MCU core voltage

2.5.2.1 Design Parameters

Table 2-1 shows the design parameter of the application sub-system.

Table 2-1. Parameters

Design Parameter	Parameter Value
Voltage input range (V_{IN})	3.3V ± approximately 3%
Input current	10mA + sensor or actuator circuits
Overvoltage protection circuit	
Overvoltage protection voltage threshold	3.9V ± approximately 5%
Fault input voltage, maximum	42V
Fault reaction time, maximum	7µs
Reset time delay, nominal	250µs
MCU voltage monitoring (V_{DD} and V_{CORE})	
Fault reaction time (V_{CORE} and V_{DD}), max	750ns
V_{CORE} OV threshold	1.40V ± 7.5mV
V_{CORE} UV threshold	1.29V ± 7.5mV
V_{DD} OV threshold	3.50V ± 0.5%
V_{DD} UV threshold	2.65V ± 0.5%
Microprocessor	
Integrated LDO output voltage range (max)	1.30V to 1.39V
VCORE operating range (max)	1.27V to 1.42V

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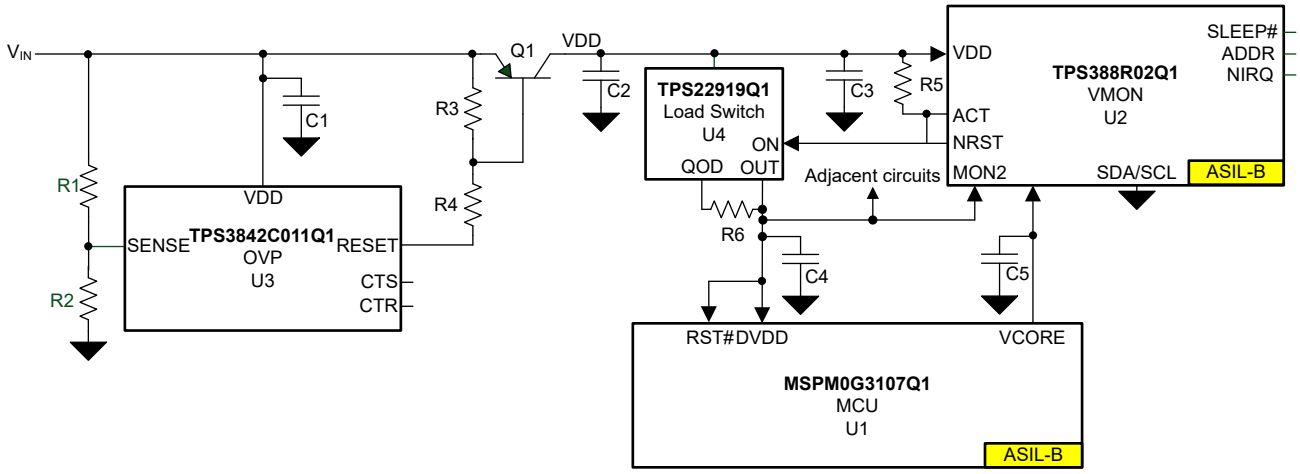

Figure 2-4. Implementation Details

2.5.2.2 Overvoltage Protection Circuit (OVP)

This design implements a two-stage OVP scheme. Use the TPS388R02-Q1 to complete the first stage, where the *MON2* pin monitors V_{DD}. If V_{DD} reaches or exceeds 3.5V, the TPS388R02-Q1 pulls the *NRST* output low, powering down the MCU using the TPS22919-Q1 load switch.

If V_{DD} rises further, the TPS3842C011-Q1 disconnects V_{IN} from the application at a nominal threshold of 3.9V through switch Q1. Extend the sense time delay and reset time delay can by connecting capacitors to the CTS and CTR pins, respectively. In this design, these pins are unpopulated, which applies the minimum sense time delay of 7µs and the minimum reset time delay of 250µs.

If overvoltage protection is not required, the OVP stage can be removed because this stage is independent from the remainder of the circuit. While the TPS388R02-Q1 can detect and respond to overvoltage conditions up to 5.5V, any voltage exceeding this level risks damaging the load switch, the voltage monitor, and the MCU.

2.5.2.3 Application Power Up and Power Down

At power-up, the TPS388R02-Q1 begins operating at 1.65V and asserts *NRST*, which keeps the MCU unpowered. The TPS388R02-Q1 reaches full operation at 2.81V then executes an internal built-in self-test (BIST). Any internal fault detected during this process keeps *NRST* asserted, which keeps the application in a safe state. Upon successful completion of the BIST, *NRST* is de-asserted. Since *NRST* and *ACT* are connected, this event simultaneously activates the TPS388R02-Q1 and enables the TPS22919-Q1 load switch, which then powers the MSPM0G3107-Q1.

At power-down, the MCU can operate down to 1.62V; however, below 2.6V the TPS388R02-Q1 can no longer monitor V_{CORE} and asserts *NRST* accordingly putting the MCU into safe state. If adjacent circuits require V_{DD} to remain above 2.6V, use the second monitoring channel (*MON2*) of the TPS388R02-Q1 to assert *NRST* at a higher voltage threshold.

2.5.2.4 TPS388R02-Q1 Software-less Operation

The TPS388R02-Q1 is pre-programmed to simplify system integration and eliminate the need for a startup software configuration. Request pre-programmed devices directly from Texas Instruments, even at low order quantities. I2C communication remains available and can be used alongside the pre-programmed configuration for additional flexibility.

2.5.2.5 V_{CORE} and V_{DD} Monitoring

In accordance with the MSPM0G3x0x-Q1 functional safety manual, V_{CORE} must be monitored externally via the *VCORE* pin. The MSPM0G3107-Q1 *VCORE* pin can source up to 100µA in RUN, SLEEP, and RESET modes, and up to 20µA in STOP and STANDBY modes. The *VCORE* pin has no sink capability. The nominal V_{CORE} voltage is 1.35V, with an absolute maximum range from 1.27V to 1.42V. The internal LDO provides an output range from 1.3V to 1.39V, offering 30mV of threshold headroom for UV and OV detection.

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The TPS388R02-Q1 monitor provides ±7.5mV accuracy and triggers an MCU power-down event (*NRST* low) upon detection of a UV or OV fault, holding this state until V_{CORE} returns to a valid range. The device supports two operating modes: Mode 1X, covering a range from 0.2V to 1.475V in 5mV steps with a maximum input leakage of 75nA over the full temperature range, and Mode 4X, covering 0.8V to 5.5V in 20mV steps with a maximum leakage of 4.3µA at 1.35V over the full temperature range.

Use mode 1X to measure V_{CORE} because this mode has finer threshold granularity, offering UV options of 1.28V, 1.285V, and 1.29V, and OV options of 1.40V, 1.405V, and 1.41V. Additionally, the lower leakage of Mode 1X leaves greater margin for other leakage sources such as the bypass capacitor and PCB effects over the product lifetime. Mode 4X, by contrast, offers one UV threshold of 1.28V and one OV threshold of 1.40V.

The typical *VCORE* bypass capacitor value is 470nF (see the MSPM0G310x-Q1 datasheet). Higher capacitor values improve disturbance immunity; however, higher values also affect V_{DD} bypass requirements, boot time, and UV/OV detection time, as illustrated in the table below.

V_{CORE} Pin Capacitor (C4)	Boot Time	V_{DD} Pin Capacitor (C3)	UV and OV Detection Time
470nF	300µs	10µF	1µs
2.34µF	450µs	50µF	5µs
4.7µF	600µs	100µF	10µs

The combination of a larger bypass capacitor and monitoring thresholds set close to the LDO output voltage range — UV at 1.29V and OV at 1.40V — contributes positively to reducing UV and OV fault detection time, enabling a faster response to voltage anomalies on the monitored rail.

If V_{CORE} is violated, a full power cycle of the MSPM0G3107-Q1 is required. During this event, *NRST* is asserted (low) and the TPS22919-Q1 disconnects the power supply from the MCU. NRST low also deactivates the TPS388R02-Q1 as *NRST* and *ACT* are tied together.

The TPS388R02-Q1 then waits for the preset *NRST* delay time before de-asserting *NRST* (high). This transition reactivates the TPS388R02-Q1 (*ACT* high). After the TOUT_SEQ time (see the TPS38800-Q1 and TPS388R0-Q1 datasheet), the device resumes full operation.

A valid MCU power cycle is achieved when V_{DD} falls below 0.9V for a minimum duration of 100µs. Depending on the capacitance values selected for *VCORE* (C5) and *VDD* (C4), size the reset delay time of the TPS388R02-Q1 and the discharge resistor R6 accordingly to produce correct power cycle behavior.

The circuit does not incorporate a dedicated measure to detect V_{DD} dropping low during a power cycle event. If this capability is required, address the multi-point fault by preventing the NRST node from transitioning high while the output of the TPS22919-Q1 remains elevated.

2.5.3 Monitoring Mechanisms

2.5.3.1 Monitoring VIN Supply Rail for OV Fault Including Protection

An OVP circuit is implemented to monitor the V_{IN} supply rail. When the input voltage exceeds the defined threshold of 3.9V, the OVP circuit automatically disconnects the application from the power source, thereby preventing damage due to overvoltage conditions.

2.5.3.2 Monitoring MCU Supply Voltages for UV or OV Faults

The TPS388R02-Q1 device provides continuous UV/OV monitoring for both the MCU V_{DD} and V_{CORE} supply rails. If the device detects a UV or OV fault on either rail, the device transitions to a safe state to maintain system integrity under abnormal voltage conditions.

2.5.3.3 Monitoring CPU processing Unit Program Flow

Program flow monitoring is achieved through two embedded watchdog timers: the Windowed Watchdog Timer (WWDT) and the Independent Watchdog Timer (IWDT). The IWDT operates from a dedicated, independent clock source, providing clock independence from the main CPU clock and enhancing fault detection coverage. Use the TPS388C02-Q1 variant if physical separation between the MCU and the watchdog timer is required. This device integrates a windowed watchdog into an external device.

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2.5.4 FMEA

Element	Sub-element	Function of sub-element	Failure mode	Failure effect	SGV	Failure cause	Measure to control or detect fault
MCU	CPU	SW execution	Instruction flow not executed, unintended instruction flow, incorrect instruction flow timing	Unintended program execution	SPF	Alpha particle or internal fault	(Independent) integrated or external windowed watchdog timer
MCU	CPU	SW execution	Incorrect Instruction flow result	Wrong calculation, wrong program sequence, wrong SP, and more.	SPF	Alpha particle or Internal fault	Plausibility check, software test functions, built-in checks
MCU	Watchdog	Monitors MCU program sequence	Watchdog does not reset when timing is violated	Wrong program execution	MPF	Watchdog fault	None
MCU	Watchdog	Monitors MCU program sequence	Watchdog reset when timing is correct	Transition to safe state	SF	Watchdog fault	-
MCU	LDO	Core voltage generation	Voltage out of spec (UV or OV)	Core voltage out of range	SPF	Reference drift, PFET short/ open	External voltage monitor
MCU	UV lockout circuit	Reset MCU if below V_{DD} below UVLO voltage	No MCU reset	MCU operates with invalid V_{DD} (and V_{CORE})	MPF	Internal fault	Redundant UVLO circuit and V_{DD} sensing in voltage monitor
OV cut-off	Voltage monitor	Monitors VIN against overvoltage	Monitor does not detect overvoltage/RST not asserted	Overvoltage at downstream devices	MPF	Resistor or reference drift/ open/short	None
OV cut-off	Voltage monitor	Monitors VIN against overvoltage	Monitor falsely detects overvoltage/ RST falsely asserted	Transition to safe state	SF	Resistor or reference drift/ open/short	-
OV cut-off	Switching element	Disconnects power source from application	Switch does not open	Overvoltage at downstream devices	MPF	Resistor drift/open/short, BJT fail short	None
OV cut-off	Switching element	Disconnects power source from application	Switch does not close	Transition to safe state	SF	Resistor drift/open/short, BJT fail open	-
Voltage monitor	VMON channel	V_{CORE} supply monitor	Monitor does not assert NRST in UV or OV fault	V_{CORE} out of range	MPF	Internal failure, reference drift	BIST
Voltage monitor	VMON channel	V_{CORE} supply monitor	Monitor falsely detects UV or OV	MCU power cycle	SF	Internal failure, reference drift	-
Voltage monitor	VMON channel	V_{DD} supply monitor	Monitor does not assert NRST in UV or OV fault	V_{DD} out of range	MPF	Internal failure, reference drift	BIST
Voltage monitor	VMON channel	V_{DD} supply monitor	Monitor falsely detects UV or OV	MCU power cycle	SF	Internal failure, reference drift	-
Voltage monitor	UV lockout circuit	Reset MCU if below V_{DD} below UVLO voltage	NRST not asserted	MCU operating without V_{CORE} monitoring	MPF	Internal fault	Redundant UVLO circuit in MCU and V_{DD} sensing
Voltage monitor	I/O circuit	Assert NRST, activation of circuit	NRST not asserted, ACT open	Device does not monitor (bypass)	MPF	Internal fault, ACT pin open	None
Load switch	Switching element	Connect V_{DD} to MCU	Switch does not open when commanded	MCU does not power down	MPF	Stuck-at, control pin open	None
Load switch	Switching element	Connect V_{DD} to MCU	Switch does not close when commanded	MCU does not power up	SF	Stuck-at, control pin open	-

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2.5.4.1 Safety Mechanisms

Multiple safety mechanisms are implemented within the system to detect and respond to random hardware faults. The following subsections describe each mechanism in detail.

2.5.4.1.1 SM1: MSPM0G3107-Q1 BIST and Software Test

The MSPM0G3107-Q1 incorporates safety mechanisms including, but not limited to, Cyclic Redundancy Check (CRC), Error Correction Code (ECC), Windowed Watchdog Timer (WWDT), and Independent Windowed Watchdog Timer (IWDT). In addition, software routines are periodically executed within the Fault Tolerant Time Interval (FTTI) to test safety-relevant application components and detect additional internal faults. For further details, refer to the MSPM0G3x0x-Q1 functional safety manual.

2.5.4.1.2 SM2: TPS388R02-Q1 BIST and Internal Fault Detection

At startup, the TPS388R02-Q1 automatically executes a BIST to verify internal functional integrity. Diagnostics can have continuous, periodic, or one time execution depending on the BIST mechanism. Upon fault detection, the TPS388R02-Q1 asserts the NRST signal to reset the MCU and initiates the safe state. For further details, see the *TPS388 Functional Safety Information* (available upon request).

2.5.4.1.3 SM3: MSPM0G3107-Q1 V_{CORE} Monitoring

The V_{CORE} supply rail of the MSPM0G3107-Q1 is continuously monitored for UV/OV conditions by the TPS388R02-Q1 so that the MCU core voltage remains within the defined safe operating range. This safety mechanism initiates a power cycle through TPS22919-Q1.

2.5.4.1.4 SM4: MSPM0G3107-Q1 V_{DD} Monitoring

The V_{DD} supply rail of the MSPM0G3107-Q1 is continuously monitored by the TPS388R02-Q1 for UV/OV faults. This safety mechanism initiates a power cycle through TPS22919-Q1.

In addition, the MSPM0G3107-Q1 integrated Brown-Out Reset (BOR) circuit provides a secondary layer of protection by placing the MCU into reset if the V_{DD} voltage falls below the defined threshold.

2.5.4.1.5 SM5: Overvoltage Protection

Overvoltage protection of the VIN supply rail is implemented across two operating ranges:

Above 3.5V: The TPS388R02-Q1, in conjunction with the TPS22919-Q1 load switch, powers down the MSPM0G3107-Q1 to prevent operation outside the defined safe voltage window.

Above 3.9V: The TPS3842C011-Q1 monitors the V_{IN} rail and automatically disconnects the power source from the application when the input voltage reaches or exceeds 3.9V nominal.

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2.6 Technical Safety Requirements

2.6.1 FMEDA for Safety Goal SG_01

Component Name	Failure rate/ FIT	Safety-related component ?	Failure Mode (FM)	FM distribution	FM potentially violating SG without safety mechanisms (SM)?	SM preventing FM from violating SG?	FM coverage with respect to violation of SG	Residual and SPF failure rate/FIT	FM violating SG combined with independent failure of another component?	Detection means? SM(s) preventing latent FM?	FM coverage with respect to latent failures	Latent Multiple-Point Fault failure rate/FIT
M0G3107QRGZRQ1	RESTRICTED	YES	Permanent	100%	X	SM1, SM3-5	>90%	RESTRICTED	X	SM1	> 90%	RESTRICTED
	RESTRICTED		Transient	100%	X	SM1, SM3-5	> 99%	RESTRICTED	X	SM1	100%	0
TPS388R02001RTERQ1	RESTRICTED	YES	Permanent	100%					X	SM2	99.71%	RESTRICTED
	RESTRICTED		Transient	100%					X	SM2	100%	0
TPS3842C011-Q1	3	YES	Reset fails to trip	35%					X	-	0%	1.05
			Reset false trip	25%								
			Reset trip out spec	30%					X	-	50%	0.45
			Reset delay out spec	10%						-		
TPS22919-Q1	3	YES	VOUT stuck on	25%					X	-	0%	0.75
			VOUT open or Hi-Z	25%								
			VOUT outside spec	35%	X	SM4	99%	0.011				
			QOD stuck on	5%								
			QOD stuck off	5%					X	-	0%	0.15
			Pin to pin short	5%					X	SM2	100%	0
Q1	4	YES	Short	80%					X	-	0%	3.2
			Open	20%								
R1	0.2	YES	Open	40%					X	-	0%	0.08
			Drift	60%					X	-	50%	0.06
R2	0.2	YES	Open	40%								
			Drift	60%					X	-	50%	0.06
R3	0.2	YES	Open	40%					X	-	0%	0.08
			Drift	60%								
R4	0.2	YES	Open	40%								
			Drift	60%								
R5	0.2	YES	Open	40%								
			Drift	60%								

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Component Name	Failure rate/ FIT	Safety-related component ?	Failure Mode (FM)	FM distribution	FM potentially violating SG without safety mechanisms (SM)?	SM preventing FM from violating SG?	FM coverage with respect to violation of SG	Residual and SPF failure rate/FIT	FM violating SG combined with independent failure of another component?	Detection means? SM(s) preventing latent FM?	FM coverage with respect to latent failures	Latent Multiple-Point Fault failure rate/FIT
R6	0.2	YES	Open	40%					X	-	0%	0.08
			Drift	60%								
C1	2	YES	Short	65%								
			Open	10%					X	SM4	99%	0.002
			Drift	25%								
C2	2	YES	Short	65%								
			Open	10%					X	SM4	99%	0.002
			Drift	25%								
C3	2	YES	Short	65%								
			Open	10%								
			Drift	25%								
C4	2	YES	Short	65%								
			Open	10%	X	SM4	99%	0.002	X	SM4	100%	0
			Drift	25%								
C5	2	YES	Short	65%								
			Open	10%	X	SM4	99%	0.002	X	SM4	100%	0
			Drift	25%								

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2.6.1.1 Notes

The FMEDA table structure is derived from the example calculation provided in ISO 26262-5:2018, Annex E.

The MSPM0G3107-Q1 and TPS388R02-Q1 are ISO 26262-compliant devices for which a full FMEDA is available upon request. The results of the Die FMEDA for both devices are incorporated into the system-level FMEDA presented above.

The TPS3842C011-Q1 is classified as a functional safety capable device. For more associated functional safety documentation, see TPS3842-Q1 Functional Safety FIT Rate, FMD and Pin FMA.

FIT rates and failure mode distributions for resistors, capacitors, and transistors are sourced from Birolini's (2017) *Reliability Engineering*.

The activation of the OVP circuit is conditional upon the connected power supply generating an overvoltage event, which constitutes the first fault in a dual-fault scenario. Since the OVP circuit is only exercised under this fault condition, the correct operation cannot be verified during normal system operation because no test circuit is implemented. This behavior satisfies the definition of a latent fault as defined in the ISO 26262 functional safety standard.

A diagnostic coverage of 50% is applied to generalized failure modes, such as parameter drift, where no specific detection mechanism is present. For these failure modes, an equal distribution of 50% safe faults and 50% dangerous faults is assumed.

The FMEDA scope is limited to the Die FMEDA only. A pin FMEDA must be performed separately for each device as applicable to the specific system implementation.

2.6.2 Quantitative Results

The FMEDA table above provides the following functional safety results for the sub-system.

Based on IEC/TR 62380	**Die**	
	Permanent	**Transient**
Single Point Fault Metric - SPFM	>99%	>99%
Latent Fault Metric - LFM	>70%	NA

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3 Summary

The proposed design fulfills the system-level functional safety requirements necessary to achieve ISO 26262 compliance with the MSPM0G3107-Q1 up to ASIL B. The system design to determines whether a specific system is ASIL B compliant. The FMEDA results presented in this document are intended to be integrated into a higher-level system FMEDA to support the functional safety assessment of the final application.

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4 References

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3. Texas Instruments, *MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual*, user guide
4. Texas Instruments, TPS388 Functional Safety Information (available upon request)
5. Texas Instruments, *TPS3842-Q1 Functional Safety FIT Rate, FMD and Pin FMA*, functional safety information
6. Alessandro Birolini, Reliable Engineering, 8th Edition, ISBN 978-3-662-54208-8
7. Texas Instruments, *MSPM0G310x-Q1 Automotive Mixed-Signal Microcontrollers With CAN-FD Interface*, datasheet
8. Texas Instruments, *TPS38800-Q1/TPS388R0-Q1 Multichannel Overvoltage and Undervoltage I2C Programmable Voltage Supervisor*, datasheet
9. Texas Instruments, *Prefiltered list of ISO26262-compliant MSPM0x devices*, webpage
10. Texas Instruments, *MSPM0 External VCore monitoring for ASIL B requirements*, application note

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