Application Note

A Guide to USB3.1 Gen1 SuperSpeed Host Transmit Electrical Compliance

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ABSTRACT

This application note describes how to perform USB 3.0 (SuperSpeed, 5Gbps) Host TX electrical compliance testing on Jacinto SoCs (TDA4AH/VH,TDA4VP/AP) using Linux commands. This procedure covers writing the xHCI PORTSC compliance register, configuring the USB PHY for CP0 and CP1 pattern generation, enabling Spread Spectrum Clocking (SSC), and capturing results with a LeCroy oscilloscope.

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Trademarks

1 Introduction

USB 3.1 Gen1 (SuperSpeed, 5Gbps) electrical compliance testing verifies that a device-under-test (DUT) meets the eye-diagram, jitter, voltage-margin, and output-amplitude requirements defined in the USB 3.1 specification and the USB-IF Compliance Test Specification (CTS).

The application note describes how to force a Jacinto SoC USB 3.0 xHCI host controller into compliance mode using either (a) direct memory-mapped register writes via devmem2, or (b) the Linux xHCI sysfs debug interface. Furthermore, the precise register fields involved, including the RX Detect state, Port Link State (PLS), Link Write Strobe (LWS), and the USB PHY register write required to enable the CP1 compliance pattern along with the SERDES PHY register to enable the SSC(Spread Spectrum Clocking) are explained in detail. Skip to Compliance Procedure for Host TX compliance procedure on the TI Automotive Processor SoCs.

2 USB 3.1 Compliance Mode: Theory of Operation

2.1 Acronyms and Definitions

Table 2-1. Acronyms and Definitions

Term	Definition
USB	Universal Serial Bus
CP0..CP1	Compliance Pattern 0..1 — defined USB 3.0 test signal sequences
CTS	Compliance Test Specification (USB-IF)
DUT	Device Under Test
LFPS	Low-Frequency Periodic Signaling — used for link detection and state transitions
xHCI	Extensible Host Controller Interface — USB 3.0/3.1 host controller specification
LWS	Link Write Strobe — xHCI PORTSC bit 16 that gates PLS writes
PLS	Port Link State — 4-bit field in xHCI PORTSC register [8:5]
PORTSC	Port Status and Control register — xHCI §4.19.7
PP	Port Power — PORTSC bit 9
RX Detect	USB 3.0 LTSSM state where TX probes for a far-end receiver; PLS = 5
SERDES	Serializer/Deserializer — analog PHY for high-speed serial links
SSC	Spread Spectrum Clocking — modulates TX clock to reduce peak EMI; separate from CP1
SS	SuperSpeed - the data rate USB supports(5Gbps). Interchangebly referred to as USB3.0, USB3.1 Gen1 or USB3.2 Gen1 but all refer to the same link rate of 5Gbps.

2.2 LTSSM and RX Detect

The USB 3.0 Physical and Link Layers implement the Link Training and Status State Machine (LTSSM). When the port is powered but no device is attached, the xHCI controller places the link in the Rx.Detect state (PLS = 5). In Rx.Detect, the transmitter periodically asserts a small DC voltage on the differential pair and monitors for a termination load that indicates a far-end receiver is present. LFPS bursts are also generated during this phase and are visible on an oscilloscope when a cable is connected or removed.

Power-On Reset ->

Rx.Detect -- No receiver (PLS = 5). TX probes for far-end termination.

--LFPS bursts generated

--Receiver detected

Polling -> Link training in progress

-- Link partner responds -----> U0 (Active, PLS = 0)

-- No Ping.LFPS / no partner --> Enters Compliance (PLS = 10 = 0xA)

2.3 Compliance Mode Entry Methods

Two software methods are supported on Jacinto SoCs:

- **devmem2 (direct MMIO write)** — Write the xHCI PORTSC register with PLS = 10 (Compliance), PP = 1, and LWS = 1. This bypasses the LTSSM timeout and immediately forces the link into compliance. This is the preferred method for validation.
- **sysfs echo compliance** — Write the string "compliance" to the xHCI debugfs portsc node. The xHCI driver translates this to the same PLS = 10 register write.

2.4 Register Reference

2.4.1 xHCI PORTSC: Port Status and Control Register

Table 2-2. PORTSC Register Addresses

SoC	USB Instance	PORTSC Address (USB3 Port 2)
TDA4VH/TDA4AH/TDA4AP/TDAVP	USB0	0x06010490

Note

Offset 0x490 from the xHCI MMIO base is the Port 2 PORTSC register. Port 1 PORTSC (USB2 HS) is at offset 0x480. The USB3 SuperSpeed port is Port 2 in the Jacinto xHCI implementation.

2.4.2 PORTSC Bit-Field Description (USB 3.0 — xHCI Spec §4.19.7)

Table 2-3. PORTSC Bit-Field Description

Bits	Field	Reset	Description
31	WPR	0	Warm Port Reset.
30	DR	—	Device Removable.
29:28	RsvdZ	0	Reserved. Write as zero.
27	WOE	0	Wake on Over-current Enable.
26	WDE	0	Wake on Disconnect Enable.
25	WCE	0	Wake on Connect Enable.
24	CAS	0	Cold Attach Status (USB 3.1).
23	CEC	0	Port Config Error Change (sticky; clear by writing 1).
22	PLC	0	Port Link State Change (sticky; clear by writing 1).
21	PRC	0	Port Reset Change (sticky; clear by writing 1).
20	OCC	0	Over-current Change.
19	RsvdZ	0	Reserved.
18	PEC	0	Port Enable/Disable Change.
17	CSC	0	Connect Status Change (sticky).
16	LWS	0	Link Write Strobe. Must be 1 for PLS writes to take effect. If LWS = 0, writes to PLS[3:0] are silently ignored by hardware.
15:14	PIC	0	Port Indicator Control.
13:10	Port Speed	—	Negotiated port speed (encoded per xHCI Table).
9	PP	—	Port Power. Must be 1 for USB3 operation.
8:5	PLS	—	Port Link State. Controls and reflects LTSSM state. See Table 2-4.
4	PR	0	Port Reset.
3	OCA	0	Over-current Active.
2	RsvdZ	0	Reserved.
1	PED	0	Port Enabled/Disabled.
0	CCS	0	Current Connect Status.

2.4.3 PLS Encoding: USB 3.0 Link States

Table 2-4. PLS Encoding: USB 3.0 Link States

PLS[3:0]	Decimal	State	Description
0000	0	U0	Active — normal operation
0001	1	U1	U1 power-save state
0010	2	U2	U2 deeper power-save
0011	3	U3	Suspend (deepest link state)
0100	4	Disabled	Link disabled
0101	5	Rx.Detect	Polling for far-end receiver. Default idle state — no device connected. LFPS bursts generated on connect/disconnect events.
0110	6	Inactive	Link in inactive state
0111	7	Polling	Active link training / negotiation
1000	8	Recovery	Link recovery in progress
1001	9	Hot Reset	In-band warm reset
1010	10 (0xA)	Compliance	Compliance mode — transmits CP0 by default; CP1 requires additional USB PHY write (Section 6.2).
1011	11	Loopback	Loopback test mode
1100–1111	12–15	Reserved	—

2.4.4 Verifying RX Detect Before Compliance Entry

The port must be in Rx.Detect (PLS = 5) before issuing the compliance write. Read PORTSC and inspect bits [8:5]:

TDA4xH/TDA4xP

$ devmem2 0x06010490 w

Bits [8:5] = 0101 => Rx.Detect (ready for compliance entry)

Bits [8:5] = 0000 => U0 (device connected; disconnect first)

2.4.5 Compliance Write Value Decode: 0x0a010340

The following 32-bit value is written to PORTSC to force compliance mode entry:

Write value: 0xa010340

Bit 31-24 = 0x0A = 0000_1010 => WCE = 1 (bit 25), WOE = 1 (bit 27) [preserve wake enables]

Bit 23-16 = 0x01 = 0000_0001 => LWS = 1 (bit 16) [ENABLE PLS write]

Bit 15-08 = 0x03 = 0000_0011 => PP = 1 (bit 9), PLS[3] = 1 (bit 8) [Port Power ON, PLS MSB]

Bit 07-00 = 0x40 = 0100_0000 => PLS[1] = 1 (bit 6) [PLS second bit]

PLS[3:0] = { bit8, bit7, bit6, bit5 } = { 1, 0, 1, 0 } = 0b1010 = 10 => Compliance

PP = 1 => Port Power ON

LWS = 1 => PLS write is valid and takes effect immediately

Note

Without LWS = 1 (bit 16), hardware silently ignores the PLS field. A common mistake is writing only PLS = 0xA without LWS, resulting in no state change.

2.5 Compliance Pattern CP1 and SSC

Compliance Pattern 1 (CP1) is defined in the USB 3.2 specification as a repeating alternating-bit pattern (101010..) transmitted at the full 5 Gbps line rate. Because adjacent bits alternate, the fundamental frequency of the resulting waveform is:

f_CP1 = BitRate / 2 = 5 Gbps / 2 = 2.5 GHz

CP1 aids in random jitter extraction by isolating the deterministic jitter (DJ) component and helps with Spread Spectrum Clocking (SSC) analysis.

On Jacinto SoCs, the SERDES PHY does not automatically generate CP1 solely from the xHCI PORTSC compliance write. A separate USB PHY register write is required to instruct the analog TX to output the 1010-clock pattern. The validated register write is shown in Section 6.2.

The SSC is not enabled by the CP1 USB register write described in this document. The SSC (Spread Spectrum Clocking) is a separate TX clock modulation feature that helps reduce peak Electromagnetic Interference (EMI). The USB specification requires that the USB superspeed devices support triangular modulation profile, with SSC modulation frequency between 30-33KHz, and downspread with upto 5000ppm (0.5% depth). See the following application note for more details on the SSC.

2.5.1 USB PHY Register — CP1 (Clock Pattern)

This USB PHY register write instructs the analog TX block to output the CP1 compliance pattern. The register must be written after the PORTSC compliance write.

2.5.2 Register Address

Table 2-5. USB PHY CP1 Register Address

SoC	USB PHY Register	Write Value	Purpose
TDA4xH/TDA4xP	0x0601812C	0x18230c10	USB PHY — CP1 pattern select register

2.5.3 CP1 Write Value Decode: 0x18230c10

The USB PHY register fields are defined in the internal TI SoC Technical Reference Manual. The validated value for CP1 pattern output is:

Write value: 0x18230c10

Binary: 0001_1000_0010_0011_0000_1100_0001_0000

Effect: Configures SERDES analog TX to output the CP1 pattern

(alternating 1010 bits => 2.5GHz fundamental frequency at 5Gbps)

Key field (per TRM):

Bit 24:21 = 1 => Force compliance pattern (CP1)

= 0 => Force compliance pattern (CP0) - default

NOTE: CP1 *does NOT enable SSC (Spread Spectrum Clocking). SSC is a separate TX reference clock modulation feature. This register write selects CP1 as the analog TX output; however, does not enable or disable SSC.*

3 Compliance Procedure — TDA4VH/AH/TDA4AP/VP

3.1 Hardware Requirements

Table 3-1. Hardware Requirements

Item	Purpose
TDA4VH/ TDA4VP EVM	DUT — SoC hosting the USB3 xHCI controller
USB 3.0 Host Test Fixture-1 (Intel)	Intel's USB3.0 Host fixture -1 with type-A connector to interface to the DUT;
High-speed Oscilloscope (LeCroy)	Captures eye diagram, jitter, TX amplitude at 5Gbps / 2.5GHz (CP0 and CP1)
SMA cables and probes	Signal path from test fixture to the scope

3.2 Software Requirements

Table 3-2. Software Requirements

Component	Details
Linux	TI SDK 11.02.00.04
devmem2	Raw 32-bit MMIO read/write; available in Yocto/buildroot SDK
debugfs	Mounted at /sys/kernel/debug; required for sysfs echo compliance method

Install the TI Processor SDK Linux 11.02.00.04 onto the SD card. Use the wget command in a Linux terminal to download the installer, then make the downloaded file executable with the command chmod +x. Use the sudo ./ command to execute the file which extracts the contents into the specified directory.

https://dr-download.ti.com/software-development/software-development-kit-sdk/MD-lOshtRwR8P/11.02.00.04/ti-processor-sdk-linux-adas-j784s4-evm-11_02_00_04-Linux-x86-Install.bin

To install the SDK onto the SD card, follow the installation instructions at:

https://software-dl.ti.com/jacinto7/esd/processor-sdk-linux-j784s4/11_02_00_04/exports//docs/linux/Overview/Processor_SDK_Linux_create_SD_card.html#create-sd-card-with-custom-images

Mount debugfs if not already present:

mount -t debugfs none /sys/kernel/debug

3.3 EVM Setup

The Host USB3.0 test fixture-1 connects to the EVM at the type-C connector through a type-C to type-A connector. Set the DIP switch SW7/SW11 to SD card boot mode. The DIP switch must be set to DFP mode. The CTS requires a 3m cable and host test fixture-2 (5in trace) which is not part of the setup here, however, the LeCroy SigTest framework compensates for the long channel by channel emulation.

SD Card Boot: The processor will attempt to boot from image on SD Card.

SW7[8:1] = 0000 0000 (Default)

SW11 [8:1] = 0100 0001 (Default)

Figure 3-1. EVM SD Card boot mode switch settings

SW2.[4:3]	OFF:OFF	USB Type C Mode Selection	Set Mode for USB Type C interface (USB0): '00' (OFF/OFF) = DFP (Downstream Facing Port) '01' (OFF/ON) = DRP (Dual Role Port) '1X' (ON, Don't Care) = UFP (Upstream Facing Port)

Figure 3-2. EVM USB-C Switch Setting

Connect the Main UART terminal of the EVM to the PC and open the first of the four COM ports on the TeraTerm terminal. Configure the serial port with the speed of 115200kbps instead of the default 9600kbps. Power on the EVM and the SoC now boots from the SD card.

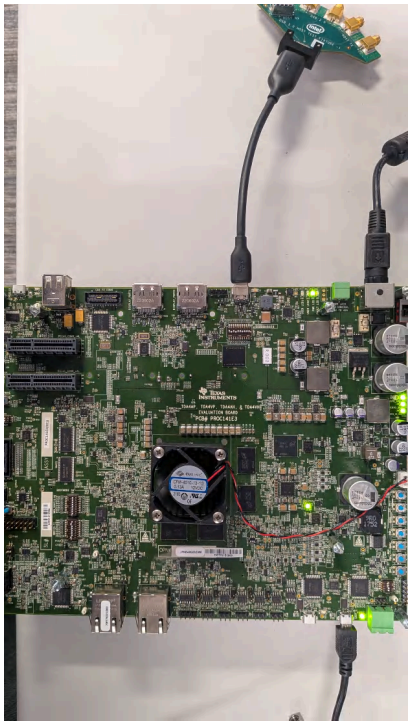

Figure 3-3. EVM Setup

3.4 Compliance Pattern Reference

Table 3-3. Compliance Pattern Summary

Pattern	Signal Description	Measurement Use	How to Enter	Notes
LFPS	Low frequency Periodic signaling	Periodic signaling to meet the rise/ fall times, burst rate, and periodicity.	Direct test fixture connection or through the Echo compliance command	
CP0	Scrambled D0.0 at 5Gbps	Eye diagram, TX amplitude (VTX-DIFF), rise/fall time, TX jitter (Tj)	PORTSC write only (PLS = 10)	Not applicable
CP1	Clock pattern at Nyquist Frequency of 2.5GHz at 5Gbps	TX output voltage at max toggle frequency; TX Jitter, SSC analysis.	PORTSC write + USB PHY write (0x18230c10)	Enable SSC through SERDES PLL

3.5 LFPS: Low-Frequency Periodic Signaling

To force the SoC USB instance into Host TX compliance mode, follow the dts changes done as per figure 3-6. To generate the LFPS signal required for USB 3.0 Host TX compliance testing, write the compliance string to the xHCI debugfs node as shown below:

root@j784s4-evm: echo compliance > /sys/kernel/debug/usb/xhci/<tab>/ports/port02/portsc.

<tab>: Press tab to auto populate the USB instance number assigned by Linux for the host controller. (for e.g , this reads as xhci-hcd.11.auto).

The cat command reads back the PORTSC register, confirming the link is in Rx.Detect. Connect the USB test fixture and observe the LFPS signal on the oscilloscope:

root@j784s4-evm: cat /sys/kernel/debug/usb/xhci/xhci-hcd.11.auto/ports/port02/portsc

0x0a0002a0 Powered Not-connected Disabled Link:RxDetect PortSpeed:0 Change: Wake: WCE WOE

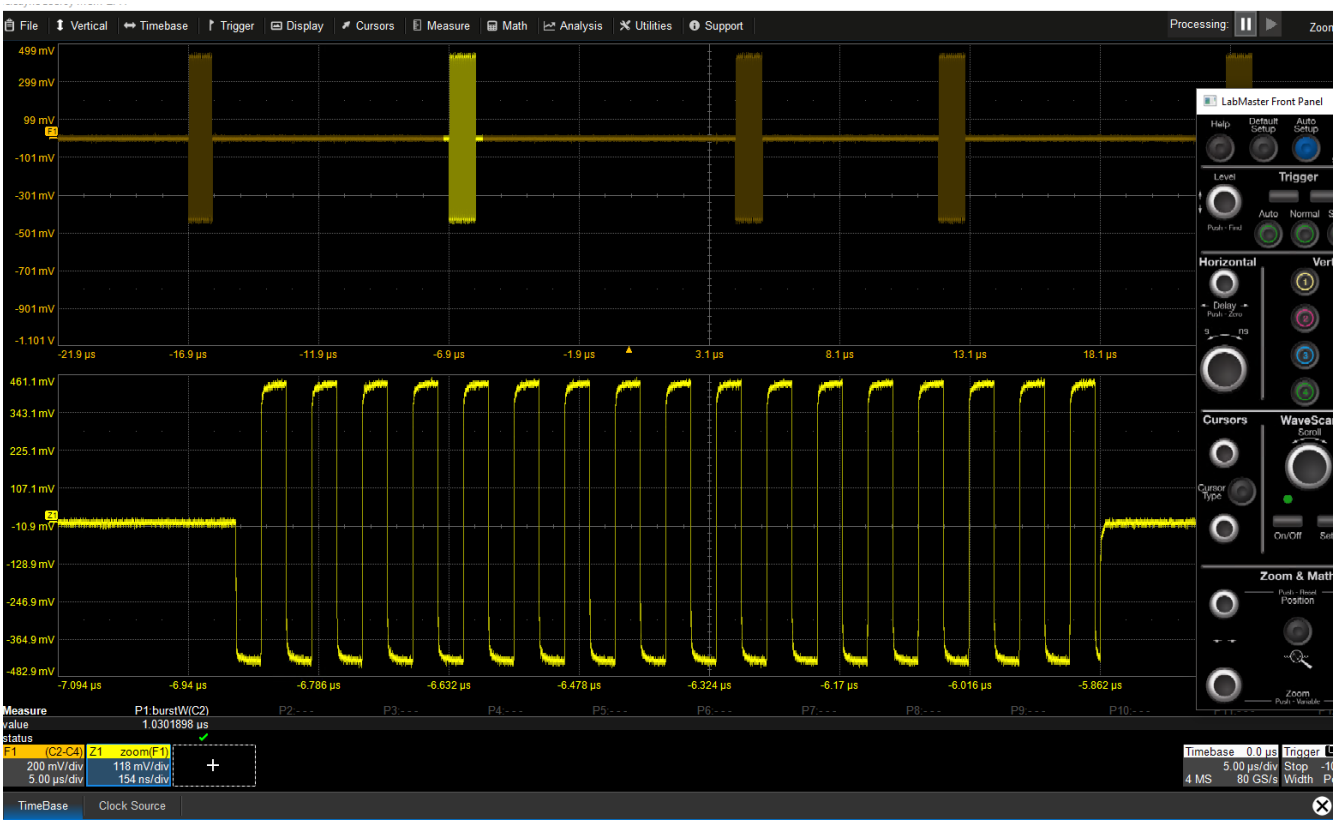

Figure 3-4. LFPS Signal Observed on Oscilloscope

3.6 Compliance Pattern 0 (CP0)

Compliance Pattern 0 (CP0) is a pseudo-random bit sequence pattern transmitted at 5.0Gbps without SKP sequences. CP0 is used to measure maximum jitter and minimum eye height against the USB 3.0 specification limits.

Pre-condition: The USB test fixture must be disconnected from the EVM. Boot the EVM from the SD card, allow Linux to start, and log in as root.

Step 1 : Verify port is in Rx.Detect:

$ devmem2 0x06010490 w

Expected: PLS bits [8:5] = 0101 (RX Detect)

If PLS = 0000 (U0), disconnect the device and re-read

Step 2: Force compliance mode (CP0):

$ devmem2 0x06010490 w 0x0a010340

PP=1, PLS=Compliance(10), LWS=1

Step 3: Write USB PHY CP0 register:

$ devmem2 0x0601812c w 0x18030c10

Step 4 : Verify compliance entry:

$ devmem2 0x06010490 w

PLS bits [8:5] now reads 1010 (Compliance)

Step 5: Connect compliance load board.

Observed signal: CP0 pattern (Scrambled D0.0 at 5Gbps).

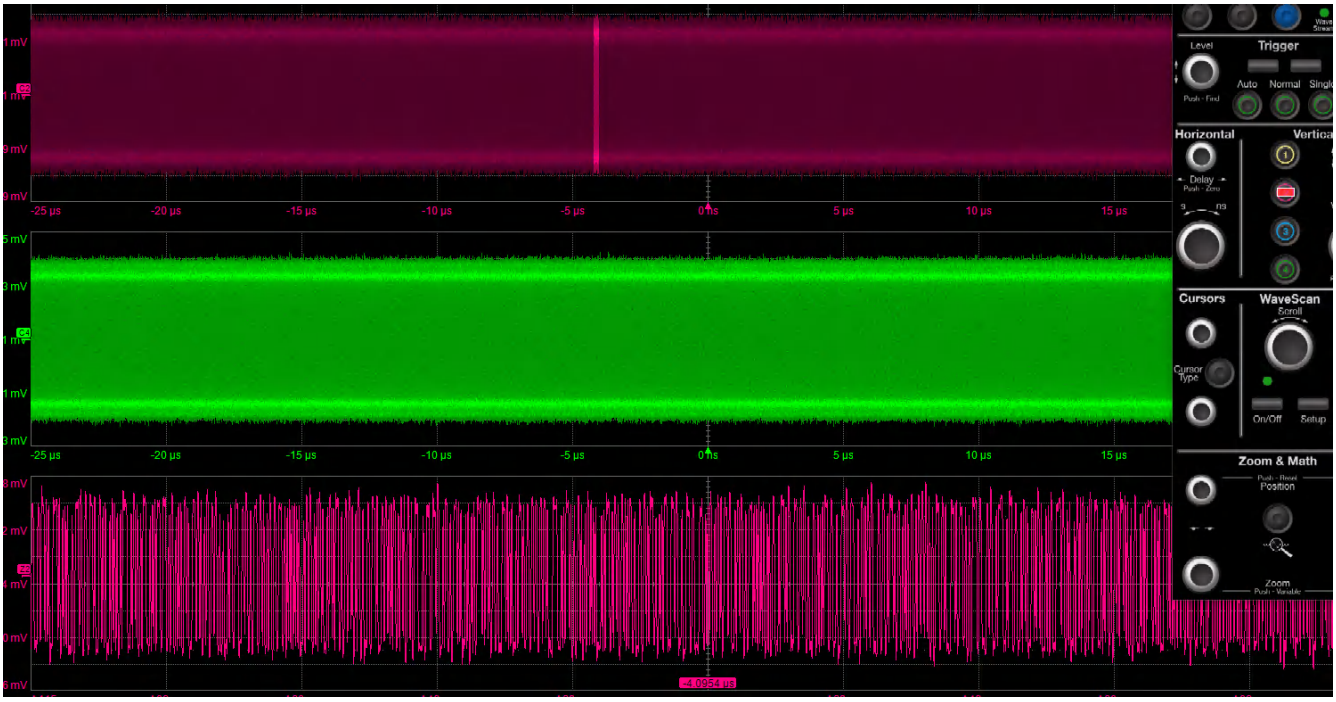

Figure 3-5. CP0 Compliance Pattern Observed on Oscilloscope

3.7 Compliance Pattern 1 (CP1)

Compliance Pattern 1 (CP1) is a clock sequence transmitted at the Nyquist frequency of the USB 3.0 link rate (5Gbps ÷ 2 = 2.5GHz).

The default TI SDK (11.02) device tree source (DTS) does not enable Spread Spectrum Clocking (SSC) on the SERDES PLL. Because CP1 testing requires SSC, the following modifications must be made to the k3-j784s4-j742s2-evm-common.dtsi file:

Go to <SDK_INSTALL_DIR>/board-support/ti-linux-kernel-<version>/arch/arm64/boot/dts/ti/ k3-j784s4-j742s2-evm-common.dtsi

Add the code below to the &serdes_wiz0 node to enable SSC as shown in Figure 5:

ti,core-clk-sel = <1>; /* Select internal ref clock */

ti,ssc-enable; /* Enable SSC */

ti,ssc-type = <1>; /* 1 for Downspread */

ti,ssc-frequency-hz = <33000>;

ti,ssc-depth-per-mil = <5>; /* 0.5% depth */

Add the following property to the serdes0_usb_link: phy@0 node to configure SSC to internal mode:

cdns,ssc-mode = <2>; /* 2 for SSC enabled (internal) */

```
&serdes0 {
        status = "okay";

        serdes0_pcie1_link: phy@0 {
                reg = <0>;
                cdns,num-lanes = <2>;
                #phy-cells = <0>;
                cdns,phy-type = <PHY_TYPE_PCIE>;
                resets = <&serdes_wiz0 1>, <&serdes_wiz0 2>;
                bootph-all;
        };

        serdes0_usb_link: phy@3 {
                bootph-all;
                reg = <3>;
                cdns,num-lanes = <1>;
                #phy-cells = <0>;
                cdns,phy-type = <PHY_TYPE_USB3>;
                resets = <&serdes_wiz0 4>;
                cdns,ssc-mode = <2>;            /* 2 for SSC enabled (internal) */
        };
};

&serdes_wiz0 {
        bootph-all;
        ti,core-clk-sel = <1>;          /* Select internal ref clock */
        ti,ssc-enable;                  /* Enable SSC */
        ti,ssc-type = <1>;              /* 1 for Downspread */
        ti,ssc-frequency-hz = <33000>;
        ti,ssc-depth-per-mil = <5>;     /* 0.5% depth */
        status="okay";
};

&usb_serdes_mux {
        idle-states = <0>; /* USB0 to SERDES lane 3 */
};

&usbss0 {
        status = "okay";
        pinctrl-0 = <&main_usbss0_pins_default>;
        pinctrl-names = "default";
        ti,vbus-divider;
};

&usb0 {
        dr_mode = "host";
        maximum-speed = "super-speed";
        phys = <&serdes0_usb_link>;
        phy-names = "cdns3,usb3-phy";
};

&serdes_wiz4 {
        status = "okay";
};
```

Figure 3-6. Device Tree Source Modifications to Enable SSC and force USB in host mode

Compile the dts file to generate the .dtb file as below:

$cd /<sdk-install directory>/board-support/ti-linux-kernel-6.12.57+git-ti

$export CROSS_COMPILE=/< sdk-install directory >/linux-devkit/sysroots/x86_64-arago-linux/usr/bin/aarch64-oe-linux/aarch64-oe-linux-

$export ARCH=arm64

$make dtbs.

Copy the .dtb file into the sd card:

$cd /< sdk-install directory > /board-support/ti-linux-kernel-6.12.57+git-ti/arch/arm64/boot/dts/ti/

$sudo cp k3-j784s4-evm.dtb /media/<username>/root/boot/dtb/ti/k3-j784s4-evm.dtb

$sudo eject /media/<username>/root/

On the EVM Teraterm:

Step 1: Disconnect load board, then reboot:

$ reboot

Step 2: Force compliance mode:

$ devmem2 0x06010490 w 0x0a010340

Step 3: Write USB PHY CP1 register:

$ devmem2 0x0601812c w 0x18230c10

*$ devmem2 0x05060340 w 0x86000002 /*PLL0_CLK_SEL_M0_PLL0_CTRL_M0 */*

Step 4: Reconnect compliance load board. Observed signal: CP1 — repeating 1010 pattern producing a 2.5GHz waveform with SSC. The USB register write, selects the CP1 directly.

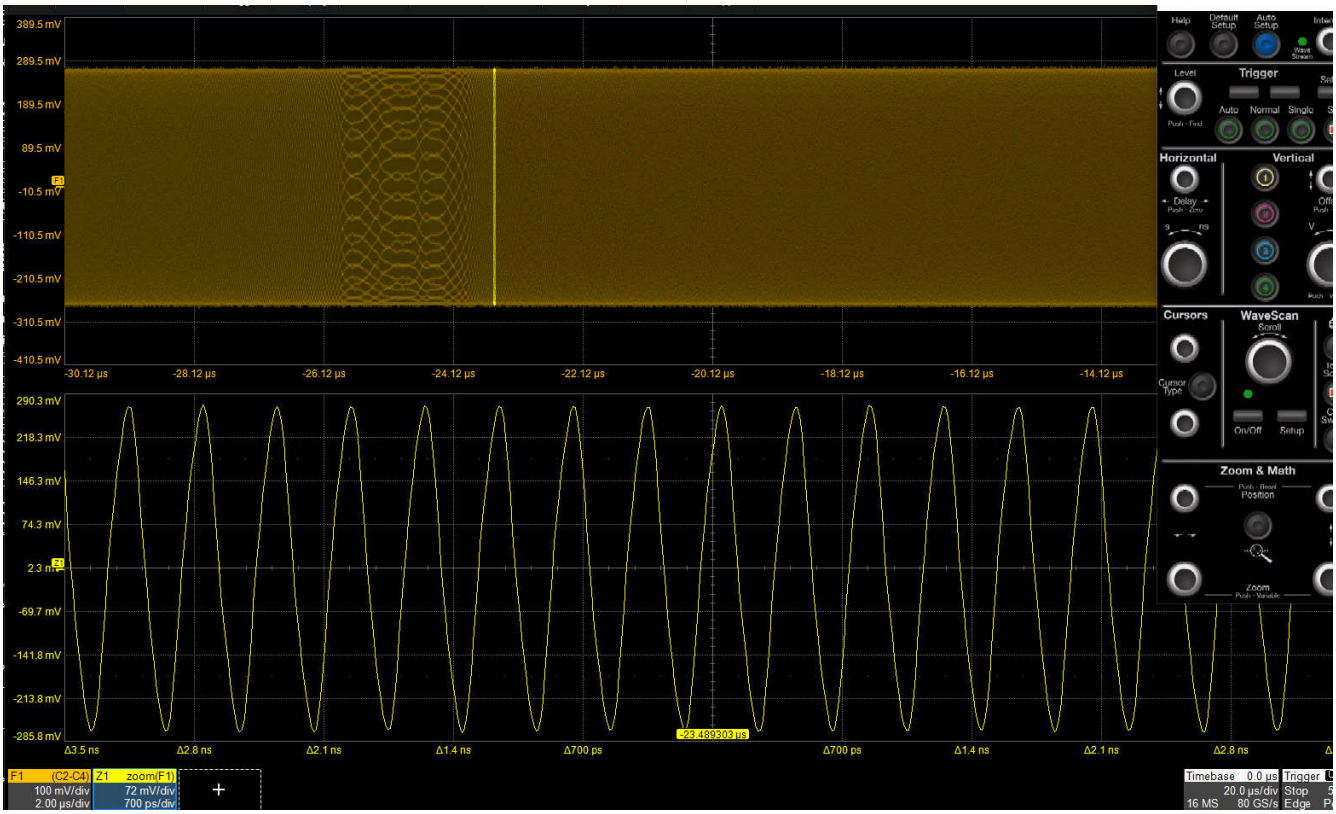

Figure 3-7. CP1 Compliance Pattern with SSC Enabled

3.8 LeCroy Scope Setup and Results

The LeCroy scope (SDA MCM-Zi-A) has QualiPHY framework that aids with automated compliance testing for high-speed serial bus standards like USB. From the QualiPHY dropdown menu(version 11.5 to match MAUI version 11.5), select USB3.1/3.2 TX and configure the Standard HostA, Gen1 as below. In the test selector tab, select the LFPS and the Gen1 tests, unselect the Gen2 tests. Once configuration is done, start the test and follow the prompts on the screen to enable each of the patterns requested. The channel calibration is highly recommended as prompted by the scope to deskew the SMA cables. Sigtest can be downloaded from the USB-IF website, if not already present on the scope.

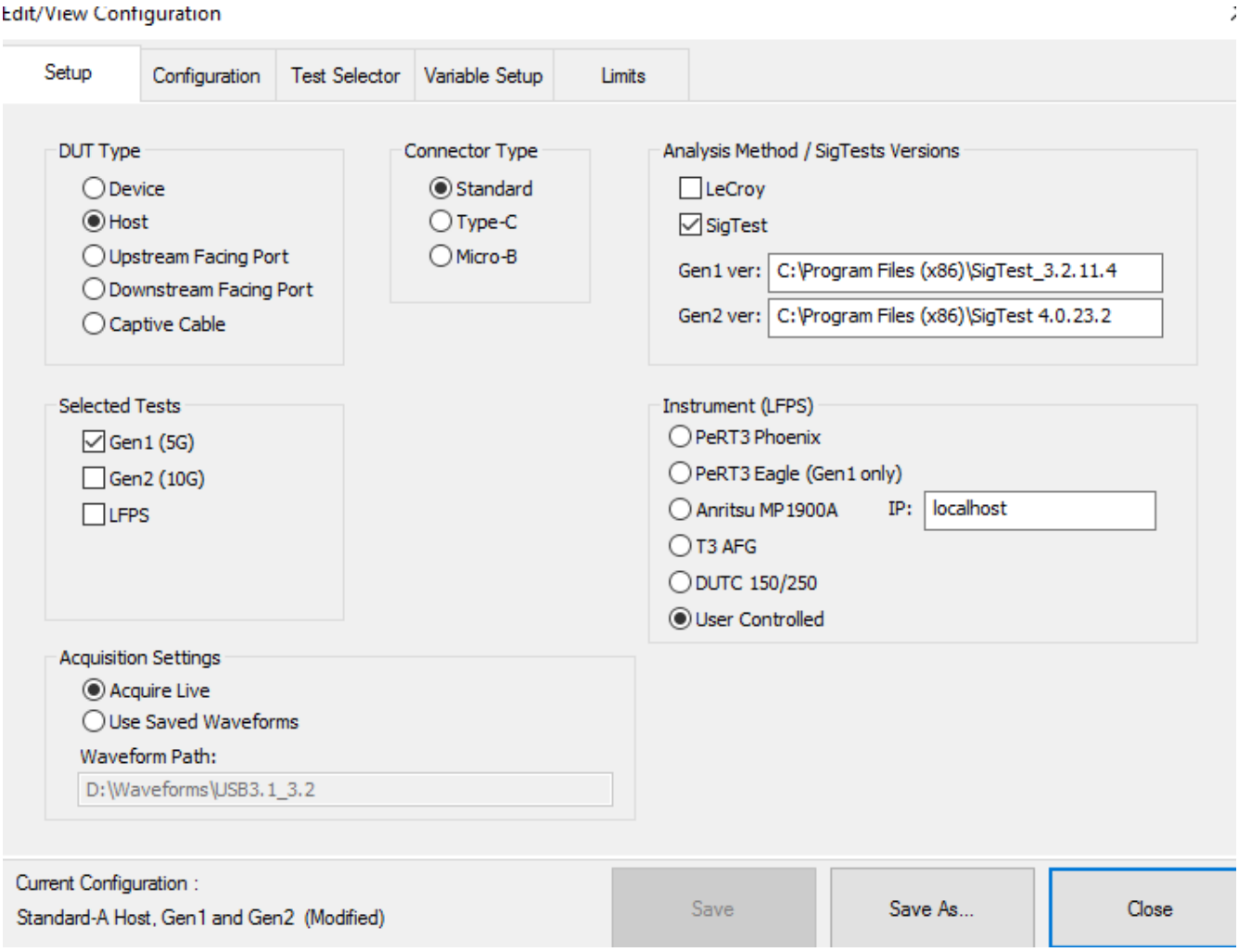

Figure 3-8. QualiPHY USB 3.1/3.2 TX Test Configuration

Once all patterns are analyzed and post-processed, the compliance software generates a PDF report as shown in Figure 3-9.

Summary Table

[Hide Table]

Pass	#	Test	Gen	Measurement	Chan	Analysis	Current Val	Test Criteria
✔	1	TD.1.1	N/A	LFPS Min Amplitude	Long	SigTest	884 mV	800 mV <= x <= 1.200 V
✔	1	TD.1.1	N/A	LFPS Min Amplitude	Long	SigTest	894 mV	800 mV <= x <= 1.200 V
✔	1	TD.1.1	N/A	LFPS Max CM AC	Long	SigTest	31.602 mV	x <= 100.000 mV
✔	1	TD.1.1	N/A	LFPS Min Period	Long	SigTest	60 ns	20 ns <= x <= 100 ns
✔	1	TD.1.1	N/A	LFPS Max Period	Long	SigTest	60 ns	20 ns <= x <= 100 ns
✔	1	TD.1.1	N/A	LFPS Min Burst Time	Long	SigTest	963 ns	600 ns <= x <= 1.400 us
✔	1	TD.1.1	N/A	LFPS Max Burst Time	Long	SigTest	1.084 us	600 ns <= x <= 1.400 us
✔	1	TD.1.1	N/A	LFPS Min Repeat Time	Long	SigTest	10.02 us	6.00 us <= x <= 14.00 us
✔	1	TD.1.1	N/A	LFPS Max Repeat Time	Long	SigTest	11.04 us	6.00 us <= x <= 14.00 us
✔	1	TD.1.1	N/A	LFPS Min Duty Cycle	Long	SigTest	49.9 %	40.0 % <= x <= 60.0 %
✔	1	TD.1.1	N/A	LFPS Max Duty Cycle	Long	SigTest	50.0 %	40.0 % <= x <= 60.0 %
✔	1	TD.1.1	N/A	LFPS Rise Time	Long	SigTest	244 ps	x <= 4.0 ns
✔	1	TD.1.1	N/A	LFPS Fall Time	Long	SigTest	234 ps	x <= 4.0 ns

Figure 3-9. Compliance Test Results: Pattern Overview

Summary Table

[Hide Table]

Pass	#	Test	Gen	Measurement	Chan	Analysis	Current Val	Test Criteria
✔	1	TD.1.6	Gen1	SSC Deviation Max (max)	Long	LeCroy	124.7 PPM	-300.0 PPM <= x <= 300.0 PPM or -2.3000 kPPM <= x <= -1.7000 kPPM
✔	1	TD.1.6	Gen1	SSC Deviation Max (min)	Long	LeCroy	74.4 PPM	-300.0 PPM <= x <= 300.0 PPM or -2.3000 kPPM <= x <= -1.7000 kPPM
✔	1	TD.1.6	Gen1	SSC Frequency Modulation Rate	Long	LeCroy	32.499 kHz	30.000 kHz <= x <= 33.000 kHz
✔	1	TD.1.6	Gen1	SSC Deviation Min (max)	Long	LeCroy	-4.8717 kPPM	-5.3000 kPPM <= x <= -3.7000 kPPM
✔	1	TD.1.6	Gen1	SSC Deviation Min (min)	Long	LeCroy	-4.9394 kPPM	-5.3000 kPPM <= x <= -3.7000 kPPM
✔	1	Legacy	Gen1	Phase Jitter Slew Rate Max	Long	LeCroy	2.561 ms/s	x = 0 us/s +/- 10.000 ms/s
✔	1	Legacy	Gen1	Phase Jitter Slew Rate Min	Long	LeCroy	-2.629 ms/s	x = 0 us/s +/- 10.000 ms/s
✔	1	TD.1.3	Gen1	Tj CP1	Long	SigTest	16.8544 ps	x <= 132.00 ps
ℹ	1	TD.1.3	Gen1	Rj (rms) CP1	Long	SigTest	0.9039 ps	Informational Only
✔	1	TD.1.3	Gen1	SigTest Pass / Fail Result (CP0, Jitter)	Long	SigTest	pass	match "Pass"
✔	1	TD.1.3	Gen1	Tj CP0	Long	SigTest	49.6665 ps	x <= 132.00 ps
ℹ	1	TD.1.3	Gen1	Rj (rms) CP0	Long	SigTest	0.9039 ps	Informational Only
✔	1	TD.1.3	Gen1	Dj DD CP0	Long	SigTest	36.9581 ps	x <= 86.00 ps
ℹ	1	TD.1.3	Gen1	Min Time Between Crossovers	Long	SigTest	184.337 ps	Informational Only
✔	1	TD.1.3	Gen1	Avg UI	Long	SigTest	200.4672 ps	199.9400 ps < x < 201.0656 ps
ℹ	1	TD.1.3	Gen1	Max PP Jitter	Long	SigTest	52.662 ps	Informational Only
✔	1	TD.1.3	Gen1	Non Transition Eye Violations	Long	SigTest	0 hits	x = 0 hits
✔	1	TD.1.3	Gen1	Transition Eye Violations	Long	SigTest	0 hits	x = 0 hits
✔	1	TD.1.3	Gen1	Total Eye Violations	Long	SigTest	0 hits	x = 0 hits
✔	1	TD.1.3	Gen1	SigTest Pass / Fail Result (CP0, Eye)	Long	SigTest	pass	match "Pass"
ℹ	1	TD.1.3	Gen1	Eye Height	Long	SigTest	223.1 mV	Informational Only
ℹ	1	TD.1.3	Gen1	Max Non Trans Voltage	Long	SigTest	224.1 mV	Informational Only
ℹ	1	TD.1.3	Gen1	Min Non Trans Voltage	Long	SigTest	-224.3 mV	Informational Only
ℹ	1	TD.1.3	Gen1	Max Trans Voltage	Long	SigTest	233.3 mV	Informational Only
ℹ	1	TD.1.3	Gen1	Min Trans Voltage	Long	SigTest	-233.7 mV	Informational Only
ℹ	1	TD.1.3	Gen1	Min Non Trans Upper Margin	Long	SigTest	62.2 mV	Informational Only
ℹ	1	TD.1.3	Gen1	Max Non Trans Lower Margin	Long	SigTest	-60.9 mV	Informational Only
ℹ	1	TD.1.3	Gen1	Max Trans Upper Margin	Long	SigTest	79.9 mV	Informational Only
ℹ	1	TD.1.3	Gen1	Max Trans Lower Margin	Long	SigTest	-78.3 mV	Informational Only
ℹ	1	TD.1.3	Gen1	Min Eye Width	Long	SigTest	150.333 ps	Informational Only
✔	1	TD.1.3	Gen1	Tj CP1	Short	SigTest	16.9204 ps	x <= 132.00 ps
ℹ	1	TD.1.3	Gen1	Rj (rms) CP1	Short	SigTest	0.9132 ps	Informational Only
✔	1	TD.1.3	Gen1	SigTest Pass / Fail Result (CP0)	Short	SigTest	pass	match "Pass"
✔	1	TD.1.3	Gen1	Tj CP0	Short	SigTest	31.0602 ps	x <= 132.00 ps
ℹ	1	TD.1.3	Gen1	Rj (rms) CP0	Short	SigTest	0.9132 ps	Informational Only
✔	1	TD.1.3	Gen1	Dj DD CP0	Short	SigTest	18.2200 ps	x <= 86.00 ps
ℹ	1	TD.1.3	Gen1	Min Time Between Crossovers (after channel)	Short	SigTest	188.220 ps	Informational Only

Figure 3-10. Compliance Test Results: Eye Diagram Analysis

Pass#	Test	Gen	Measurement	Chan	Analysis	Current Val	Test Criteria
✔ 1	TD.1.3	Gen1	Avg UI	Short	SigTest	200.4672 ps	199.9400 ps < x < 201.0656 ps
1	TD.1.3	Gen1	Max PP Jitter	Short	SigTest	32.882 ps	Informational Only
✔ 1	TD.1.3	Gen1	Non Transition Eye Violations	Short	SigTest	0 hits	x = 0 hits
✔ 1	TD.1.3	Gen1	Transition Eye Violations	Short	SigTest	0 hits	x = 0 hits
✔ 1	TD.1.3	Gen1	Total Eye Violations	Short	SigTest	0 hits	x = 0 hits
1	TD.1.3	Gen1	Eye Height SigTest	Short	SigTest	396.2 mV	Informational Only
1	TD.1.3	Gen1	Max Non Trans Voltage SigTest	Short	SigTest	327.6 mV	Informational Only
1	TD.1.3	Gen1	Min Non Trans Voltage SigTest	Short	SigTest	-326.5 mV	Informational Only
1	TD.1.3	Gen1	Max Trans Voltage SigTest	Short	SigTest	348.2 mV	Informational Only
1	TD.1.3	Gen1	Min Trans Voltage SigTest	Short	SigTest	-346.4 mV	Informational Only
1	TD.1.3	Gen1	Min Non Trans Upper Margin	Short	SigTest	159.3 mV	Informational Only
1	TD.1.3	Gen1	Max Non Trans Lower Margin	Short	SigTest	-164.3 mV	Informational Only
1	TD.1.3	Gen1	Max Trans Upper Margin	Short	SigTest	149.8 mV	Informational Only
1	TD.1.3	Gen1	Max Trans Lower Margin	Short	SigTest	-146.4 mV	Informational Only
1	TD.1.3	Gen1	Min Eye Width SigTest	Short	SigTest	168.940 ps	Informational Only

Figure 3-11. Compliance Test Report Summary

3.9 Troubleshooting

Table 3-4. Troubleshooting Guide

Symptom	Likely Cause	Resolution
No pattern after devmem2 write	Port not in Rx.Detect; device still connected	Disconnect device; read PORTSC and confirm PLS[8:5] = 0101 before writing
No Pattern after fixture connected	SoC is not in host mode; USB-C cable orientation needs flipped	Check the DIP switches are set to host DFP mode. Try both sides of the USB-C cable;
PORTSC unchanged after write	LWS (bit 16) not set; wrong address used	Check the write value is 0xa010340 (LWS=1); verify SoC MMIO base address
Only CP0 visible; no CP1	USB CP1 register not written	Write 0x18230c10 to USB PHY register after PORTSC write; reboot first if needed
Failing USB SSC compliance	SSC is not enabled	Enable SERDES PLL SSC through the device tree source .dts file modification
Failing LFPS specs	Cable mismatch	Run the De-skew operation on the cables; Match the compliance test suite QPHY version with MAUI s/w version

3.10 Compliance Procedure: DRA821 / TDA4AL/VL/VE / J721S2

The DRA821/ TDA4AL/VL/VE / J721S2 SoC uses the same USB MMIO base address (0x06010000) as the TDA4xH/TDA4xP SoC. All register addresses and compliance procedure steps are identical to those described in Section 3.

4 Summary

A comprehensive guide to enable USB3.1 Gen1 Superspeed Host TX electrical compliance testing on the Jacinto Processors SoCs has been provided. Using the latest available SDK, the method described can be applied to custom boards, or on the EVM. This approach provides a highly cost-effective TX validation path by eliminating the need for external Bit Error Rate Testers (BERT) or specialized hardware pattern generators. Using the native Linux commands and device tree source modifications, the engineers can force the SoC to output the compliance patterns and activate the SSC (spread spectrum clocking) required for quick USB compliance checkout.

5 References

1. USB, usb.org, webpage.
2. USB-IF, *USB-IF Compliance Test Specification (CTS) for USB 3.1*, webpage.
3. Intel, *xHCI Interface Specification for USB, Revision 1.2*, webpage.
4. Texas Instruments, *TDA4xH Jacinto™ SoC Technical Reference Manual*, technical reference manual.

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