Application Note

Inrush Current Control for the BQ2579X Input MUX FETs

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ABSTRACT

This application note examines the relationship between FET turn on speed and inrush current, presenting design equations and measurement results that can be used to predict and reduce startup current spikes.

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1 Introduction

In-rush current is the peak current that an electric device draws at power up, before the current settles to a normal operating current. The device's integrated circuits (ICs) have varying amounts of capacitance at the IC's pins. A discharged capacitor is essentially a short circuit when a fast-rising voltage is first applied as shown by the equation below:

$$i_c = C \times dv/dt \quad (1)$$

where i_C is the current through the capacitor

C is the capacitance

dv is the change is voltage across the capacitor

dt is the time for the change in voltage

If the capacitor's voltage slew rate (dv/dt) is high, the capacitor sinks a high current, commonly called inrush current, until the capacitor fully charges. The current spike places significant stress on the power supply/battery that is applying this voltage and/or any other components or PCB traces through which the current flows. This stress potentially results in thermal damage or electrical shutdown if the components are not rated for the surge. For example, if a USB-C source has negotiated only 500mA output current but the inrush current is 1.5A, the USB-C source detects over current and drops to a lower power state. Designers often consider adding soft start circuitry to slowly charge high capacitive nodes to reduce the current spike. If the component preceding a capacitor is a MOSFET, a common method to reduce this current spike is to slow the FET's turn on time or slew rate and limit the downstream capacitor charging current.

2 Detailed Description

2.1 Inrush Current

To allow for switching between two different input sources, the BQ2579x charger family has two FET output drivers (ACDRVx pins) for driving common source NFETs.

Figure 2-1 shows a non-soft started power up waveform using a BQ25798EVM with C_{VBUS}+C_{PMID}=40uF.

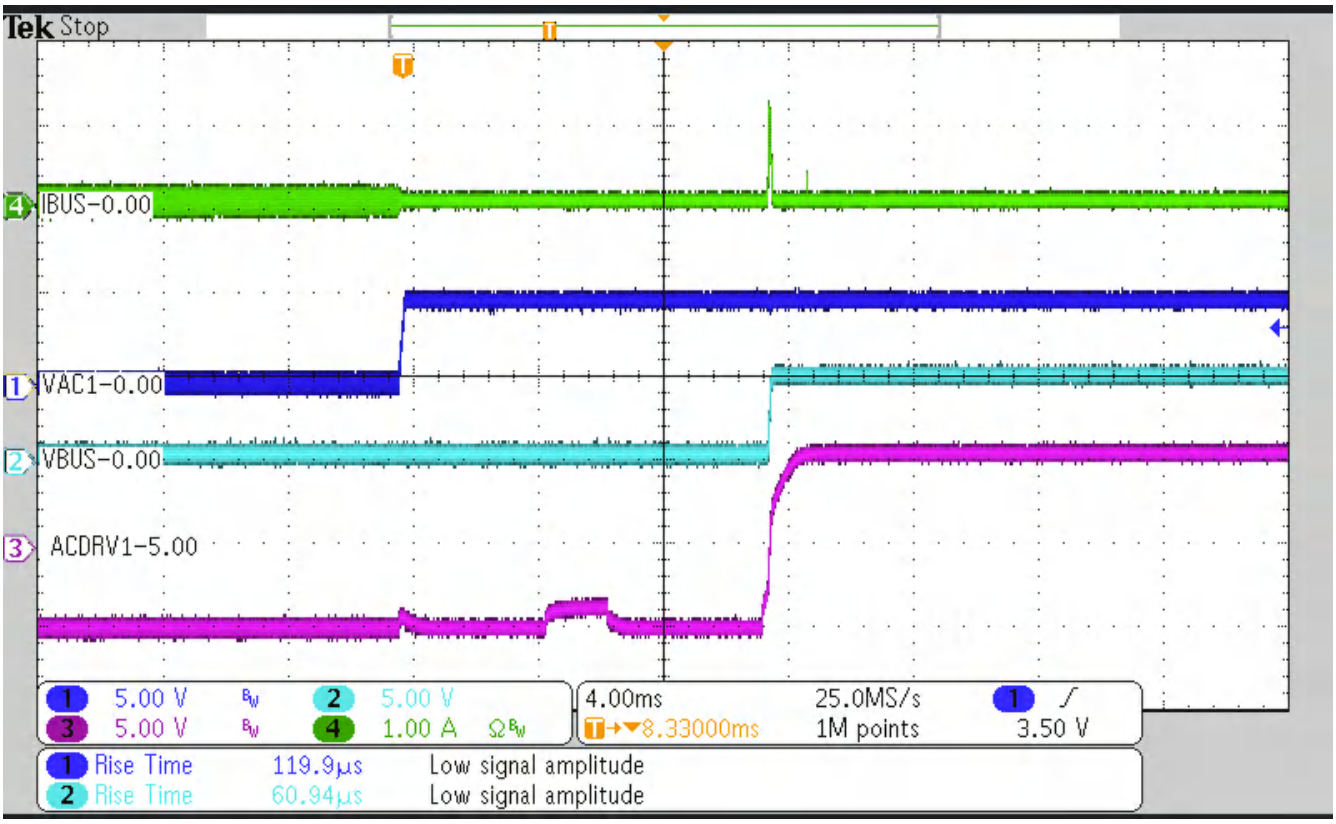

Figure 2-1. Inrush current spike when ACFET turns on

When a voltage is first applied the VAC1 sense input (CH1-dark blue), an internal input FET detection algorithm runs for approximately 15ms to determine if the FET pair is attached. After this 15ms delay expires, the charger's ACDRVx pin (CH3-pink with 5V offset) turns on the input FET to charge the capacitance at the VBUS (CH2-light blue) and through an internal FET's body diode to the PMID pins. The first large inrush current pulse (CH4-green) occurs as the input source charges the VBUS and PMID capacitors. The second, smaller current pulse, is due to the internal NFET between VBUS and PMID turning on to raise the PMID voltage to VBUS from a diode drop below.

2.2 Adding FET soft start with a capacitor

Slowing down the ACDRVx drive voltage by increasing the series resistance from ACDRVx to FET gate and/or adding a gate to source capacitor is one way to slow down a FET's turn on (i.e. soft start the FET). However, the BQ2579x family's 15ms FET detection algorithm can false trip without careful sizing of that resistor and capacitor. Another way to implement FET inrush control is to add more capacitance between the FET's gate and drain, C_{DG-ADD}. Figure 2-2 shows the schematic for one of the BQ25798 input MUX FET pairs and the additional gate to drain capacitance C_{DG-ADD}.

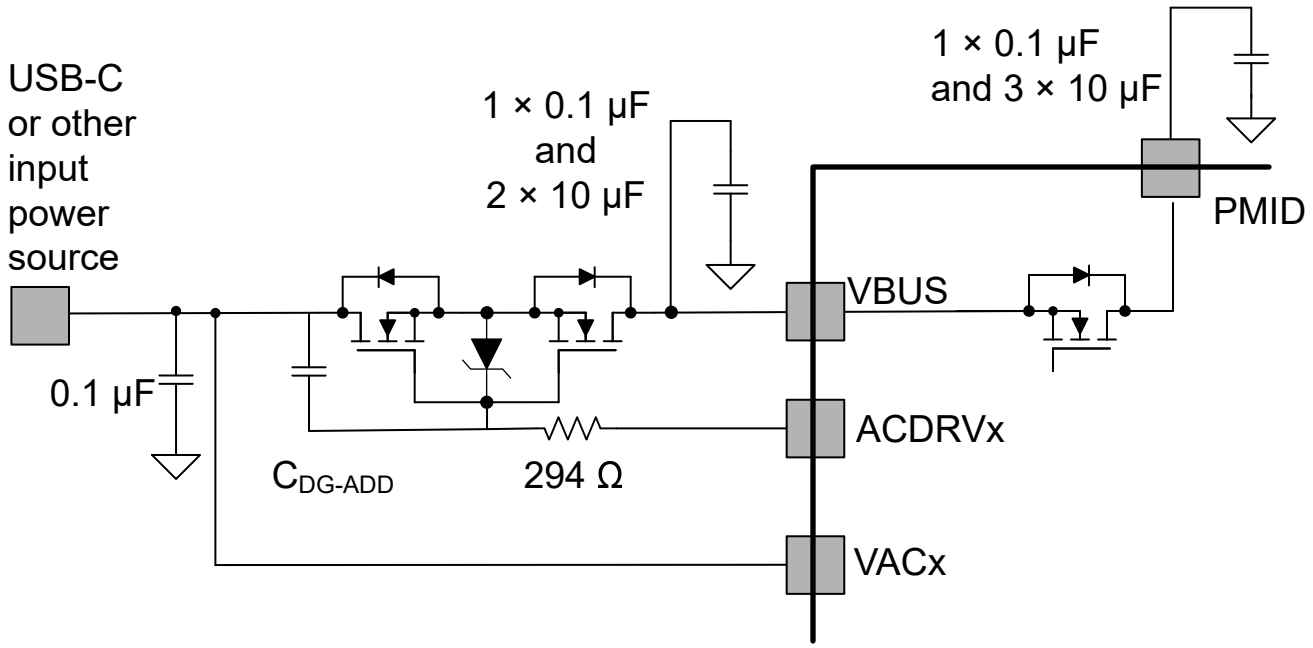

Figure 2-2. BQ2579X MUX input schematic

If C_{DG-ADD} is at least an order of magnitude higher than the FET's inherent C_{DG}, the inherent C_{DG} (typically in the 1000pF range) can be ignored and FET turn on time is proportional to C_{GD-ADD} charge time. The ACDRVx pin's output is essentially a current source with typical output current of I_{ACDRV} = 45uA. So, equation 1 above can be used to predict C_{DG-ADD} charge time and VBUS turn on time.

The additional C_{DG-ADD} must be sized

1. Large enough to meet the desired inrush current spec, $I_{IN-RUSH} = (C_{VBUS+}C_{PMID}) * dV_{BUS}/dt$. Because the ACDRVx current source charges the C_{DG-ADD}, the FET turn on time and therefore VBUS rise time can be estimated by the equation $I_{ACDRV} = C_{DG-ADD(MIN)} * V_{BUS}/dt$.
2. Small enough to prevent a current pulse at initial power up, i.e. $C_{DG-MAX} = I_{CDG-VACi} / (d_{VACi}/dt)$ where d_{VACi}/dt is the VACx voltage rise time (CH1 initial rise in Figure 2),
3. Small enough that the FET turns fully on (i.e. has lowest R_{DSON} from ACDRVx=VBUS+5V)
   a. Before the charger's converter starts, 200ms after VBUS is higher than UVLO (3.6V typical)
   b. So that the FET does not heat up enough to exceed the safe operating area (SOA).

Note that when a fully-on wall adapter is hot-plugged, VACx sees a voltage with very high slew rate (d_{VACi}/dt) that causes an initial current pulse due to C_{DG-ADD}. In this case, C_{DG-MAX} computes too small to minimize the MUX FET inrush current. Adding a small series resistor (10W) reduces $I_{CDG-VACi}$. If the additional series resistance does not reduce $I_{CDG-VACi}$ enough, the only choice for soft starting the MUX input FET is to use additional C_{DG} capacitance and higher series resistor between ACDRVx and NFET gate.

Luckily, most recent battery-powered end equipment use USB-C port for power. USB-C ports regulate the output voltage slew rate to 30mV/us. In general, C_{DG-ADD} works for end equipment powered by USB-C ports and other slow turn on power sources.

2.3 Test results for 5V USB-C input power source

Using requirement 1 we find $C_{DG-ADD(MIN)}$.

- For $I_{IN-RUSH}$ less than 100mA, the max dV_{BUS}/dt must be less than 100mA / 40uF = 2500V/s.
- For a 5V supply, VBUS rise time must be slower than dt= 5V/(2500V/s) = 2ms so $C_{DG-ADD(MIN)}$ = 45uA / (5V/2ms) = 0.018uF.

Using requirement 2, we find $C_{DG-ADD(MAX)}$.

- A USB-C 5V source with 30mV/us slew rate, has d_{VACi}/dt = 167us. For desired $I_{CDG-VACi}$ = 1mA, $C_{DG-ADD(MAX)}$ = 1mA / (5V/167us) = 0.033uF.

Requirement 3 is irrelevant in this example.

Figure 3 shows the same BQ25798EVM being powered in Figure 1 but with C_{DG-ADD} = 0.03uF.

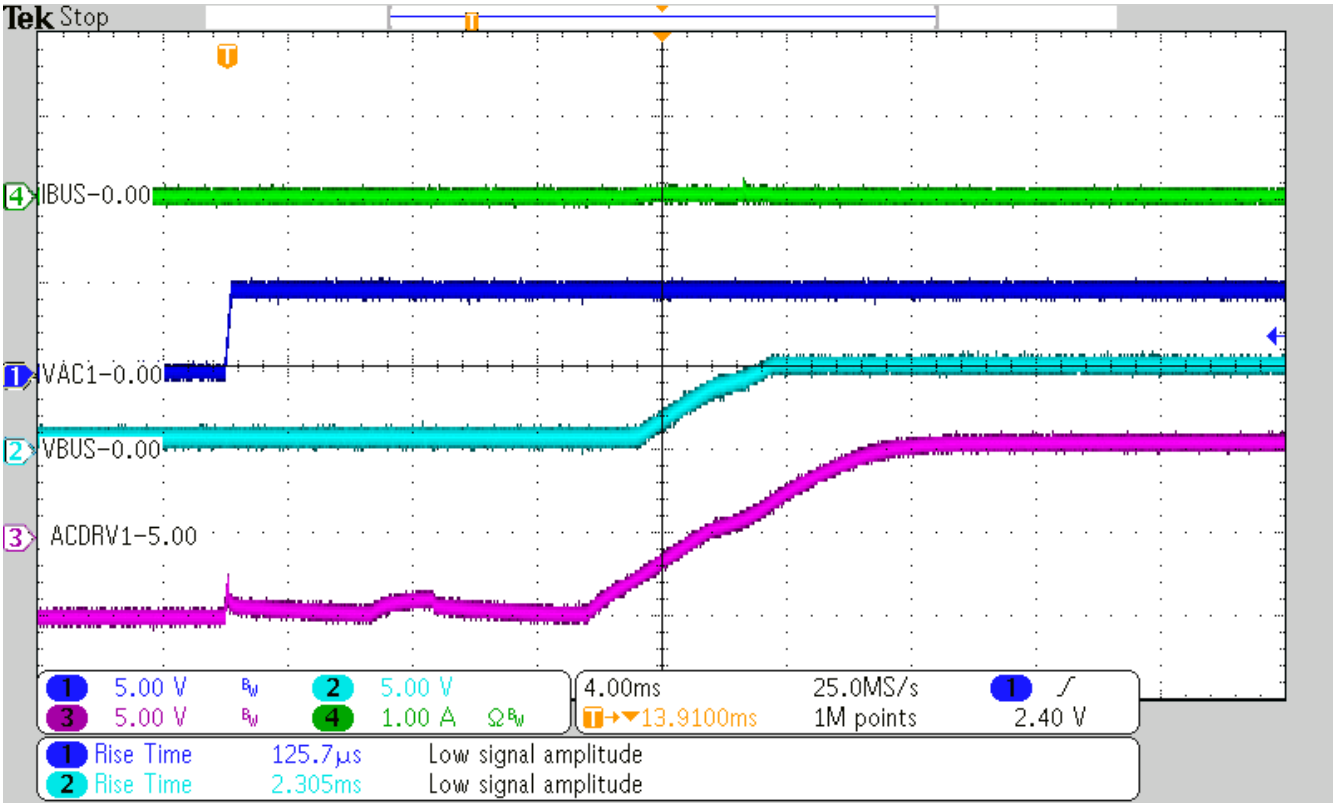

Figure 2-3. BQ25798EVM powerup with C_{DG-ADD} = 0.03uF

The VAC1 input voltage rise time is a simulated USB-C port of 5V/(30mV/us) = 167us. Note that ACDRV1 and VBUS rise slowly and there are no current spikes in Figure 3 compared to Figure .

Table 2-1 compares theoretical calculations with experimental measurements for different input voltages and C_{DG-ADD} values.

Table 2-1. Measured vs Calculated VBUS Rise Time for Different C_{DG-ADD} Values

VBUS (V)	C_{DG-ADD} (nF)	Measured VBUS Rise Time (ms)	Calculated VBUS rise time from dt = C_{DG-ADD}*VBUS/I_{ACDRV}(ms)
9	47	8	9.4
9	7.5	1.2	1.5
9	30	4.2	6
5	47	6.2	5.2
5	7.5	1	0.8
5	30	4	3.3

The correlation between the measured rise time and the computed rise time confirms that the relationship between C_{DG-ADD} charge time and VBUS rise time is valid. Slowing the ACDRVx drive voltage reduces the VBUS pin voltage slew rate dv/dt, which decreases the peak inrush current at FET turn on.

3 Summary

Proper selection of additional C_{DG} provides an effective method for controlling inrush current through the BQ2579x input MUX FETs, while maintaining reliable device operation.

4 References

1. BQ25798 I2 C Controlled, 1 to 4-Cell, 5A Buck-Boost Battery Charger with Dual-Input Selector , MPPT for Solar Panels and Fast Backup Mode datasheet (Rev. C)
2. BQ25790 I2 C Controlled, 1 to 4-Cell, 5A Buck-Boost Battery Charger with Dual-Input Selector , MPPT for Solar Panels and Fast Backup Mode datasheet (Rev. C)
3. BQ25672 I2 C Controlled, 1 to 4-Cell, 5A Buck-Boost Battery Charger with Dual-Input Selector , MPPT for Solar Panels and Fast Backup Mode datasheet (Rev. C)

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