Application Note

Full-Bridge LLC with UCC25661x

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Abstract

This application note describes the implementation of a full-bridge LLC resonant converter based on the UCC25661x LLC controller. Since the controller is primarily intended for half-bridge applications, additional circuitry is employed to generate the required gate-drive signals and necessary features for full-bridge operation.

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1 Introduction

LLC resonant converters are widely used in high-efficiency isolated DC-DC power conversion applications due to their ability to achieve soft-switching operation over a wide load range. By operating the primary switches under zero voltage switching (ZVS) conditions and minimizing switching losses, LLC converters offer high efficiency, reduced electromagnetic interference (EMI), and high-power density. These characteristics make them attractive for server power supplies, telecom power systems, consumer electronics, and industrial power conversion systems.

The half-bridge LLC converter is commonly employed in medium-power applications because of its simple implementation and reduced component count. However, as the power level increases, a Full-Bridge LLC topology becomes attractive due to its ability to apply the full input bus voltage across the resonant tank, thereby reducing current stress and conduction losses while enabling higher power capability.

The UCC25661x family is a highly integrated LLC resonant controller primarily intended for half-bridge LLC converters. In applications requiring higher output power, it can be desirable to retain the features of the UCC25661x while implementing a Full-Bridge power stage. This can be achieved using an additional interface and gate-drive circuitry.

This application note presents the implementation of a full-bridge LLC resonant converter using the UCC25661x controller. The document discusses the operating principle, gate-drive generation method, protection implementation, design considerations, and experimental validation of the proposed design.

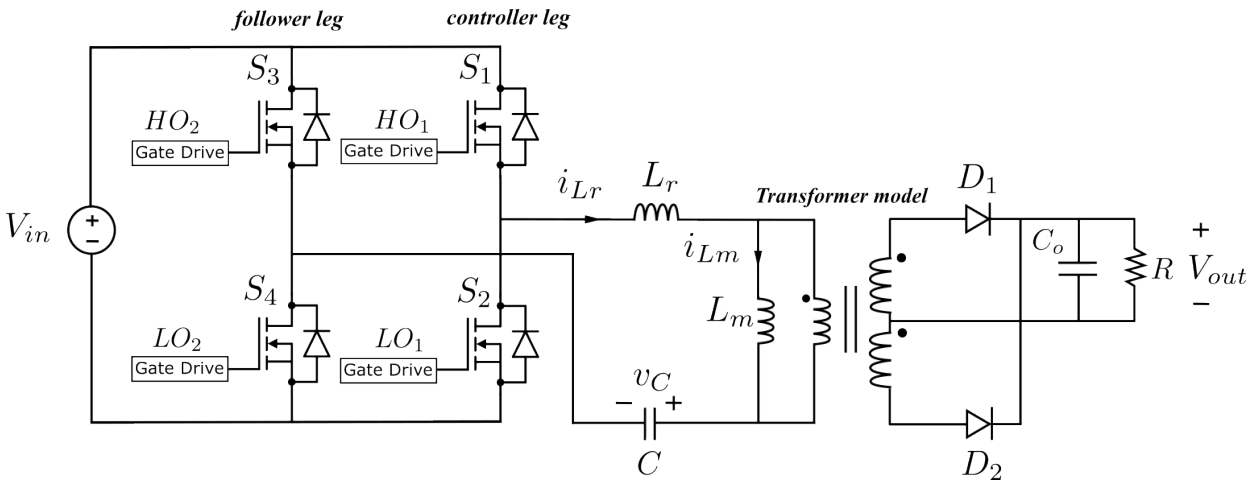

Figure 1-1. Full-Bridge LLC Resonant Converter

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2 Full-Bridge LLC Operating Principle

This section provides an overview of the Full-Bridge LLC converter operation. Figure 2-1 shows the complementary switching sequence of the two bridge legs. During steady state operation, diagonally opposite switches are turned on simultaneously, applying alternating polarity across the resonant tank. This results in tank square-wave excitation which generates a near-sinusoidal resonant current that flows through the resonant network and transformer. The AC current is hence scaled, rectified and filtered to produce a regulated DC output voltage.

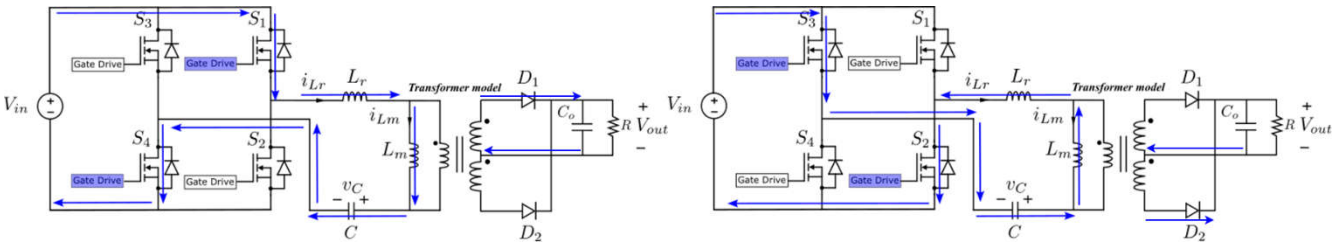

Figure 2-1. Switching States and Resonant Tank Operation of the Full-Bridge LLC Converter

From the resonant tank perspective, the full-bridge LLC converter operates similarly to the half-bridge LLC converter. The primary difference is that the full input bus voltage is applied across the resonant tank, whereas only half of the bus voltage excites the resonant tank in a half-bridge implementation. Consequently, the gain relationship and transformer turns-ratio selection differ by a factor of two, while the resonant tank analysis and frequency-control methodology remain unchanged. The simplified resonant tank gain expression obtained using the first harmonic approximation (FHA) is given by Equation 1 (where Bridge is 0.5 for half bridge and 1 for full bridge topology):

$$\text{Normalized Gain} = \text{Bridge Gain} \times \text{N(Transformer turns ratio)} \times \text{Impedance Ratio Gain} \quad (1)$$

Figure 2-3 shows the resonant tank gain characteristics for different load conditions. All gain curves intersect at the resonant frequency, while the peak of each curve defines the boundary between capacitive and inductive operation. To verify zero voltage switching (ZVS) and minimize switching losses, LLC converters are designed to operate in the inductive region. The corresponding resonant tank waveforms are shown in Figure 2-2 (for fs < fr).

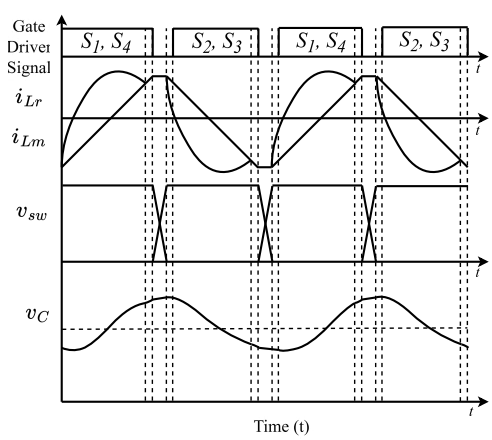

Figure 2-2. FB-LLC Steady State Waveforms

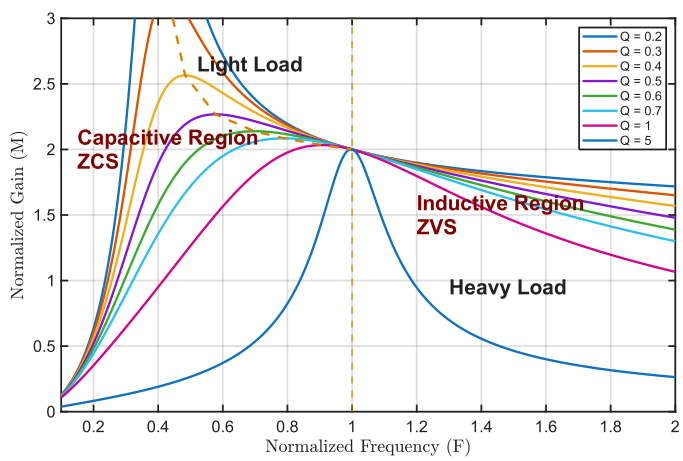

Figure 2-3. Gain Characteristics of the FB-LLC

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3 Implementation With UCC25661x

3.1 Gate Drive Architecture

The UCC25661x generates the *HO* and *LO* signals required for half-bridge LLC operation. In a full-bridge LLC converter, the high-side switches of each leg are referenced to different floating switch nodes rather than to ground (PGND). Therefore, the controller outputs cannot be directly applied to the follower leg. Isolated gate drivers are employed to verify that each gate signal is properly referenced to its corresponding source terminal, enabling correct gate-drive voltage. Similar gate drivers can be used on the controller leg as well to verify delay matching across both the legs. Here, HO1 and LO1 denote the controller leg gate drive signals, and HO2 and LO2 denote the follower leg gate drive signals. HS and HS1 denote the switching node voltage of the controller and follower leg respectively.

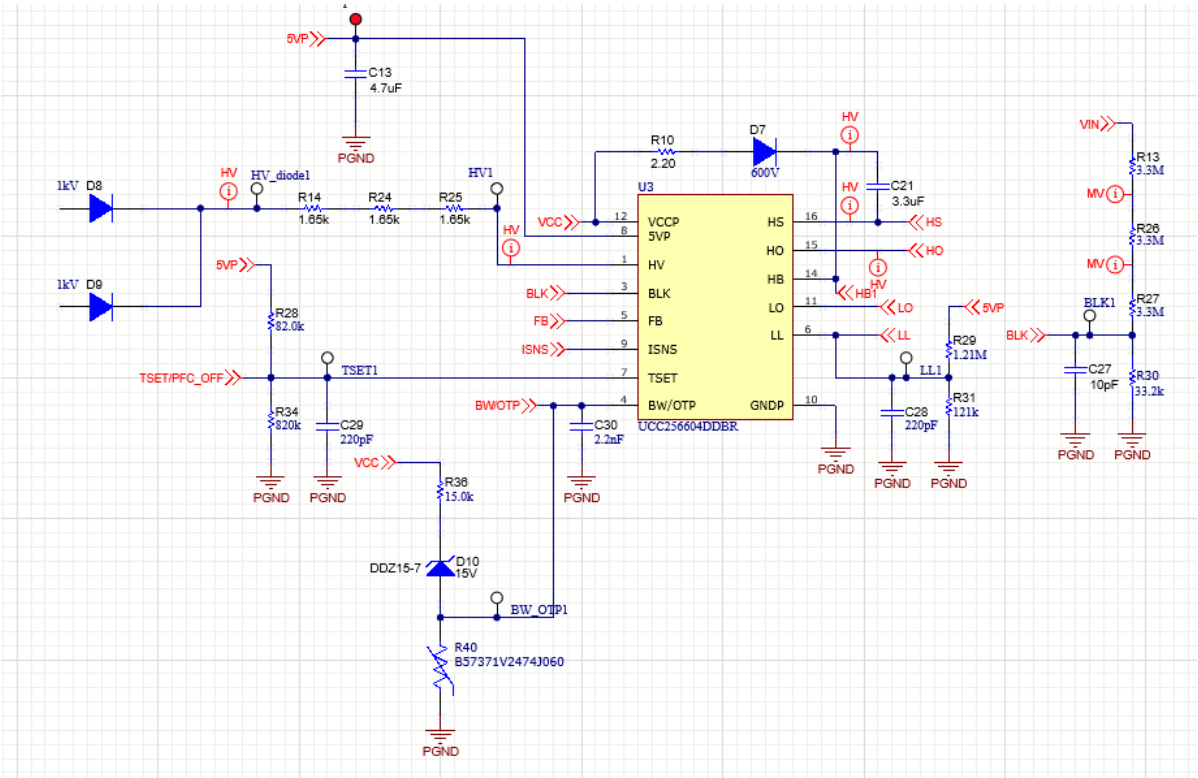

Figure 3-1. UCC25661x Implementation in Half-Bridge LLC

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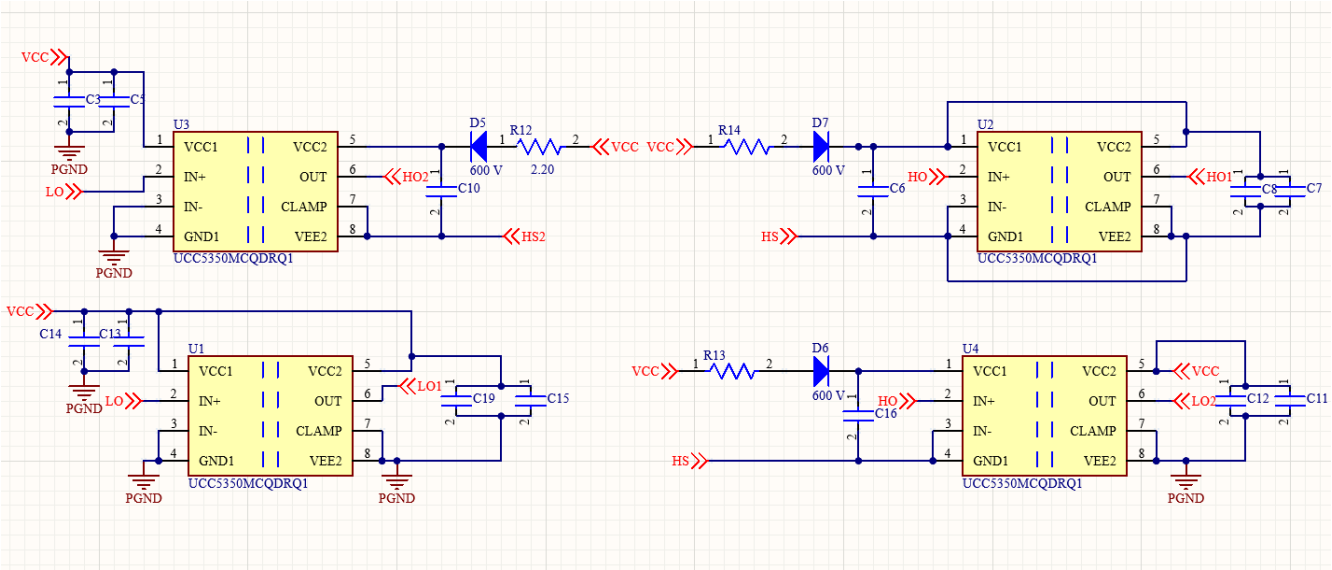

Figure 3-2. Full-Bridge LLC Isolated Gate Driver Implementation

The controller outputs HO and LO are routed through four isolated gate drivers to generate the gate-drive signals HO1, LO1, HO2, and LO2 required for the full-bridge LLC converter. The high-side gate drivers employ bootstrap circuits to provide the floating gate-drive supply referenced to the respective switching nodes (HS and HS1).

3.2 ISNS Circuit Modification

The UCC25661x Half-Bridge LLC EVM uses a split resonant capacitor arrangement and a differentiator-based circuit to sense the resonant tank current at the ISNS pin. In the Full-Bridge LLC implementation, the split capacitor arrangement is no longer required, and both ends of the resonant tank are connected to actively switching bridge nodes. Consequently, the resonant capacitor and tank network no longer possess a fixed reference node (PGND), making the original differentiator-based sensing method unsuitable. Therefore, the differentiator circuit is replaced with a current transformer (CT)-based sensing.

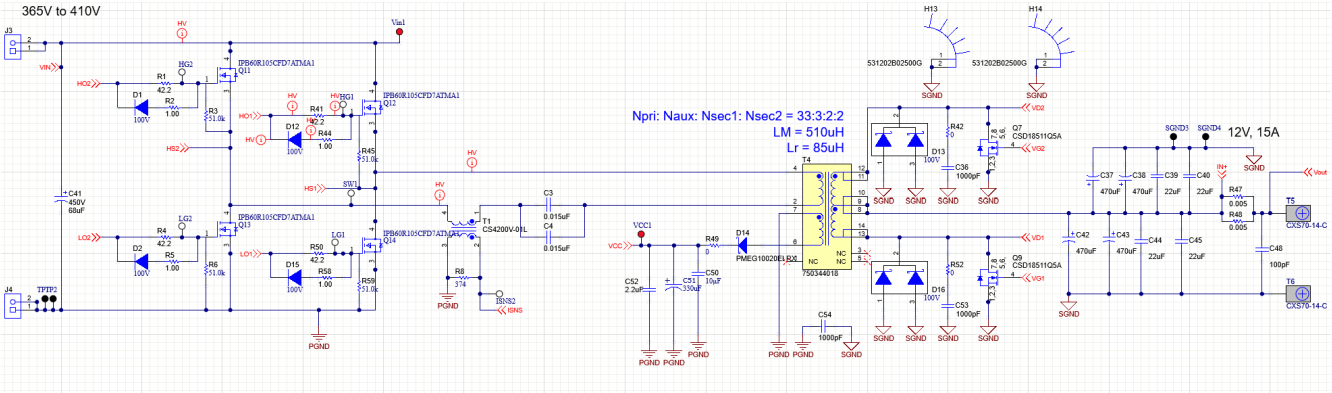

Figure 3-3. FB LLC Power Stage Schematic

The ISNS pin also sets the over current protection level (OCP1). The threshold value of OCP1 is either 3.5V or 4V depending on the TSET pin resistors and the variant being used. For this design, UCC256611 is being used and the OCP1 threshold value (OCP1_Threshold) is 3.5V. If the peak resonant current at full load is known (I_PEAK), then for a CT with turns ratio N (Pri : Sec) the burden resistance (RT) can be chosen as:

$$RT < OCP1_Threshold \times N / I_PEAK \quad (2)$$

The peak resonant current at OCP1 level (I_PEAK_OCP1) is then calculated using:

$$I_PEAK_OCP1 = OCP1_Threshold \times N / RT \quad (3)$$

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Note

The selected CT must be chosen to provide adequate current rating and volt-sec capability over the intended operating range.

3.3 Auxiliary Logic Implementation

During start-up, the controller applies an initial 200µs LO1 pulse to charge the bootstrap capacitor for the high-side switch. However, if isolated power supply modules are used for bootstrap charging, the converter immediately enters normal full-bridge operation, HO2 turns on simultaneously with LO1. As a result, the resonant tank is subjected to a voltage of V_{IN} + V_{CR} which is applied across the resonant or leakage inductor resulting in a large tank current that may exceed the safe operating limits of the power switches. To avoid this condition, an auxiliary logic circuit forces LO2 to turn on together with LO1 during the start-up interval. This effectively connects both ends of the resonant tank to the negative DC Bus, allowing the resonant capacitor to discharge under safe current limits before normal full-bridge operation is enabled.

The HO and LO outputs of the controller are first translated to 5V logic levels, denoted as LO2_5V and LO_5V, to verify compatibility with the digital logic circuitry. During the LLC startup sequence, the TSET signal transitions low before the controller generates the 200µs LO1 startup pulse. The same sequence is repeated during fault-retry operation, where TSET again transitions low following the 1s idle interval. This falling edge is detected using a one-shot circuit to generate a short SET pulse for the SR latch. Similarly, the falling edge of LO_5V is detected using a second one-shot circuit to generate a short RESET pulse. These SET and RESET pulses control the SR latch, whose output Q determines the converter operating mode.

When the latch is set (Q = 1), the logic forces Logic level LO2 high and HO2 low, thereby establishing the predefined start-up switching state. The latch retains this state until a RESET pulse is generated by the falling edge of LO_5V. Upon receiving the RESET pulse, the latch is cleared (Q = 0), removing the forcing action from the logic outputs. Thereafter, LO2 and HO2 follow the translated controller signals, enabling normal Full-Bridge LLC operation.

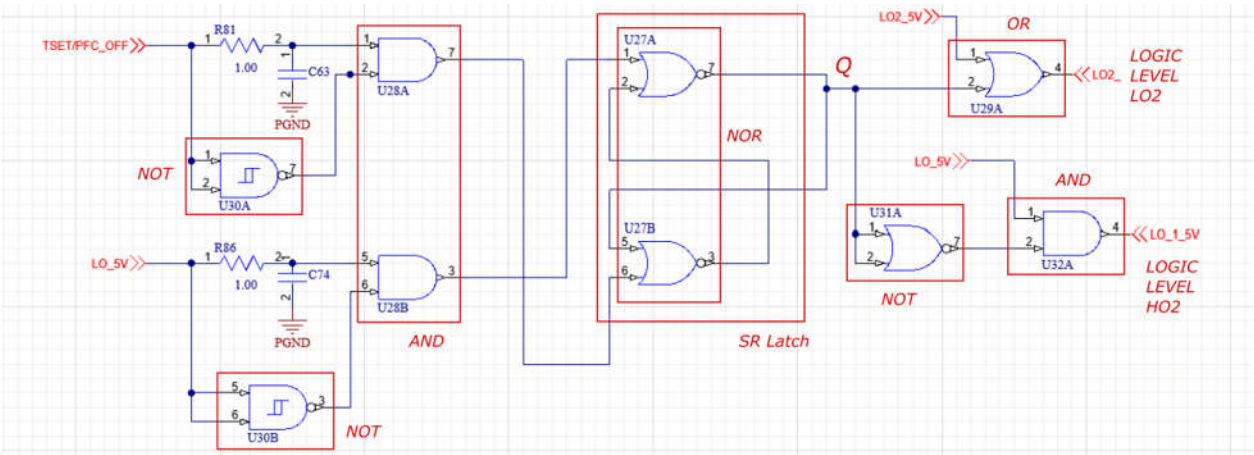

Figure 3-4. Auxiliary Logic Implementation Schematic

3.4 Logic Level Signal Translation

1. To implement the auxiliary logic circuit, the HO and LO signals from the controller need to be translated into logic level 5V (LO2_5V and LO_5V) respectively.

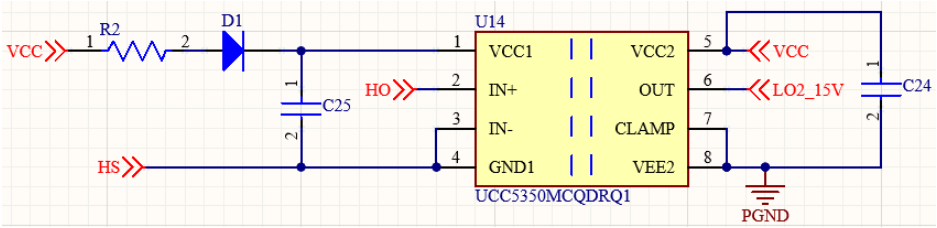

Figure 3-5. Logic-Level Translation of the HO Controller Output - 1

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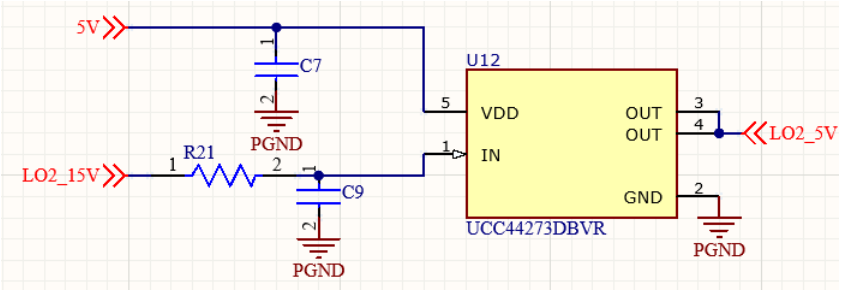

Figure 3-6. Logic-Level Translation of the HO Controller Output - 2

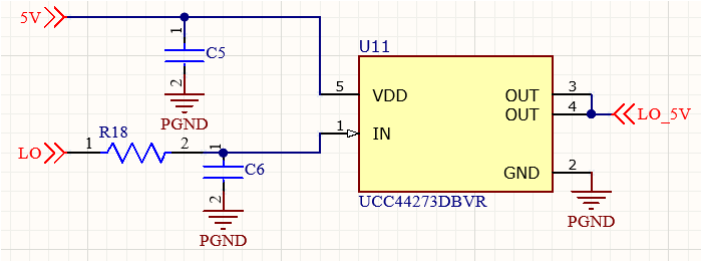

Figure 3-7. Logic-Level Translation of the LO Controller Output

An alternative implementation with reduced component count is shown in Figure 3-7. The floating HO signal is translated using the ISO1211 isolated digital input receiver, while the LO signal is translated using a resistor divider to generate logic-compatible 5V signals for the auxiliary logic circuit.

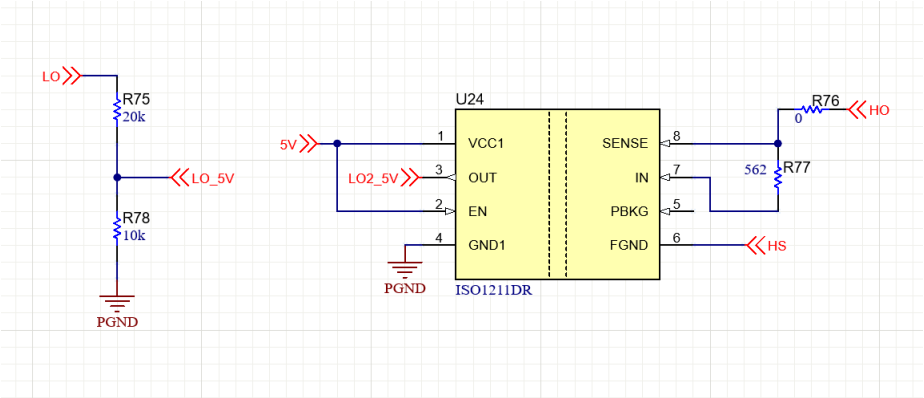

Figure 3-8. Alternative Logic-Level Translation of the HO and LO Controller Outputs

The logic-level outputs HO2 (LO_1_5V) and LO2 (LO2_5V) generated by the auxiliary logic circuit can be interfaced to the power stage using the four isolated gate-driver implementation shown in Figure 3-8. Alternatively, the same functionality can be realized using half-bridge gate drivers, as shown in Figure 3-9.

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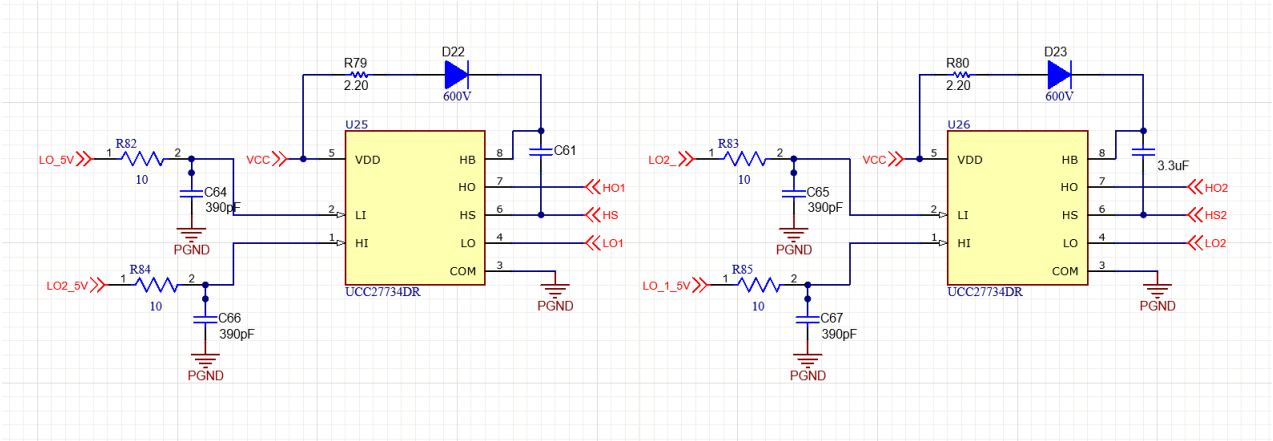

Figure 3-9. Alternative Full Bridge LLC Gate Driver implementation using Half-Bridge Gate Drivers

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4 Hardware Results

The experimental results for full-bridge LLC in normal resonant mode operation, burst mode operation, start up, load transient and bulk brown out are as shown below.

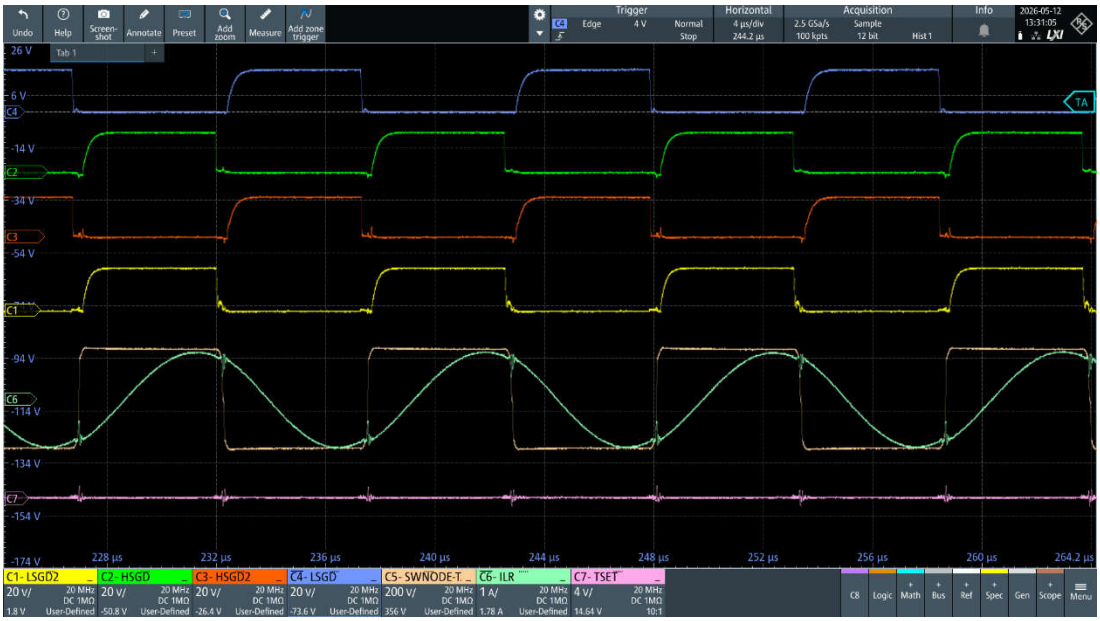

Figure 4-1. Vin = 185V , Vout = 12V , Iout = 7A, Normal Resonant Mode Operation, C1 = LO2 Gate Drive, C2 = HO1 Gate Drive, C3 = HO2 Gate Drive, C4 = LO1 Gate Drive C5 = Tank Voltage, C6 = Tank Current, C7 = TSET Pin Voltage

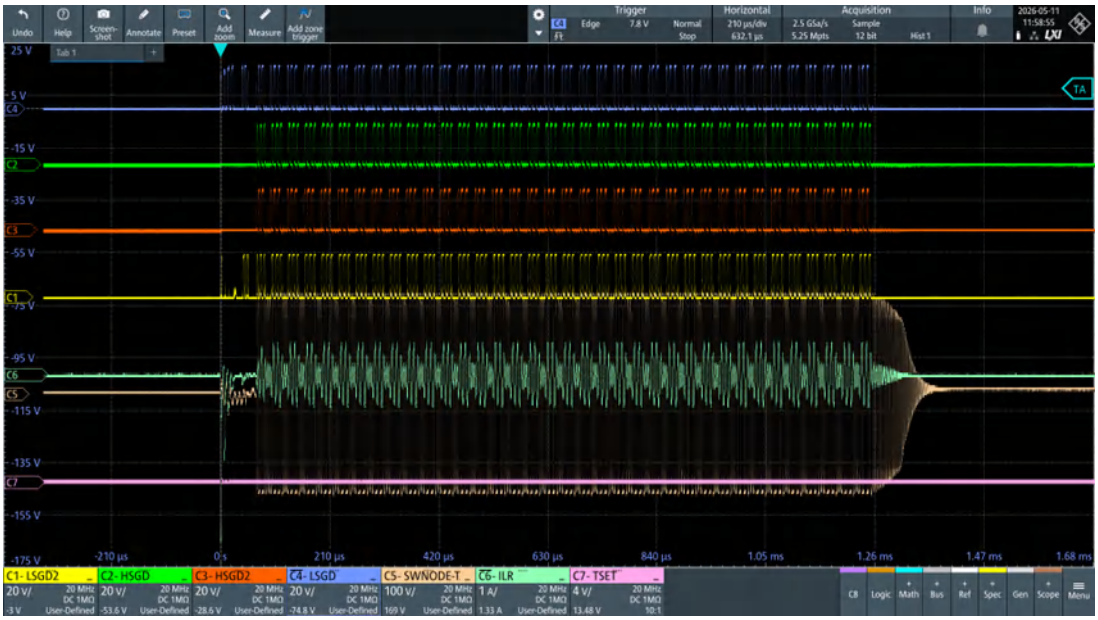

Figure 4-2. Vin = 185V , Vout = 12V , No Load, Burst Mode Operation, C1 = LO2 Gate Drive, C2 = HO1 Gate Drive, C3 = HO2 Gate Drive, C4 = LO1 Gate Drive C5 = Tank Voltage, C6 = Tank Current, C7 = TSET Pin Voltage

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Figure 4-3. Auxiliary Logic in Start-Up – HO2 and LO2 on for 200us Pulse, C1 = LO2 Gate Drive, C2 = HO1 Gate Drive, C3 = HO2 Gate Drive, C4 = LO1 Gate Drive, C5 = Tank Voltage, C6 = Tank Current, C7 = TSET Pin Voltage

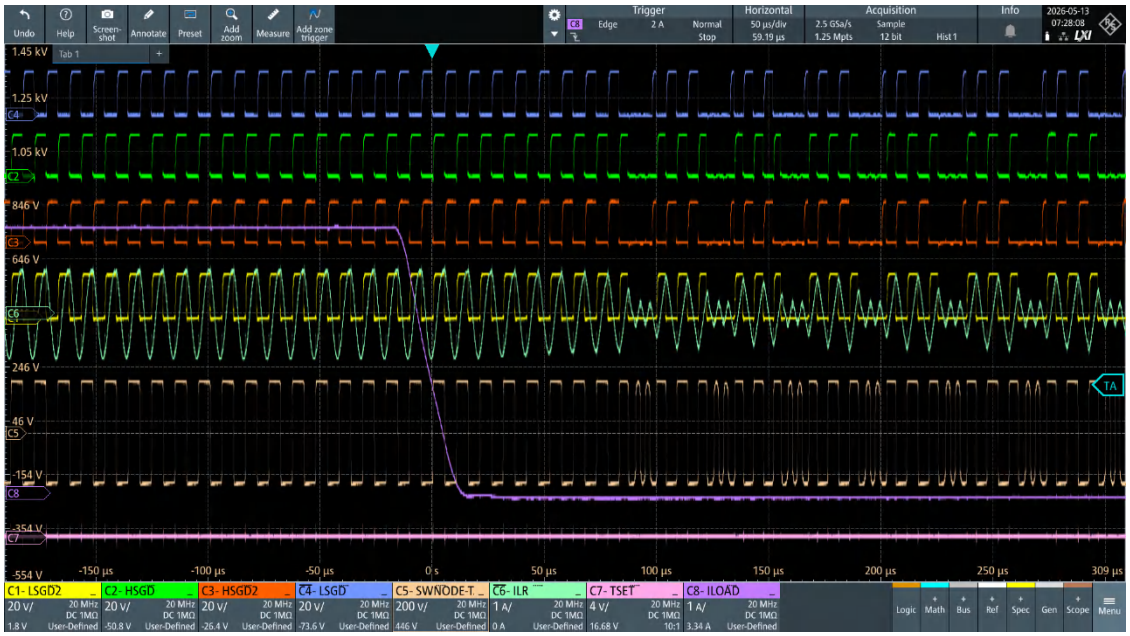

Figure 4-4. Vin = 185V, Vout = 12V, Iout = 5A to 0.01A Load Transient (0.2A/us) C1 = LO2 Gate Drive, C2 = HO1 Gate Drive, C3 = HO2 Gate Drive, C4 = LO1 Gate Drive C5 = Tank Voltage, C6 = Tank Current, C7 = TSET Pin Voltage, C8 = Load Current

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Figure 4-5. Vin = 185V, Vout = 12V, Iout = 0.01A to 5A Load Transient (0.2A/us) C1 = LO2 Gate Drive, C2 = HO1 Gate Drive, C3 = HO2 Gate Drive, C4 = LO1 Gate Drive C5 = Tank Voltage, C6 = Tank Current, C7 = TSET Pin Voltage, C8 = Load Current

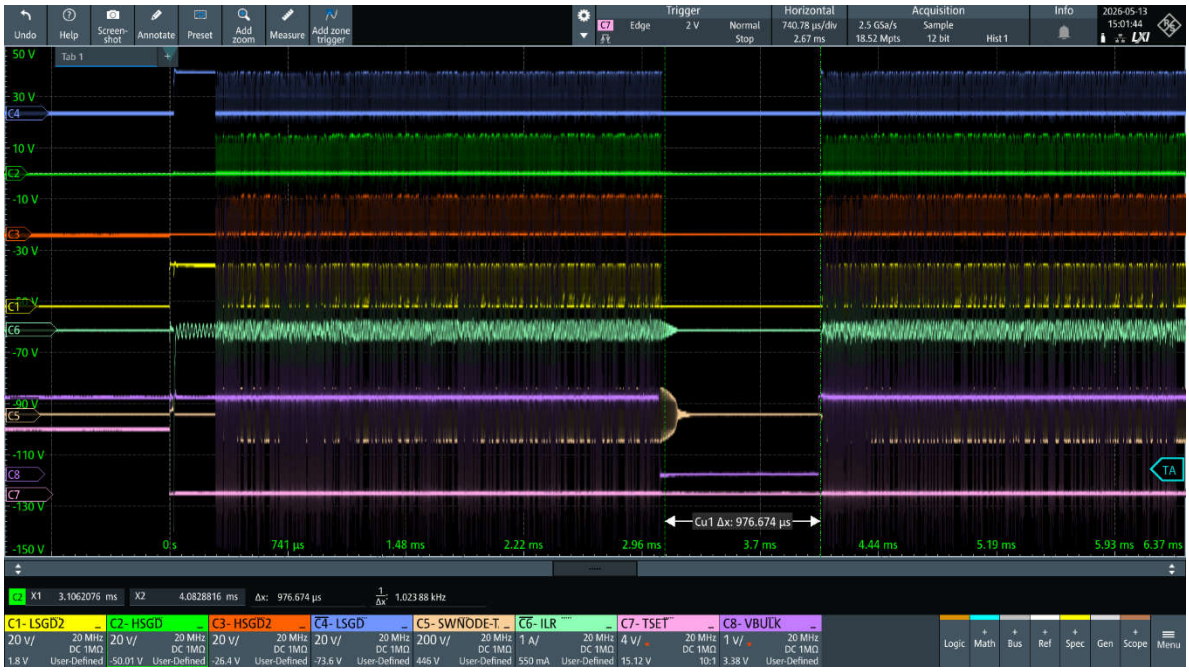

Figure 4-6. BLK Brownout Emulated at Vin = 100V, No Load Depicting Auxiliary Logic Operation C1 = LO2 Gate Drive, C2 = HO1 Gate Drive, C3 = HO2 Gate Drive, C4 = LO1 Gate Drive C5 = Tank Voltage, C6 = Tank Current, C7 = TSET Pin Voltage, C8 = Bulk Pin Voltage

All experimental results were obtained on the modified UCC25661x EVM in full-bridge configuration with the auxiliary startup circuit enabled (mentioned in Section 3). Because the full-bridge LLC applies twice the tank voltage of the half-bridge LLC, the prototype was tested at 185VDC using the original EVM magnetics.

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5 Summary

This application note demonstrates the implementation of a Full-Bridge LLC converter using the UCC25661x Half-Bridge LLC controller. The required hardware modifications, including isolated gate-drive implementation, auxiliary startup logic, and current transformer-based resonant current sensing, are presented. Experimental results on the modified UCC25661x EVM validate the proposed implementation and demonstrate reliable Full-Bridge LLC operation.

6 References

1. Texas Instruments, *UCC25661x Family 750kHz Wide VIN /VOUT Range LLC Controller Optimized for Light-Load Efficiency* , datasheet.
2. Texas Instruments, *UCC25661x Half Bridge LLC Evaluation Module*, EVM user's guide.

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7 Revision History

Changes from Revision * (September 2026) to Revision A (October 2026) **Page**

- Updated Figure 1-1 to use the term "controller leg" instead of "master leg" 2
- Created *Gate Drive Architecture* sub-section 4
- Moved content from *Implementation With UCC25661x* section to *Gate Drive Architecture* sub-section 4
- Replaced all instances of the term "master" with "controller" 4
- Created *ISNS Circuit Modification* sub-section 5
- Moved content from *Implementation With UCC25661x* section to *ISNS Circuit Modification* sub-section 5
- Created *Auxiliary Logic Implementation* sub-section 6
- Moved content from *Implementation With UCC25661x* section to *Auxiliary Logic Implementation* sub-section 6
- Added Figure 3-4 6
- Created *Logic Level Signal Translation* sub-section 6
- Moved content from *Implementation With UCC25661x* section to *Logic Level Signal Translation* sub-section. 6
- Deleted Figure 4-7 through Figure 7-12 for being duplicates of Figure 4-1 through Figure 4-6 9

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