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Abstract

This application note introduces the protection example for single-stage On-Board Chargers (OBCs). With single-stage OBCs gaining traction for higher power density, key design challenges including voltage stress, fast fault response, and AC voltage dips must be addressed. To overcome these limitations, Texas Instruments' TPLD family provides rich internal hardware resources, such as LUTs, delay blocks, internal oscillators, and analog comparators with flexible online programming capabilities. Finally, an example is presented to demonstrate how TPLD replaces bulky discrete logic components, optimizing BOM cost and simplifying system design while verifying robust protection.

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1 Introduction

An on-board charger (OBC) is a critical component in electric vehicles (EVs) and plug-in hybrid electric vehicles (PHEVs) that enables battery charging directly from standard AC power sources. With the development of EVs, the OBC architecture has evolved through several generations. The most recent trend is a single-stage OBC topology, which reduces component count, cost while delivering higher power density. The architecture merges PFC stage and DCDC stage into one high frequency conversion stage.

The matrix converter is currently the most prominent single-stage topology under discussion. [Figure 1-1](#) shows the block diagram of a matrix converter. Matrix converters eliminate bulky DC-link capacitors and AC input inductors required in traditional converters, so this can improve power density and reduce cost in space-constrained and cost-sensitive EV applications. Because there are no electrolytic capacitors, which are often failure points in traditional designs, matrix converters have improved reliability.

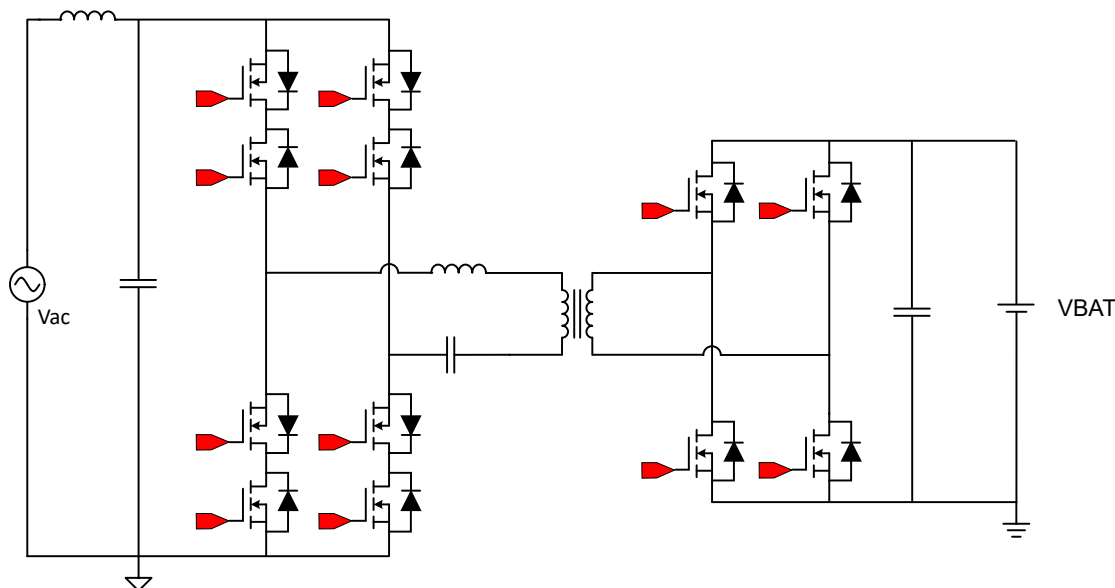


Figure 1-1. Block Diagram of the Matrix Converter

Despite these advantages, widespread adoption of matrix converters also faces challenges. Among them, overcurrent protection is one of the challenges of matrix converter, which is mainly due to the following several reasons.

2 Challenges in Overcurrent Protection

2.1 Voltage Stress Due to Blocking Freewheeling Path

When overcurrent faults happen, the basic idea is to turn off all power switches to protect them from thermal failure. This protection method is widely used in traditional two-stage OBC. As shown in [Figure 2-1](#) after all power switches are turned off, the current in the transformer then freewheels through the body diodes.

However, this control scheme cannot be used in matrix converter because of no freewheeling path. If all switches are completely turned off, the transformer current will charge the parasitic capacitance, resulting in a large voltage spike that can damage the devices, as shown in [Figure 2-2](#).

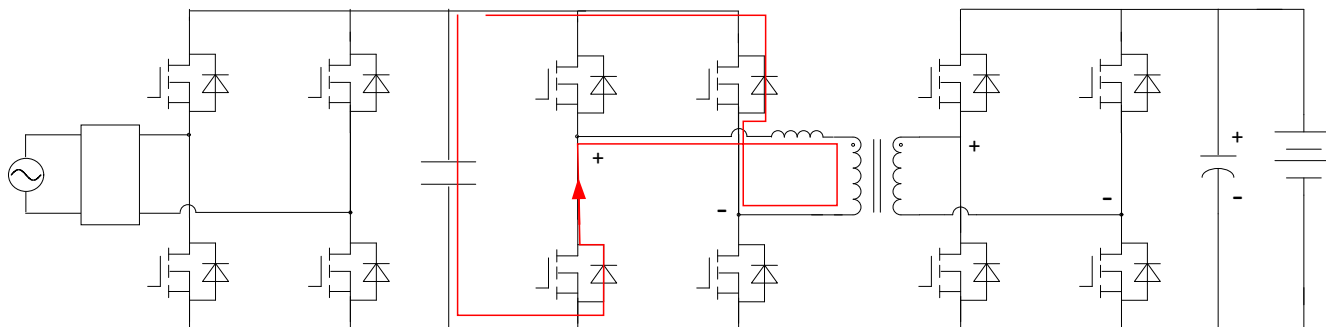


Figure 2-1. Current Path in Traditional OBC After all FETs Turn Off

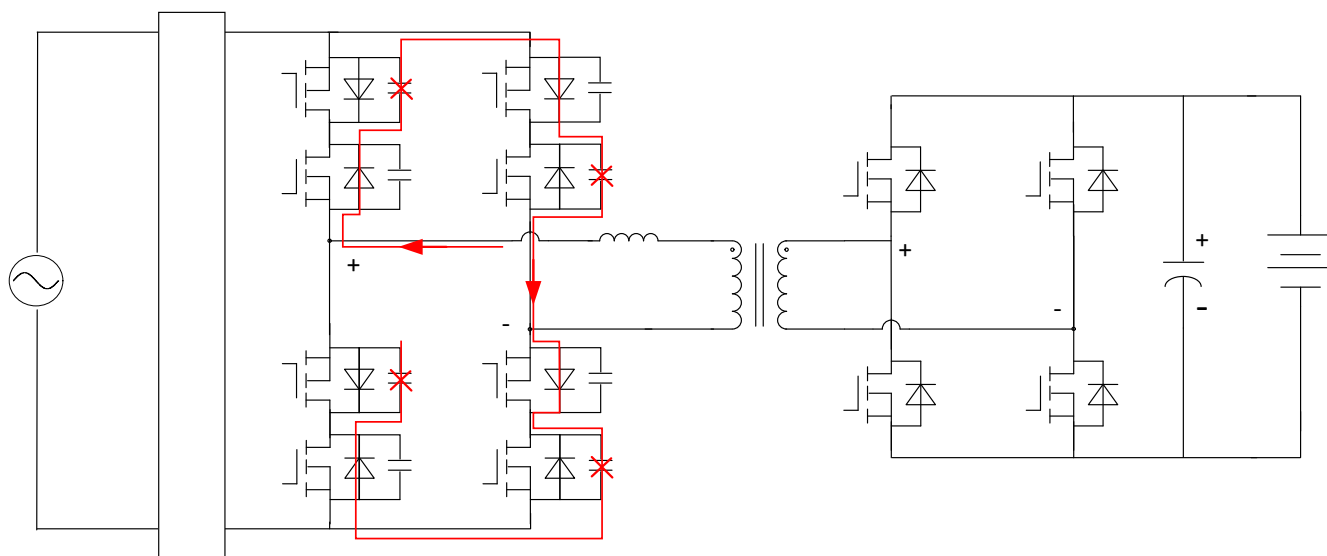


Figure 2-2. Current Path in Matrix Converter After All FETs Turn Off

Therefore, after OC flag is tripped, it is necessary to maintain a continuous current path for freewheeling. This means that the power switches need to be turned off with the sophisticated sequence.

2.2 Requirements on Fast Response Time

In traditional OBC, the PFC switching frequency is usually no more than 100kHz, while in matrix converter customers are pursuing 200kHz to 500kHz to increase power density. In higher switching frequency applications, SiC or GaN is used to replace Si based power switches. For traditional Si based power switches, the short-circuit withstand time can exceed 10 μ s. However, this value drops to less than 2 μ s in the case of SiC based power switches and further decreases to be less than 1 μ s in GaN based power switches.

The key factor affecting the short-circuit withstand time is the thermally induced catastrophic failure. The power switch is subjected to high voltage and high current during a short-circuit scenario, which leads to enormous instantaneous power dissipation and rapid temperature increase. Generally, GaN based power switches have higher current density, resulting in high power-density and rapid temperature increases during short-circuit conditions.

Therefore, for matrix converters, the OC response must be faster than traditional OBC because of the characteristics of power switches.

2.3 AC Grid Voltage Drop

OBC product testing requires that when the AC input voltage suddenly drops, the OBC will enter a fault-protection state and then recover after the abnormal input ends. During this event, the AC voltage can drop from 311V to -311V within several microseconds, and the reversed voltage can persist for up to $t_1 = 1$ ms, as shown in Figure 2-3.

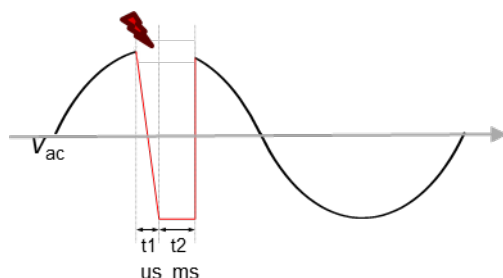


Figure 2-3. Sudden AC Voltage Drop Triggers OCP

When a sudden AC voltage drop occurs, the OBC must quickly trigger OCP. If the converter continues operating in original mode, it can cause AC-side short circuits. Figure 2-4 is the current path during normal operation, and Figure 2-5 is the current path when AC voltage drop occurs. When the AC voltage is reversed, the current goes through the body diode of the power switch and cause current spike. If the short-circuit current magnitude and duration (in microseconds) exceed the device limits, the power switches can be damaged.

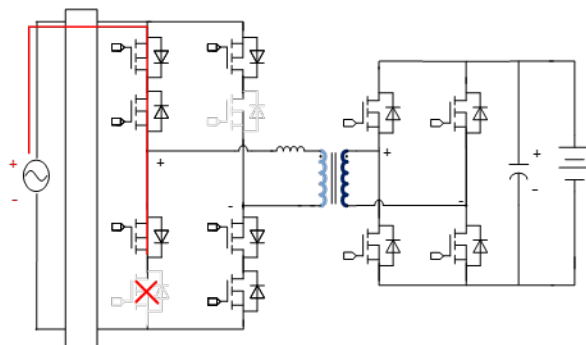


Figure 2-4. $V_{ac} > 0$ Operating Condition

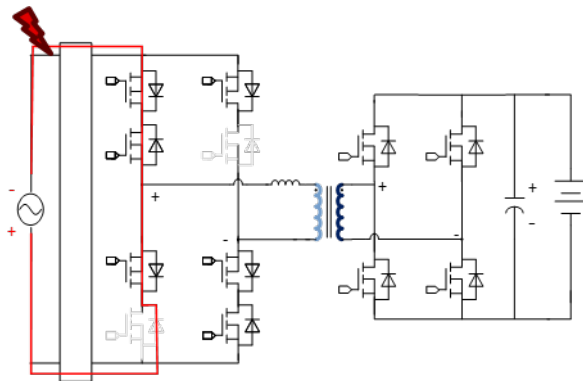


Figure 2-5. Current Path in AC Voltage Drop

Therefore, the AC grid voltage drop must also be taken into consideration. This means that the shutdown sequence requires information of the AC voltage direction.

Typically, the turn-off sequence can be implemented by the CLB module of DSP. However, in some cases where high functional safety level is required, the system must be shut down safely even if the DSP loses functionality. In these cases a pure analog design must be proposed as the back-up protection path for functional safety requirements.

3 TPLD Overview and Configuration

3.1 TPLD Overview

Calculating, coding, and processing digital signals build the fundamentals of all kinds of digital controllers. Wider bits and faster clock inside controllers allow users to realize more complex and more integrated designs. However, there is another consideration for safety that asks developers to extract some part of simple logic process out of controllers. For example, there must be a *foot* to press the *brake* when MCU is out of control. Developers are adding multiple AND/OR/D flip-flop in systems to build a proper break. This is stable, but it can be even better: smaller size and more flexible configuration by TPLD.

Table 3-1. Title Here

	Discrete Logic Circuit	TPLD	CPLD/FPGA
Space	Quite large	Optimized small	Medium
Cost	\$	\$	\$\$\$\$
Flexibility	No	Medium	High

Short example to show advantage of TPLD:

$Y=AB/C+/ABC$ requires 2 NOT gates, 4 2-in AND gates and 1 2-in OR gate. Discrete logic circuit costs >30mm², while TPLD801 is only 3.36mm².

Using TPLD series is TPLD support OTP (one-time programmable) through InterConnect Studio means a user can optimize a design in every period of development in the same pin out. Once the design is fixed, OTP is locked to prevent readback of content.

3.2 TPLD Product Resources

Different TPLDs have different numbers of gate resources. All logic gates in TPLD are set as LUT(look-up table). For example, a 3-in AND gate can be described as LUT=111. This means only all inputs of LUT are logic high and output logic high.

Apart from LUTs, there are many blocks inside TPLD that can be used to simplify and optimize the design:

1. Analog Comparator: integrated reference in 32mV division. Directly convert analog signals in the system into operable logic levels based on threshold values without adding extra voltage reference and comparators.
2. Counters and Delay Generators: achieving accurate delay at low cost has always been a challenging problem in systems. However, with the oscillator and delay module inside the TPLD, this can now be accomplished.
3. State Machine: When the logic circuit that is being designing is highly dependent on timing, or that the next state must be determined based on the current state and a specific trigger, try this.

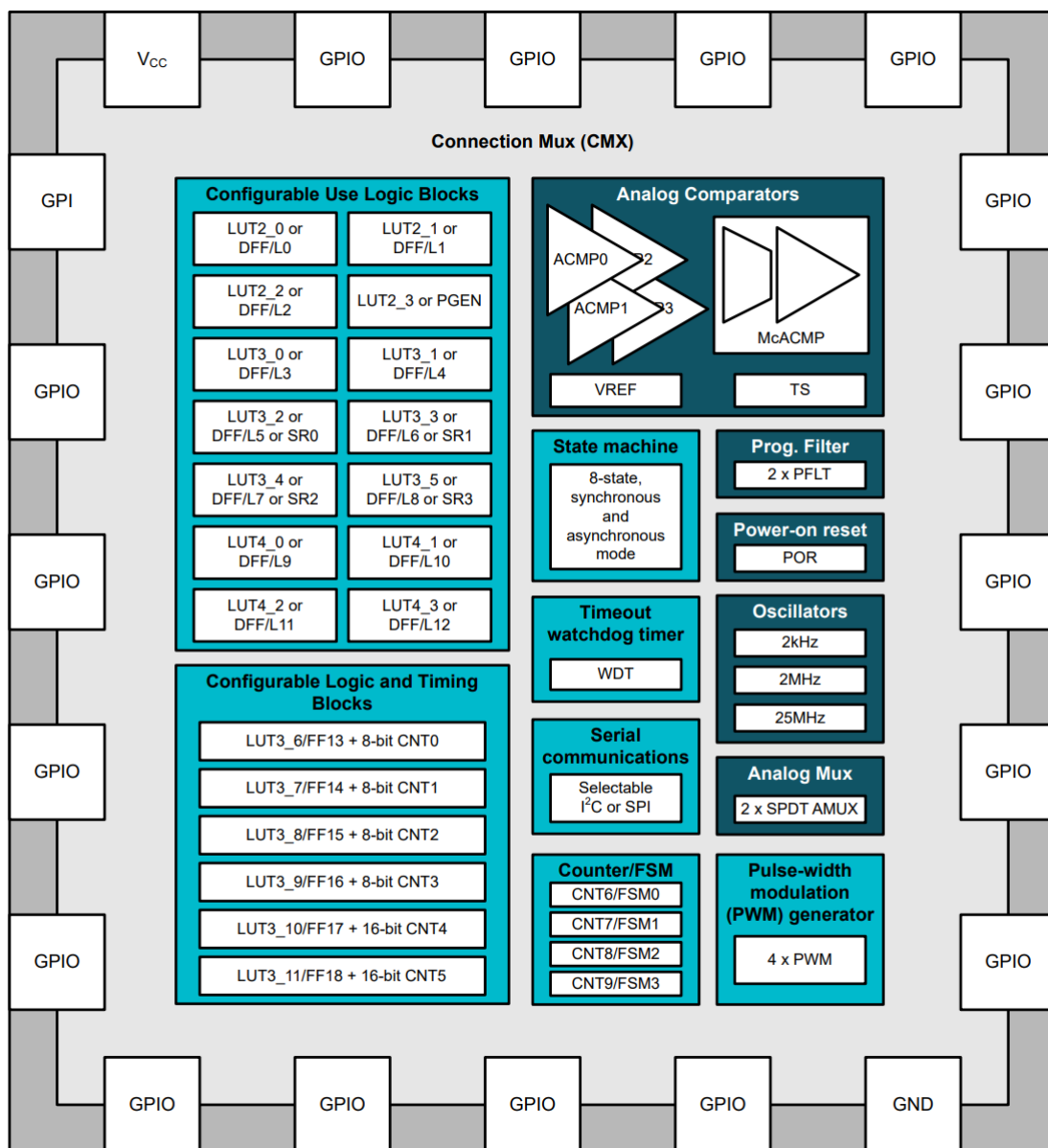


Figure 3-1. TPLD2001-Q1 Block Diagram

In fact, many other interesting functions can be implemented using TPLD, such as analog channel MUX, PWM generation, frequency capture and more. In addition to learning how to use it from the datasheet, there is a useful tool to help the user understand and design a TPLD.

3.3 Start A Circuit Online

INTERCONNECT-STUDIO provide graphical interface for developers to design a circuit.

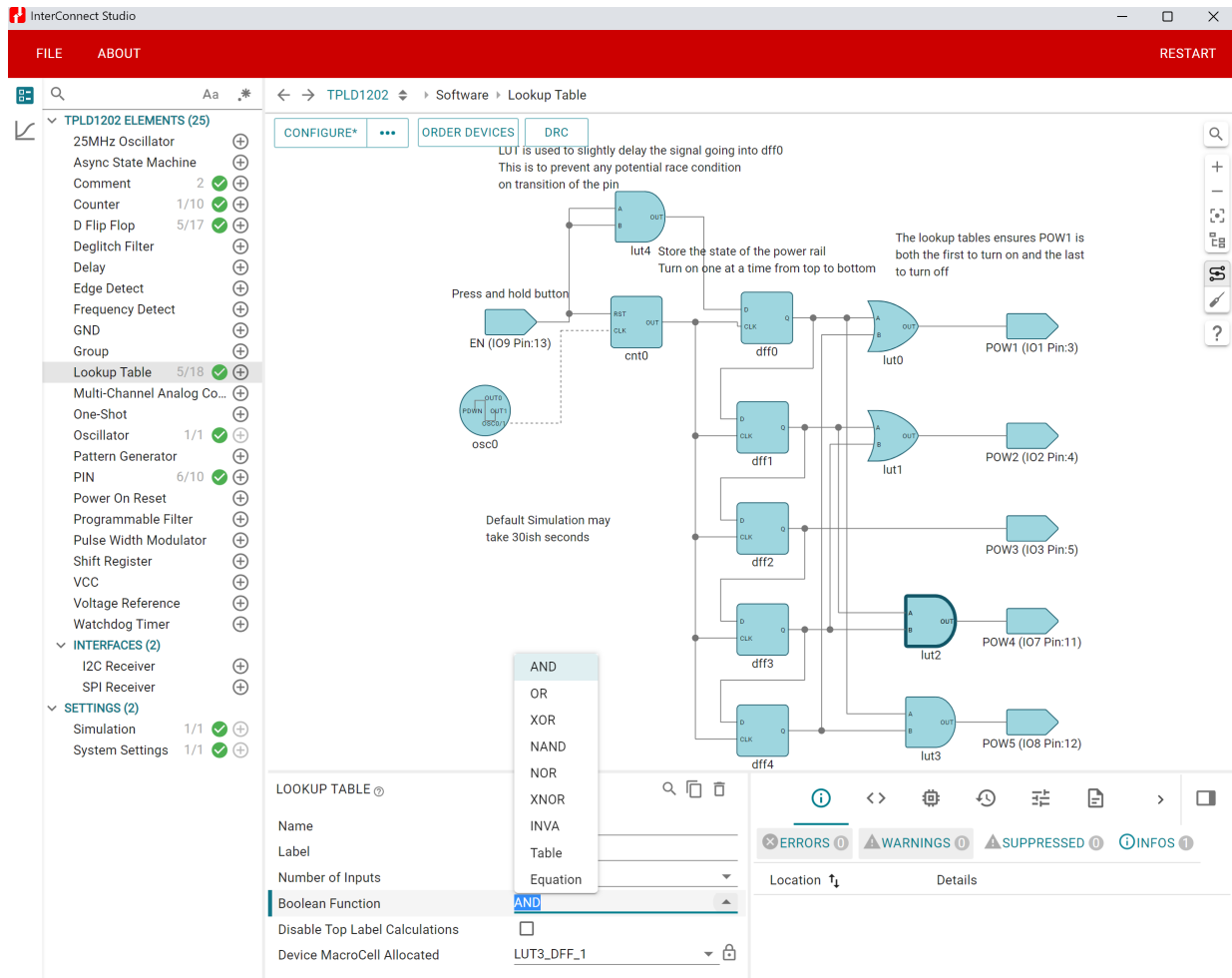


Figure 3-2. TPLD InterConnect Studio

In InterConnect Studio, after selecting the part number and related package, the user can start design and simulate the circuit. Here is an example for realizing power sequences from the reference demo. All blocks on the left can be added into the right zone. There are limits on the number of each block. If there is a red warning, select a higher-end TPLD. For the selected LUT, it can be set with nine kinds of uses depending on developer requirements. Optimize the logic circuit by using the table and equation to save resources.

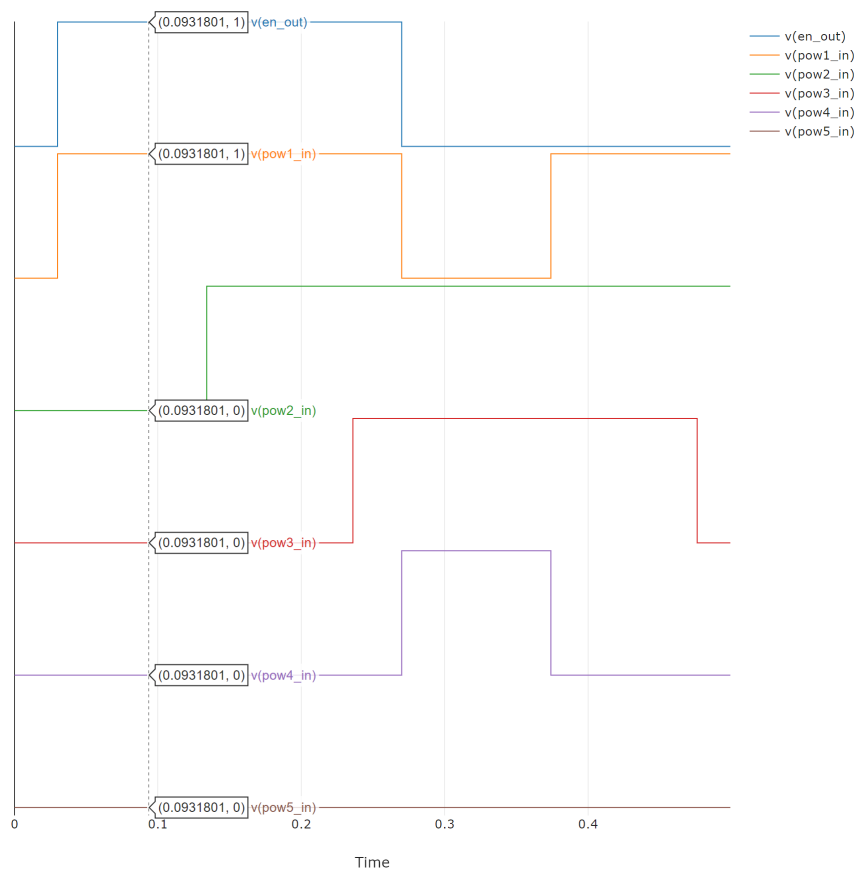


Figure 3-3. TPLD Simulation Waveform

Simulation provides timely design check. Through design, simulation, and redesign, a user can gradually achieve the optimal custom TPLD. Press the CONFIGURE* button and think twice if permanent configuration is required.

4 System Example of TPLD Circuit

To realize the configurable protection and specific turn-off sequences mentioned in [Figure 4-1](#), TPLD2001-Q1 provides a flexible internal logic matrix. Engineers can configure complex timing sequences, interlocking logic, and signal delays without adding external hardware components.

[Figure 4-1](#) shows the system-level connection of the example design and architecture using the TPLD2001-Q1 in an On-Board Charger (OBC) system.

- **Normal Operation:** Under standard operating conditions, PWM signals generated by the MCU (PWM_IN) pass directly through the TPLD2001-Q1 (pass-through mode) to four independent gate driver units: GDU1 (driving G11, G12), GDU2 (driving G21, G22), GDU3 (driving G31, G32), and GDU4 (driving G41, G42).
- **Fault Protection and Shutdown Logic:** If an MCU failure or a system-level fault occurs, the TPLD2001-Q1 acts as a hardware-based safety mechanism. Upon receiving fault triggers, such as a digital fault signal (FLT) from external circuits or an abnormal AC voltage condition through the VAC_SNS input, the TPLD2001-Q1 overrides the MCU control.
- **Flexible Monitoring and Configurable Action:** The VAC_SNS pin allows system monitoring either through TPLD's internal analog comparators or by interpreting external AC voltage sensing signals. Once a protection event is triggered, TPLD2001-Q1 executes a user-configurable, pre-programmed turn-off sequence to safely shut down all gate drivers, preventing thermal damage or power stage destruction.

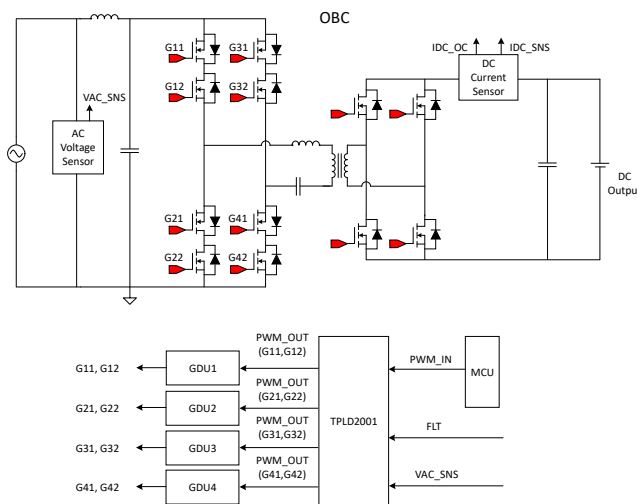


Figure 4-1. TPLD2001-Q1 System Block Diagram

By programming these functional blocks fully inside the TPLD2001-Q1, the entire protection and driving timing circuit is consolidated into a single, highly integrated IC. This substantially reduces total Bill of Materials (BOM) cost, simplifies PCB layout complexity, and improves overall system reliability.

5 Summary

This application note presents a TPLD-based protection implementation for On-Board Charger (OBC) or other applications that require timing protection. By acting as a hardware-based safety mechanism, TPLD2001-Q1 monitors system status and safely overrides the PWM during fault conditions to execute programmable PWM shutdown sequences. Replacing bulky discrete logic gates with TPLD2001-Q1 significantly reduces Bill of Materials (BOM) cost, minimizes PCB footprint, simplifies layout complexity, and boosts overall system reliability.

6 References

1. Texas Instruments, [TPLD2001-Q1 Programmable Logic Device Datasheet](#), datasheet.
2. Texas Instruments, [Towards Functional Safety in On-Board Charger: Design Approach and Component Overview](#), application note.

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