

Application Note

Migrating Between TCAN28xx-Q1 and TCAN29xx-Q1



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Abstract

This migration guide is to assist automotive ECU designers in switching from the TCAN28xx-Q1 system basis chip (SBC) to the newer TCAN29xx-Q1 SBC. This document introduces TCAN29xx-Q1, shows the key differences from TCAN28xx-Q1, and highlights potential design changes a user must make in the system that previously used TCAN28xx-Q1 to enable TCAN29xx-Q1 to work properly.

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1 Introduction

The TCAN29xx-Q1 is a family of system basis chips (SBC) that provides a control area network flexible data rate capable (CAN FD) transceiver in the TCAN294x-Q1 version and a CAN SIC transceiver for the TCAN295x-Q1 versions. The TCAN29x7-Q1 version includes a local interconnect network (LIN) transceiver. The CAN transceiver supports data rates up to 8Mbps while the LIN transceiver supports fast mode data rates up to 200kbps. There are integrated LDOs which can provide power to other external components such as MCUs and sensors. If more current is needed an external PNP transistor can be used for additional power needs. TCAN29xx-Q1 will also provide ASIL-B versions for safety intensive applications.

The TCAN28xx-Q1 is also a family of SBCs with many of the same features as the newer TCAN29xx-Q1 family such as partial networking, WAKE pins, and high-side switches (HSS). Both SBCs come in a 32-pin QFN package (RHB) and are considered pin-to-pin compatible with each other, so moving from the TCAN28xx-Q1 to the TCAN29xx-Q1 allows customers to easily scale their system to higher ASIL ratings without losing key functionality. However, just because they are pin-to-pin compatible does not necessarily mean that you can simply swap out a TCAN28xx-Q1 for a TCAN29xx-Q1 on a PCB and expect the system to work the same as before. It is important to consider the internal differences between both SBC family that can impact hardware or software design.

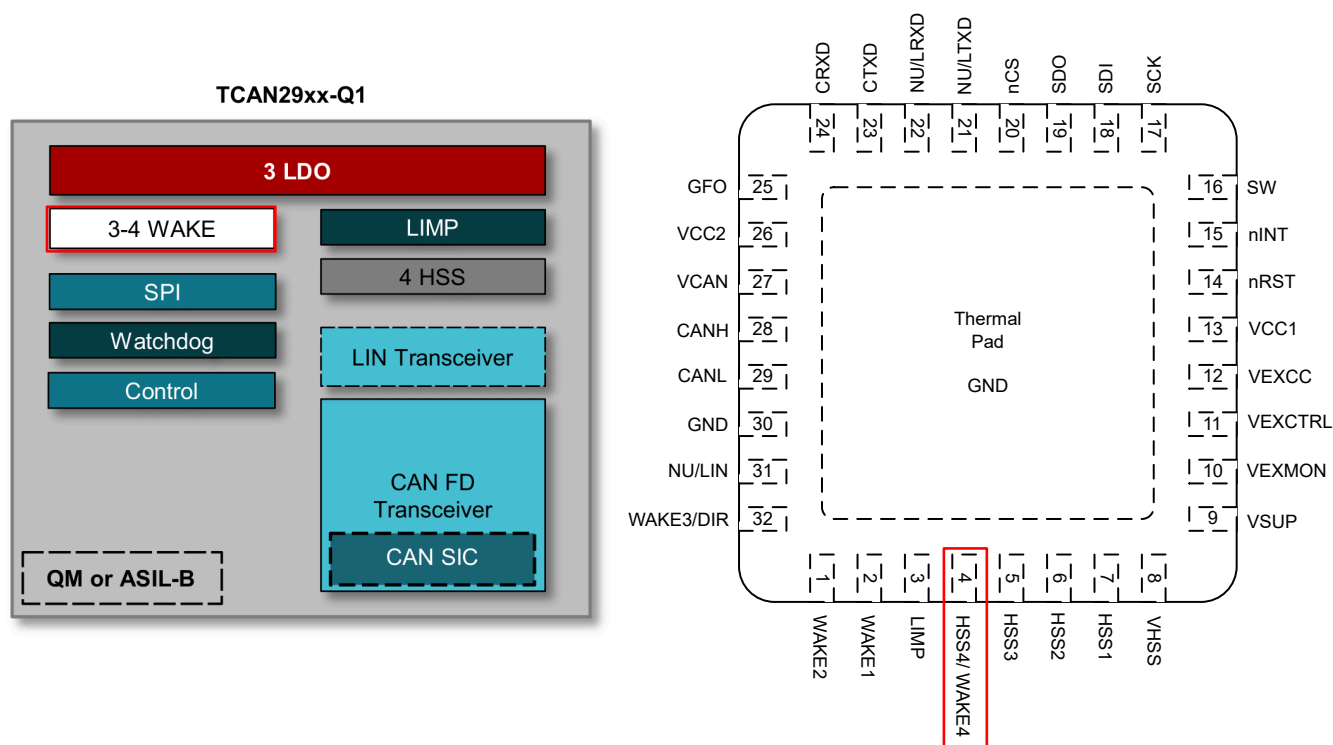


Figure 1-1. TCAN29xx-Q1 Block Diagram and Pinout

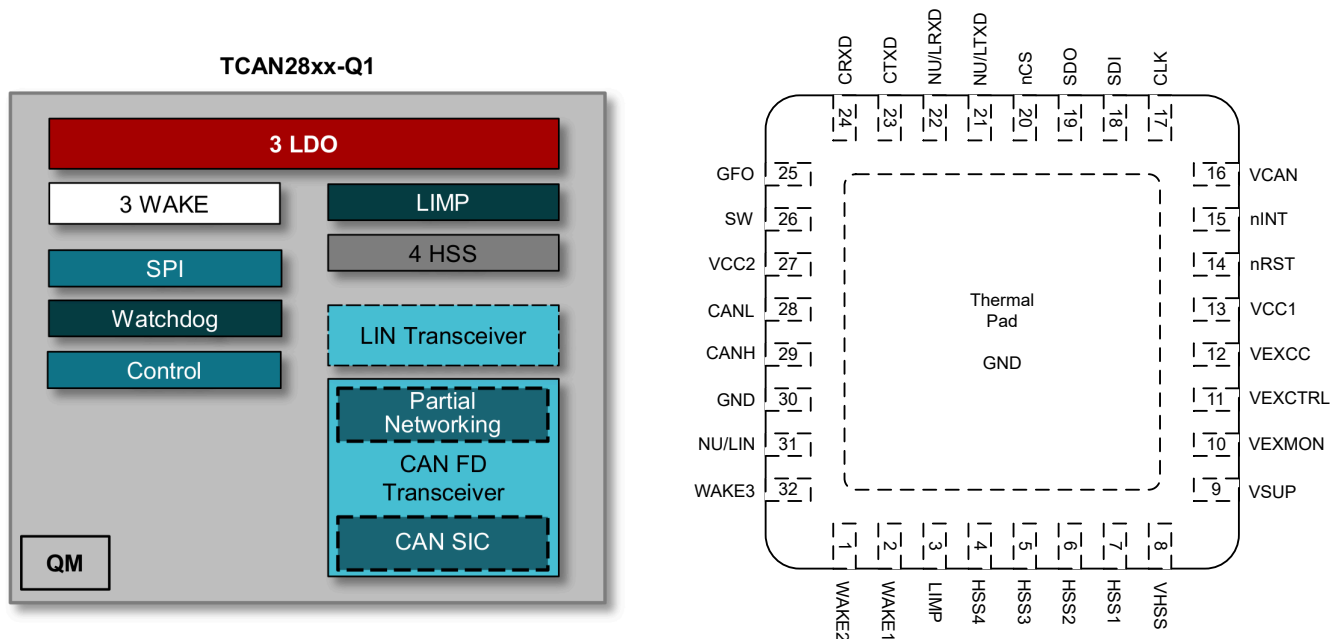


Figure 1-2. TCAN28xx-Q1 Block Diagram and Pinout

2 Detailed Description

2.1 Overview

The following tables shows a high-level overview of the differences between TCAN28xx-Q1 and TCAN29xx-Q1. The following sections discusses each difference.

Table 2-1. Device Comparison

Feature	TCAN29xx-Q1	TCAN28xx-Q1
Functional Safety	ASIL-B, QM	QM
CAN FD	1 CAN-FD/SIC	1 CAN-FD/SIC
Partial Networking	No	Yes
CAN Bus Max DC Voltage Tolerance (V)	±40	±58
LIN	0-1	0-1
LIN Bus Max DC Voltage Tolerance (V)	±40	±58
Customer NVM Programming Method	None (factory only)	EEPROM
LDOs	3	3
VCC1 (V)/(mA)	3.3 & 5/250mA	3.3 & 5/250mA
VCC2 (V)/(mA)	5/100mA (No STB Prot.)	5/200mA (STB Prot.)
VEXCC (V)	1.8/2.5/3.3/5V (STB Prot.)	1.8/2.5/3.3/5V (STB Prot.)
# of HSS	4	4
HSSx (RDSO)/ILIM-min	7Ω/150mA	5Ω/150mA
Fail Outputs (LIMP)	1	1
# of WAKE Pins	4 HV, 1 LV	3 HV, 1 LV
Watchdog	TO, WWD, Q&A	TO, WWD, Q&A
HBM Local Pins (kV)	±2	±4
HBM Global Pins (kV)	±8	±8
IEC Contact Global Pins (kV)	±8	±8

1. STB=short-to-battery, HV=high voltage, LV=low voltage, TO=timeout, WWD= window watchdog, Q&A=question & answer

2.2 Functional Safety

TCAN29xx-Q1 offers both ASIL-B rated and Functional Safety-Quality Managed variants while TCAN28xx-Q1 only offers Functional Safety-Quality Managed variants. Automotive Safety Integrity Level (ASIL) B is a risk category defined by the ISO 26262 functional safety standard that TCAN29xx-Q1 was designed to adhere to. ASIL rated devices like TCAN29xx-Q1 are also considered Functional Safety-Compliant per TI standards and include additional resources like fault-tree analysis (FTA). Functional Safety-Quality Managed devices like TCAN28xx-Q1 provide device data to support designers of functional safety systems, but certain safety mechanisms, such as voltage supervisors, that are included in ASIL rated devices would need to be implemented externally on the PCB. (see <https://www.ti.com/technologies/functional-safety.html> for more info).

Two of the main safety mechanisms TCAN29xx-Q1 implements internally to reach ASIL-B is a separate bandgap reference for cross monitoring the main bandgap reference and Analog Built-In Self-Test (ABIST) which acts as an on-chip diagnostic mechanism that automatically verifies the health of the circuitry in the device such as voltage monitors, comparators, and temperature sensors. For further information about the additional functional safety mechanisms and information of TCAN29xx-Q1, refer to the documents below which can be found in the product folder on ti.com:

- Functional safety manual
- FMEDA
- Functional Safety Analysis Report Summary
- Family Quantitative Functional Safety Analysis Report (SN29500 for the die)
- Family Quantitative Functional Safety Analysis Report (IEC 62380 for the package & die)

2.3 CAN Transceiver

Both SBC families include a CAN-FD or CAN-FD SIC transceiver that supports data rates up to 8Mbps. However, TCAN29xx-Q1 does not offer any variants that support partial networking/selective wake, unlike devices such as TCAN2845-Q1.

Design Consideration: If the system you are designing requires partial networking, consider adding a separate partial networking CAN transceiver such as TCAN1575-Q1 to the ECU to enable this capability. See the following figure for details.

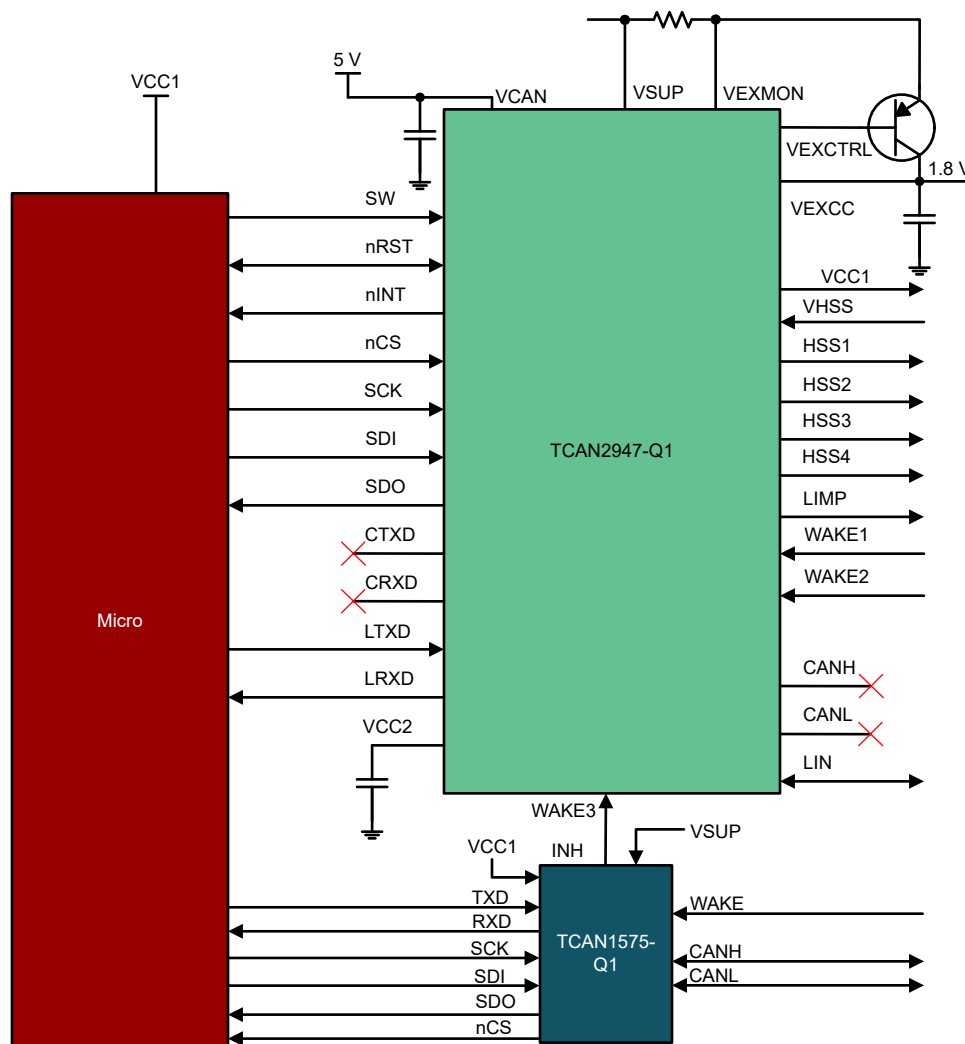


Figure 2-1. TCAN29xx-Q1 Partial Networking Design Example

TCAN29xx-Q1 has a lower fault tolerance on the CANH and CANL pins compared to TCAN28xx-Q1 (40V vs 58V). This also applies to the LIN transceiver as well.

Design Consideration: If your system is prone to overvoltage on the CAN/LIN bus that exceeds 40V, considering shortening the cable length or adding clamping circuitry on the CANH and CANL and/or LIN pins to reduce the voltage seen by the device to not violate the pin ratings.

While TCAN28xx-Q1 detected a variety of CAN bus faults such as an open bus or short-to-ground, the TCAN29xx-Q1 will only detect "short" faults on the CAN bus (short-to-ground, short-to-battery, and so on.).

Design Consideration: If you were relying on TCAN28xx-Q1 to detect non-short faults, this needs to be done externally when using TCAN29xx-Q1.

2.4 LDOs

Both SBC families have 3 low-dropout regulators (LDOs): VCC1, VCC2, and VEXCC. In TCAN29xx-Q1, VCC1 will still be the main LDO that controls state transitions and SPI communications and can supply up to 250mA. However, VCC2 on TCAN29xx-Q1 is limited to 100mA and is not short-to-battery protected or -1V GND shift protected.

Design Consideration: Make sure the VCC2 loads of TCAN29xx-Q1 are not drawing more than 100mA and are not at risk of a short-to-battery or ground shift event. If they are, use VEXCC instead or add extra protection circuitry such as Zener diodes and reverse polarity protection diodes.

VEXCC in TCAN29xx-Q1 will have tighter Vshunt threshold for better current limiting capabilities. No design change is needed in this regard when switching over from TCAN28xx-Q1, but something to consider if you are wanting to potentially shrink the size of your PNP transistor since the current will be limited sooner.

Load sharing between VCC1 and VEXCC differs slightly between TCAN28xx-Q1 and TCAN29xx-Q1. In TCAN28xx-Q1, the current limit and current ratio between VCC1 and VEXCC is determined solely based off the Rshunt value between VSUP and VEXMON. However, when you are load sharing, the current limit is disabled on VEXCC. In TCAN29xx-Q1, the ratio is set by setting the VEXCC_VCC1_LOAD_RATIO register bit field to the desired ratio. This allows for current limiting in load sharing and standalone mode for VEXCC.

Design consideration: To share loading between VCC1 and VEXCC with TCAN29xx-Q1, be sure to set the ratio via a register write and adjust the value of Rshunt accordingly.

2.5 State Machine

TCAN29xx-Q1 follows essentially the same state machine and SBC modes as TCAN28xx with some minor differences:

- In Sleep mode, VCC1 will always be off. Standby mode is the lowest power mode you can be in while keeping VCC1 turned on. (See the following image for TCAN29xx-Q1 State Machine)
 - **Design Consideration:** If VCC1 is powering the MCU, the MCU will turn off when the SBC transitions to Sleep mode. The MCUs software should take this into account since it will essentially restart every time the SBC wakes up if it is powered by VCC1. Since VCC1 is off in the Sleep mode, watchdog will also be disabled in Sleep mode.

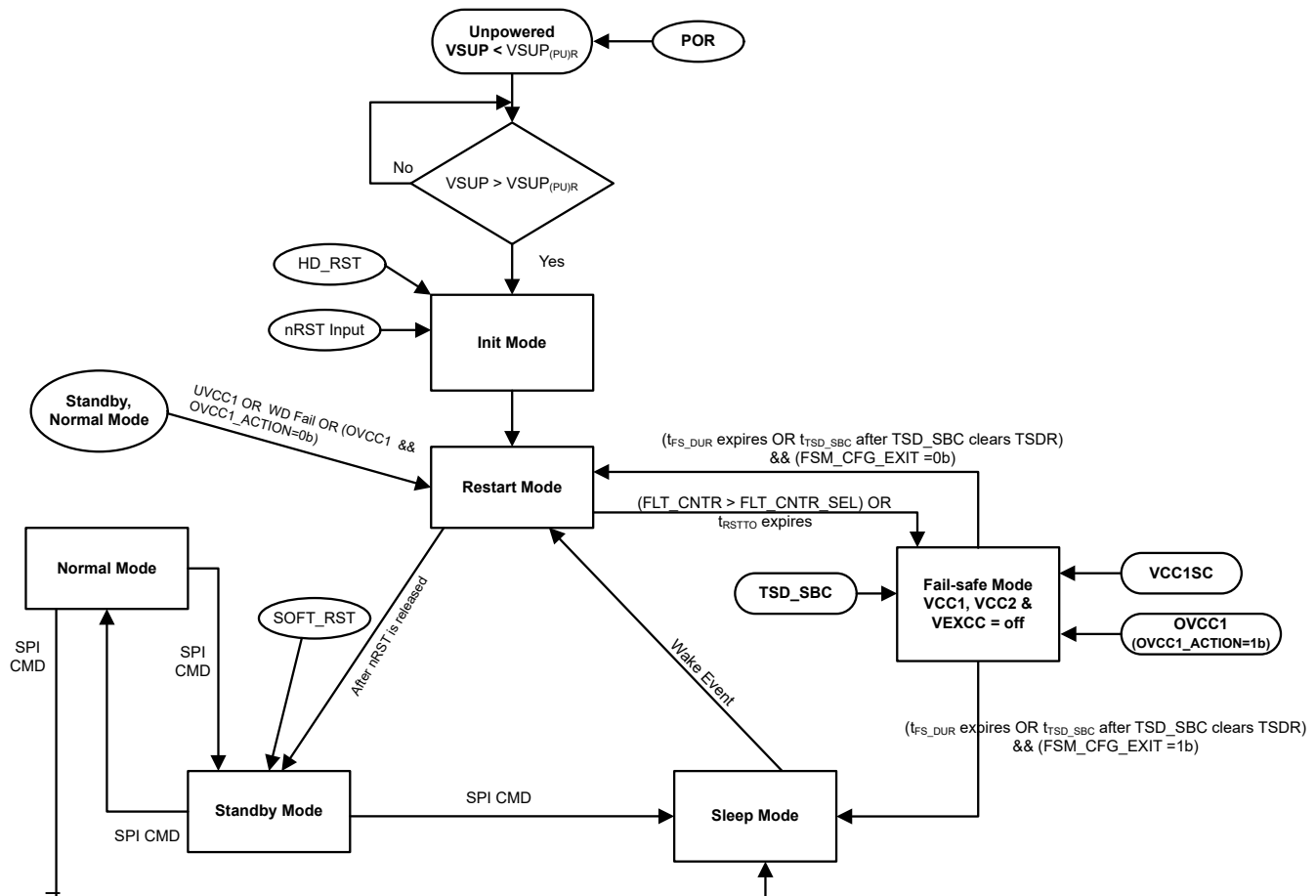


Figure 2-2. TCAN29xx-Q1 State Diagram

- The restart counter (RSRT CNTR) in TCAN28xx-Q1 increments every time the device goes into Restart mode. In TCAN29xx-Q1, this is replaced with the "fault counter", and it only increments when a fault causes the SBC to transition to Restart mode. These faults included watchdog error, UVCC1, and OVCC1 (when the option is to not enter Fail-safe mode directly).
- TCAN29xx will auto-recover from fail-safe mode (FSM) after 250ms and does not need a wake event unless FSM_EXIT_CFG is set to 1b, which causes it to go to Sleep mode.
- Fail-safe mode (FSM) is now always enabled in TCAN29xx-Q1 with no FSM counter for functional safety compliance. Having no FSM counter would be the same as if you had FSM_DIS always set to 0b and FSM_CNTR_SET always set to 0000b in TCAN28xx-Q1.
 - Design Consideration:** The FSM_DIS register fields will no longer exist since FSM is always enabled in TCAN29xx. In the event of an SBC fault, the device will immediately go to FSM by default. To allow for multiple faults of a missed watchdog, UVCC1, or OVCC1, you will need to rely solely on the fault counter to do this (located in register 16h).

2.6 Watchdog

The watchdog TCAN29xx-Q1 will have all the same features as the watchdog in TCAN28xx-Q1. However, one additional feature that TCAN29xx-Q1 adds is that when entering standby mode from a wake event, a register bit can be set to require one watchdog trigger, even if watchdog is disabled in standby mode. This feature is disabled by default but can be enabled via the WD_STBY_EN_ON_WK bit in WD_CONFIG_1.

2.7 SW Pin

The SW pin acts as a software development pin where, when it is active, watchdog servicing is not required. However, in TCAN29xx-Q1, making the SW pin active also moves the CAN and LIN transceivers in the device to the On state, whereas in TCAN28xx-Q1, a register write to CAN_CNTRL_1 and/or LIN_CNTRL is required to move the transceivers to the On state.

Design Consideration: If you want to save power in Standby mode by keeping the CAN and LIN transceivers in a mode other than On, be sure the SW is not active.

2.8 High-Side Switches (HSSs)

TCAN29xx-Q1 will still have 4 programmable HSSs which can be configured for pulse width modulation (PWM), timer based output, or constant DC output, just like TCAN28xx-Q1. However, the HSSs in TCAN29xx-Q1 will have reduced quiescent current when they are enabled. They will also have a new optional low power mode which reduces the quiescent current even more at the cost of wider current limit variation.

In TCAN28xx-Q1 the only way for an HSS to stay on in Sleep mode was with direct drive or if it was being used for cyclic sensing wake. However, any HSS in TCAN29xx-Q1 can be configured for PWM, DC, or timer based outputs when in Sleep mode.

Design Consideration: If the system is relying on an HSS to turn off automatically in Sleep mode, the respective HSS_CNTRL register will need to be modified to ensure this happens. Otherwise the HSS will stay in whatever mode it was in prior to going to sleep.

The HSS in TCAN29xx-Q1 will have a higher RDSON compared to TCAN28xx-Q1. This will increase the heat across each switch in the device.

Design Consideration: The PCB designer needs to ensure that the extra heat is accounted for in the board layout to not exceed the max junction temperature of the SBC. Refer to thermal table in the TCAN29xx-Q1 datasheet for details.

2.9 WAKE Pins

TCAN29xx-Q1 adds an additional high voltage WAKE pin which is multiplexed with the HSS4 pin (pin 4). Only one function can be used at a time for this pin. If pin 4 is configured as WAKE4, HSS3 is used for cyclic sensing wake, if applicable.

Design Consideration: If HSS4 is intended to be used for cyclic sensing wake, make sure the relevant registers are configured properly and it is not configured to be used as WAKE4.

2.10 Long Duration Timer and Cyclic Wake

The longest timer provided in the TCAN28xx-Q1 can only last up to 10 minutes. TCAN29xx-Q1 adds a long duration timer which can last up to 14 days.

With the addition of the Long Duration Timer, the way cyclic wake functionality is implemented has changed. In TCAN28xx-Q1, cyclic wake was a way for the device to self-wake when it transitions into Sleep mode via a SPI command. This was done by configuring Timer1 or Timer2 and enabling cyclic wake in Sleep mode by setting SLP_CYC_WK_EN to 1b. Cyclic wake also had some functionality in Normal and Standby mode where instead of a wake event happening, the nINT pin would just be pulled low based on the Timer1 or Timer2 configuration. However in TCAN29xx-Q1, the Long Duration Timer is the only way to have the device self-wake from Sleep mode if it goes to sleep via a SPI command. The *cyclic wake* feature only applies to normal or standby mode in TCAN29xx-Q1.

Design Consideration: If you were using cyclic wake in TCAN28xx-Q1 as a way for the device to self-wake from Sleep mode, you will need to transition this functionality to the Long Duration Timer in TCAN29xx-Q1 which uses different registers and register fields. Also, the shortest time the Long Duration Timer offers is 5s whereas timer1 or timer2 only span from 0.1ms to 200ms, so your minimum wake up time will increase with TCAN29xx-Q1 (for example, the device stays asleep for longer before it wakes up).

2.11 Register Map

TCAN29xx-Q1 shares many of the same registers, addresses, and bit fields as the TCAN28xx-Q1 register map. However, there are some differences that should be accounted for in the MCU software. See the following table for a high-level comparison of these register differences. For full details, please consult the device datasheet.

Table 2-2. Register Comparison

Register Address	TCAN28xx-Q1 Register Name	TCAN29xx-Q1 Register Name	Comment
0Dh	VREG_CONFIG1	VREG_CONFIG1	Removed VCC1_CFG since VCC1 always turns off in Sleep mode in TCAN29xx-Q1.
0Eh	SBC_CONFIG1	SBC_CONFIG1	Removed CAN_SLOPE_CTRL_EN, FSM_CYC_WK_EN, VCC1_SLP_ACT, and SW_FSM_EN bit fields. Selective wake and slope control were removed, and TCAN29xx-Q1 will always auto-wake from fail-safe mode.
10h	CAN_CNTRL_1	CAN_CNTRL1	Removed SW_EN, CAN1_FSM_DIS bit fields since selective wake is not present and the CANTRX is always wake capable in TCAN29xx-Q1. The CAN_WUP_PATTERN bit field was also added.
11h	WAKE_PIN_CONFIG1	WAKE_PIN_CONFIG1	Removed the option for a pulse configuration and the WAKE_WIDTH_INVALID and WAKE_WIDTH_MAX bit fields.
12h	WAKE_PIN_CONFIG2	WAKE_PIN_CONFIG2	Removed WAKE_PULSE_CONFIG bit field.
13h	WD_CONFIG_1	WD_CONFIG_1	Bit 3 become WD_STBY_EN_ON_WK since watchdog cannot be enabled during sleep mode in TCAN29xx-Q1.
16h	WD_RST_PULSE	WD_RST_PULSE	RSRT_CNTR becomes FLT_CNTR
17h	FSM_CONFIG	FSM_CONFIG	Removed FSM_CNTR_ACT bit field and modified options in remaining bit fields to reflect functionality updates in TCAN29xx-Q1 such as ABIST failure flags. FSM_DIS is also changed to FSM_EXIT_CFG since fail safe mode is always enabled in TCAN29xx-Q1.
18h	FSM_CNTR	FSM_CNTR	All bit field in this register are now RSVD in TCAN29xx-Q1
1Ah	DEVICE_CONFIG1	DEVICE_CONFIG1	LIMP_SLP_FLT_EN bit field is now RSVD because TCAN29xx-Q1 always goes fail-safe mode and LIMP turns ON and stays ON even when sleep mode is entered based on FSM_EXIT_CFG. FSM_CYC_SEN_EN and LIMP_DIS bit fields are also removed.

Table 2-2. Register Comparison (continued)

Register Address	TCAN28xx-Q1 Register Name	TCAN29xx-Q1 Register Name	Comment
1Bh	DEVICE_CONFIG2	DEVICE_CONFIG2	WAKE_WIDTH_MAX_DIS bit field is removed because the pulse configuration for a WAKE pin is not available in TCAN29xx-Q1
1Ch	SWE_TIMER	LDT_TIMER	Removed SWE timer and replaced with long duration timer
1Fh	PWM1_CNTL1	DEVICE_CONFIG3	DEVICE_CONFIG3 provides low power mode enables for HSSs and VEXCC/VCC1 load sharing ratio not previously available in TCAN28xx-Q1
20h	PWM1_CNTL2	PWM1_CNTL1	PWM_CNTL bits are rearranged due to HSS modifications.
21h	PWM1_CNTL3	PWM1_CNTL2	PWM_CNTL bits are rearranged due to HSS modifications.
22h	PWM2_CNTL1	PWM_RSVD	Removed 3 rd control register since certain bits were consolidated in 1 and 2.
23h	PWM2_CNTL2	PWM2_CNTL1	PWM_CNTL bits are rearranged due to HSS modifications.
24h	PWM2_CNTL3	PWM2_CNTL2	Removed 3 rd control register since certain bits were consolidated in 1 and 2.
25h	TIMER1_CONFIG	TIMER1_CONFIG	Removed the option to keep on HSS constantly on via the TIMER1_ON_WIDTH bit field. It should be done via the HSS_CNTRL registers
26h	TIMER2_CONFIG	TIMER2_CONFIG	Removed the option to keep on HSS constantly on via the TIMER2_ON_WIDTH bit field. It should be done via the HSS_CNTRL registers
28h	RSRT_CNTR	FLT_CNTR	Fault counter settings vs restart counter settings
2Ah	WAKE_PIN_CONFIG3	WAKE_PIN_CONFIG3	Adds WAKE4 bit fields.
30h – 47h	Selective wake registers	RSVD	TCAN28xx-Q1 uses registers 30h – 47h for selective wake. TCAN29xx doesn't use these since it does not support selective wake.
4Bh	RSVD	ABIST_CONFIG (only in TCAN29xxB versions)	TCAN28xx-Q1 does not have ABIST
4Ch	RSVD	ABIST_STATUS (only in TCAN29xxB versions)	TCAN28xx-Q1 does not have ABIST
4Eh	EEPROM_CONFIG	RSVD	EEPROM is removed in TCAN29xx-Q1
4Fh	HSS_CNTL3	HSS_CNTL3	RSTRT_TMR_SEL bit field is replaced with HSS_OC_FLTR. SLP_CYC_WK_EN bit field is also removed.
50h	INT_GLOBAL	INT_GLOBAL	ABIST interrupts are indicated in bit field 1 in TCAN29xx-Q1
51h	INT_1	INT_1	WKERR is now the LDT interrupt. FRAME_OVF_1 interrupt is also removed.
52h	INT_2	INT_2	SMS and SME interrupts are removed

Table 2-2. Register Comparison (continued)

Register Address	TCAN28xx-Q1 Register Name	TCAN29xx-Q1 Register Name	Comment
53h	INT_3	INT_3	SWERR interrupt is removed. RSTR_CNT and CRC_EEPROM are also changed.
5Ah	INT_4	INT_4	CYC_WUP interrupt is replaced with LDT_WAKE. EEPROM_CRC_INT is also removed.
5Bh	RSVD	INT_5	INT_5 contains overcurrent, clock failure, and HSS readback interrupts that TCAN28xx does not contain.
5Fh	RSVD	INT_EN_5	INT_5 mask
63h - 64h	RSVD	INT_BIST1,2	ABIST interrupts
78h – 7Ah	RSVD	ID pin registers	The WAKE pin of TCAN29xx-Q1 can also serve as ID pins. Since TCAN28xx-Q1 WAKE pins don't have this function, these registers aren't used.
7Bh	RSVD	WAKE_PIN_CONFIG5	Contains registers for WAKE4.

3 Summary

In conclusion, both TCAN28xx-Q1 and TCAN29xx-Q1 are CAN system basis chips that can be used in the same systems (apart from a few things like ASIL rating) if the designer fully understands the differences between the two. Consulting this app note in conjunction with the device datasheet and functional safety documentation will make that process easy.

4 References

1. Texas Instruments, [TCAN29xx-Q1 Automotive, Functional Safety-Compliant CAN FD and LIN System Basis Chip \(SBC\) Family With Integrated LDOs and Enhanced Diagnostics](#), datasheet.
2. Texas Instruments, [TCAN285x-Q1 Automotive CAN FD SIC and LIN System Basis Chip \(SBC\) with Wake Inputs and High-side Switches](#), datasheet.
3. Texas Instruments, [TI Functional Safety Page](#), webpage.

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