Application Note

Highly Integrated Design and Application Design for TBOX Backup Battery System

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Abstract

The TBOX backup battery system is evolving from discrete to integrated design. The TPS6138x-Q1 family realizes single-chip high-level integration through architectural innovations including stacked MOSFET load-dump protection, integrated power MOSFETs, and intelligent mode management, thereby overcoming design constraints of conventional discrete implementations. This application note provides comprehensive technical analysis of the monolithic integrated architecture, operational mechanisms, and key design challenges, serving as a detailed technical reference for developing next-generation highly integrated backup battery system.

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1 Introduction to Backup Battery Solution in TBOX

TBOX systems serve as core components of the Internet of Vehicles (IoV), playing a pivotal role in bridging the gap between the external world and automotive platforms. These systems integrate multiple external wireless services, including 4G/5G Modem, GPS, BLE, WiFi, and V2X, and facilitate information exchange between the telematics application processor and internal automotive networks (comprising CAN, Ethernet, and LIN protocols).

From a technological evolution standpoint, as illustrated in Figure 1-1, TBOX system is advancing toward higher-level algorithmic data processing, upgraded positioning technologies, and enhanced cybersecurity compliance. The transition from 5G to 5G-A enables TBOX systems to support massive data transmission, meeting the demands of high-precision fusion positioning while strengthening end-to-end encryption and regulatory compliance requirements. Concurrently, technological iterations are driving the integration of TBOX into cockpit platforms, fostering resource sharing of computing power and hardware assets to enhance overall system performance.

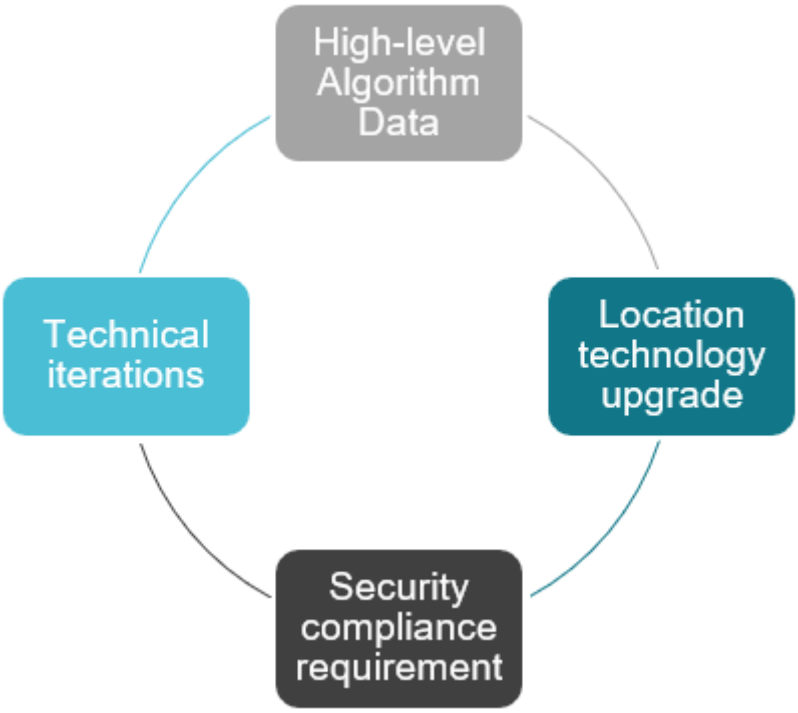


Figure 1-1. TBOX Trends

Figure 1-2 illustrates the architectural evolution of backup battery systems in next-generation intelligent cockpit platforms. While traditional solutions rely on highly distributed discrete components, the integrated approach provides improved alignment with system requirements and elevated power efficiency.

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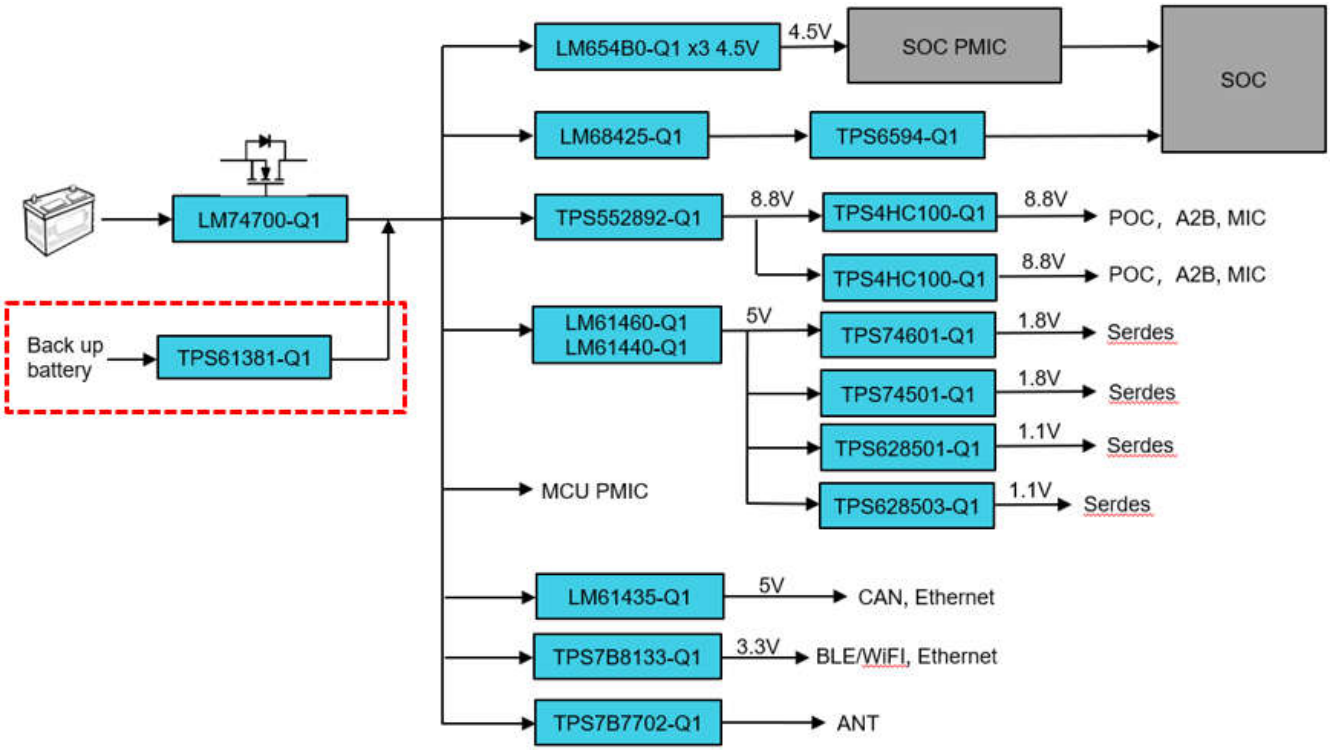


Figure 1-2. Cockpit Integrates with TBOX

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2 Discrete Solution and Integrated Solution for Back up Battery System

In the automotive telematics (T-BOX) system, the auxiliary battery must maintain critical functions including emergency calling (eCall), Over-The-Air (OTA) updates, and location reporting upon main power supply failure. The integration level of the charging and discharging management scheme directly determines the bill of materials (BOM) cost, printed circuit board (PCB) area, and overall system reliability.

The discrete component approach is fundamentally constrained by high component count, substantial quiescent power consumption, and increased control complexity. As illustrated in Figure 2-1, this solution comprises multiple discrete components, including a BQ25171-Q1 linear charger, LM5152-Q1/TPS61088-Q1 boost converters, three power MOSFETs, and two I²C interfaces. It additionally requires occupying the operational amplifier or microcontroller unit (MCU) analog-to-digital converter (ADC) resources for voltage and current acquisition. Within this discrete approach, the charger's integrated low-dropout regulator (LDO) cannot support charging currents exceeding 1 A, making it difficult to meet fast-charging requirements. Mode switching among discharge, charge, and battery health monitoring functions relies entirely on MCU control, resulting in limited mode transition speed. Furthermore, the high-side MOSFET exhibits excessive leakage current reaching 200 nA, resulting in unacceptably high static power consumption.

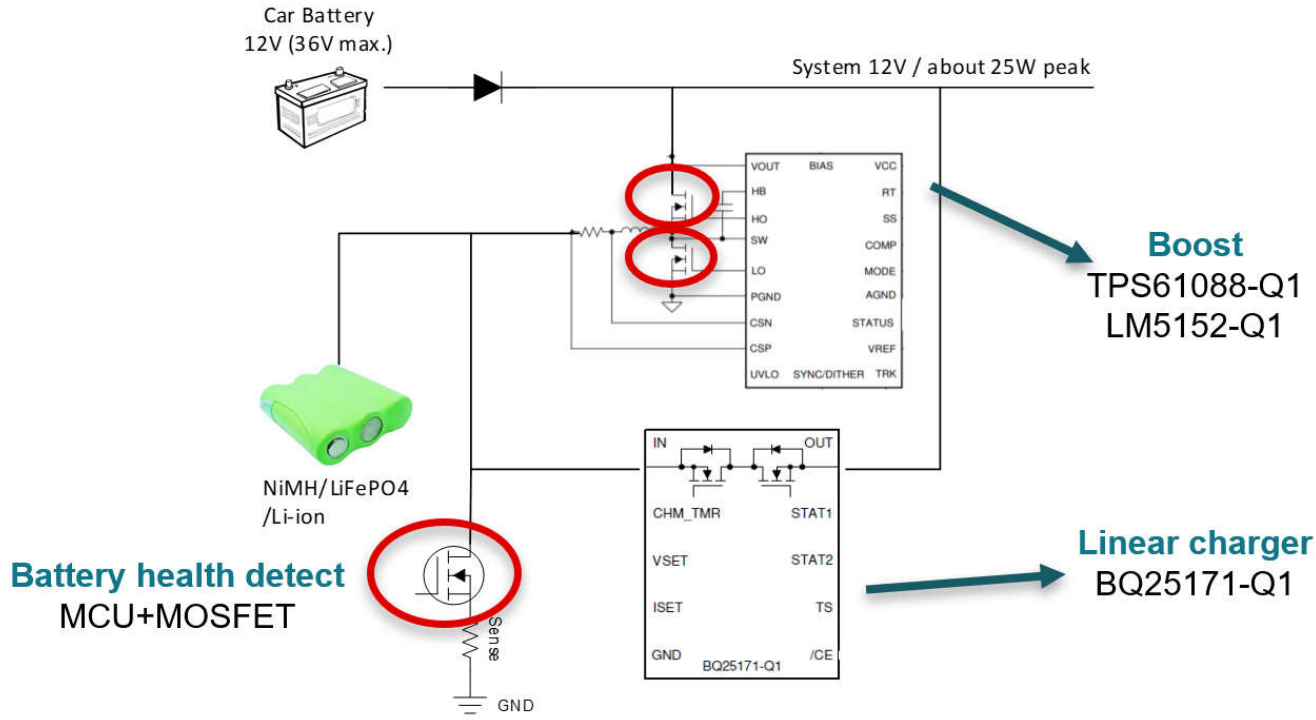


Figure 2-1. Discrete Solution

In comparison with existing package-level integrated solutions available in the market, the TPS6138x-Q1 series achieves function-level integration and implements architectural-level optimization. This device integrates three distinct functions—boost, charging, and battery state-of-health (SOH) detection—into a single chip.

As shown in Figure 2-2, the device incorporates integrated isolation MOSFETs and supports multiple backup battery chemistries including Nickel-Metal Hydride (NiMH), Lithium Iron Phosphate ($LiFePO_4$), and Lithium-ion (Li-ion). Compared to the discrete component approach, the TPS6138x-Q1 occupies significantly reduced PCB area of only 0.799 square inches (versus 1.428 square inches for the discrete solution). The charging mode supports both LDO and buck configurations, delivering a comprehensive charging architecture with multi-level charging protection and NTC thermistor-based temperature monitoring. The boost mode achieves a remarkably low minimum input voltage of 1V.

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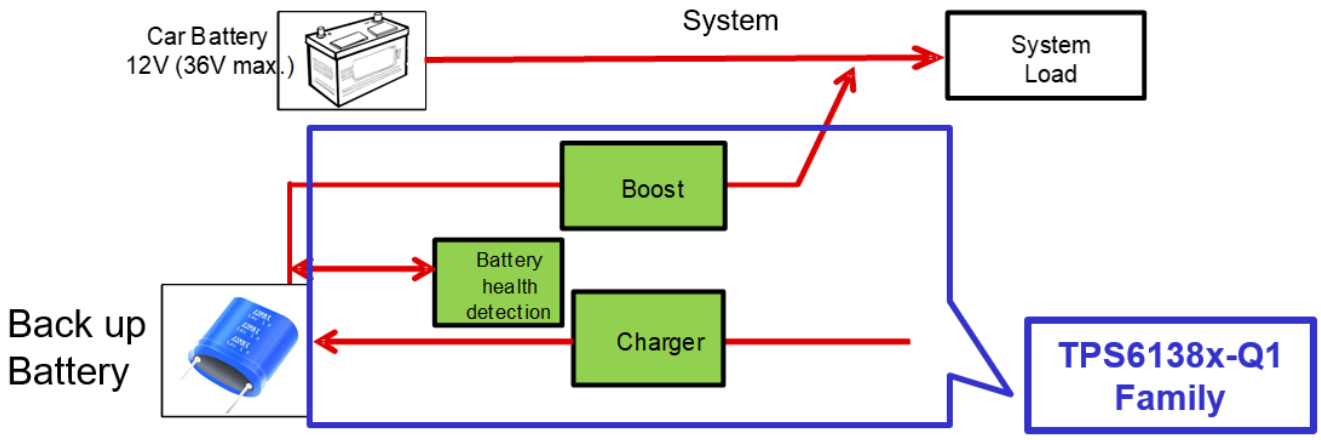


Figure 2-2. Integrated Solution of TPS6138x-Q1

Regarding mode transition and switching capability, when the vehicle's primary battery operates normally, the system can operate in standby, charging, or SOH monitoring mode to achieve efficient power management and battery health assessment. Upon primary battery failure causing voltage drop, the chip leverages a rapid response mechanism to automatically switch to boost mode within 20 microseconds, utilizing the backup battery to continuously supply power to the system load and ensure the normal operation of critical functions, thereby significantly enhancing system reliability.

By employing the new process technology, the design not only satisfies the stringent requirements of automotive electrical environments but additionally achieves 30% chip cost reduction, establishing an excellent balance between performance and cost. This makes the device particularly well-suited for space and cost-sensitive backup battery management systems in automotive applications.

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3 Design Considerations for Application of TPS6138x-Q1

3.1 TPS6138x-Q1 Schematic Key Points

The TPS6138x-Q1 is a highly integrated power management IC whose schematic design encompasses several critical design considerations, as illustrated in Figure 3-1. In the grounding architecture, analog ground (AGND) and power ground (PGND) must be segregated and connected at a single point. This segregation strategy is essential to prevent voltage drops across the ground return path caused by large currents circulating in the power circuits, which would otherwise introduce detrimental interference to sensitive analog circuitry. Connecting the VCC, COMP, AGND pins, and thermal pad to AGND further ensures the stability of analog signals, since these components are intimately associated with the chip's internal analog circuits. Unified grounding of these elements effectively reduces noise induced by potential differences.

Regarding driver design, resistor R5 is employed to drive Q1 with a resistance value in the range of 1–3Ω, primarily to limit the drive current and damping gate voltage oscillation. The selection of MOSFET package size is recommended to be 3mm x 3mm, motived by the balance of thermal dissipation capability and layout convenience.

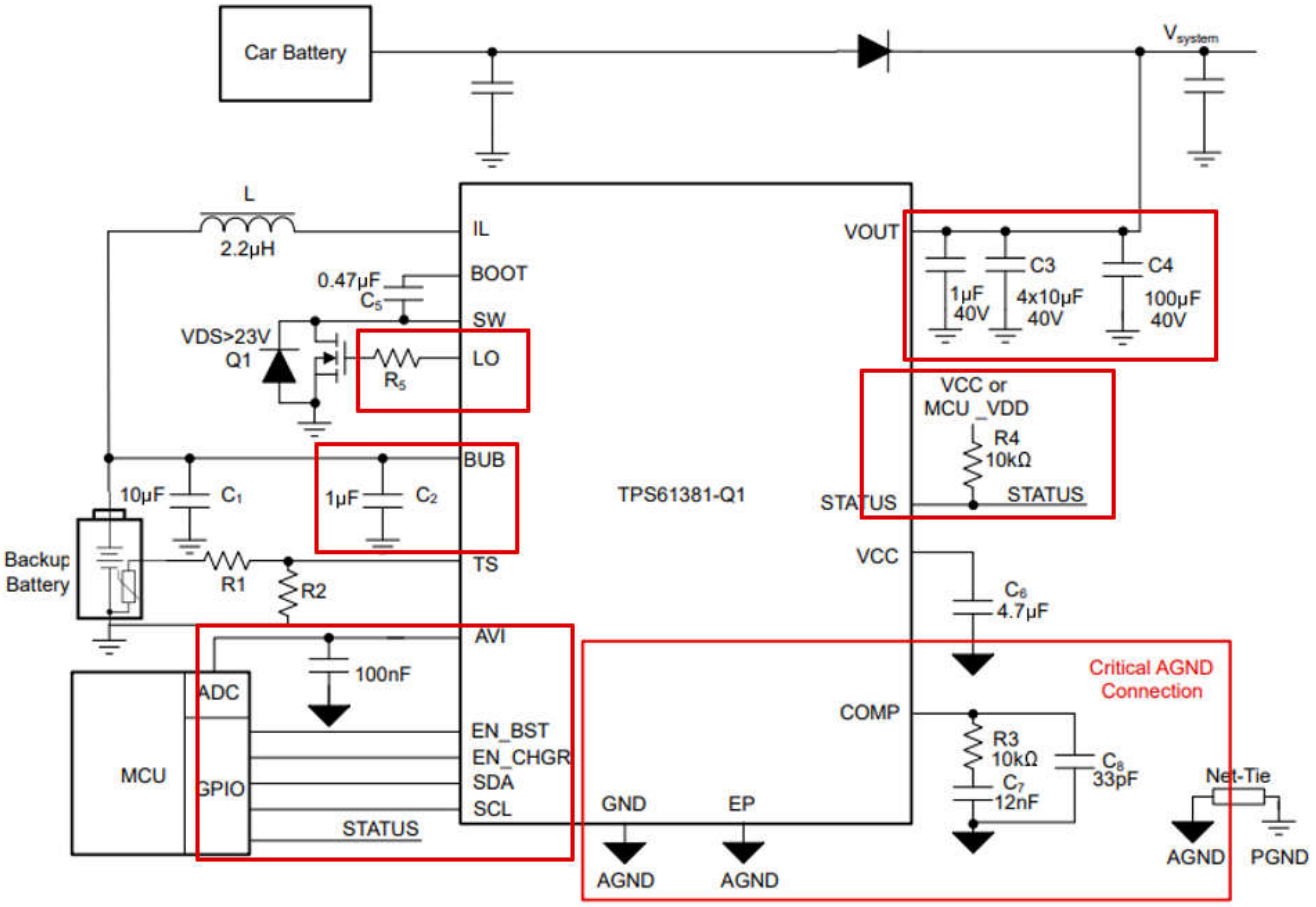


Figure 3-1. Schematic Key Points

The pin design for detection and diagnostics primarily involves the AVI, BUB, and STATUS pins. The AVI pin is connected to a 100pF decoupling capacitor to filter high-frequency noise and stabilize the pin voltage. The STATUS pin employs an open-drain output configuration, which facilitates wired-OR connection of status signals from multiple devices and enables convenient system monitoring of the chip's operational status. The BUB pin connects to the backup battery to sense its voltage and incorporates a 1µF capacitor, which serves to filter and stabilize the backup battery voltage. This design ensures that the chip can accurately detect the backup battery's voltage status and automatically switch to backup battery power supply when the primary battery fails, thereby guaranteeing uninterrupted system operation.

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3.2 Loop Compensation Optimization Design to Avoid Large Overshoot

Transient overshoot may trigger the system's standby threshold, as shown in Figure 3-2. When the output voltage exhibits an overshoot exceeding a specified threshold, the IC may misidentify this condition as meeting the standby criterion, inadvertently transitioning from boost mode to standby mode. Subsequently, in standby mode, the output voltage may decline, and upon dropping below a certain level, the IC re-enters boost mode, resulting in repeated mode oscillation between boost and standby modes. This continuous mode switching not only compromises system stability but also increases power consumption and noise, thereby degrading the power conversion efficiency of the supply.

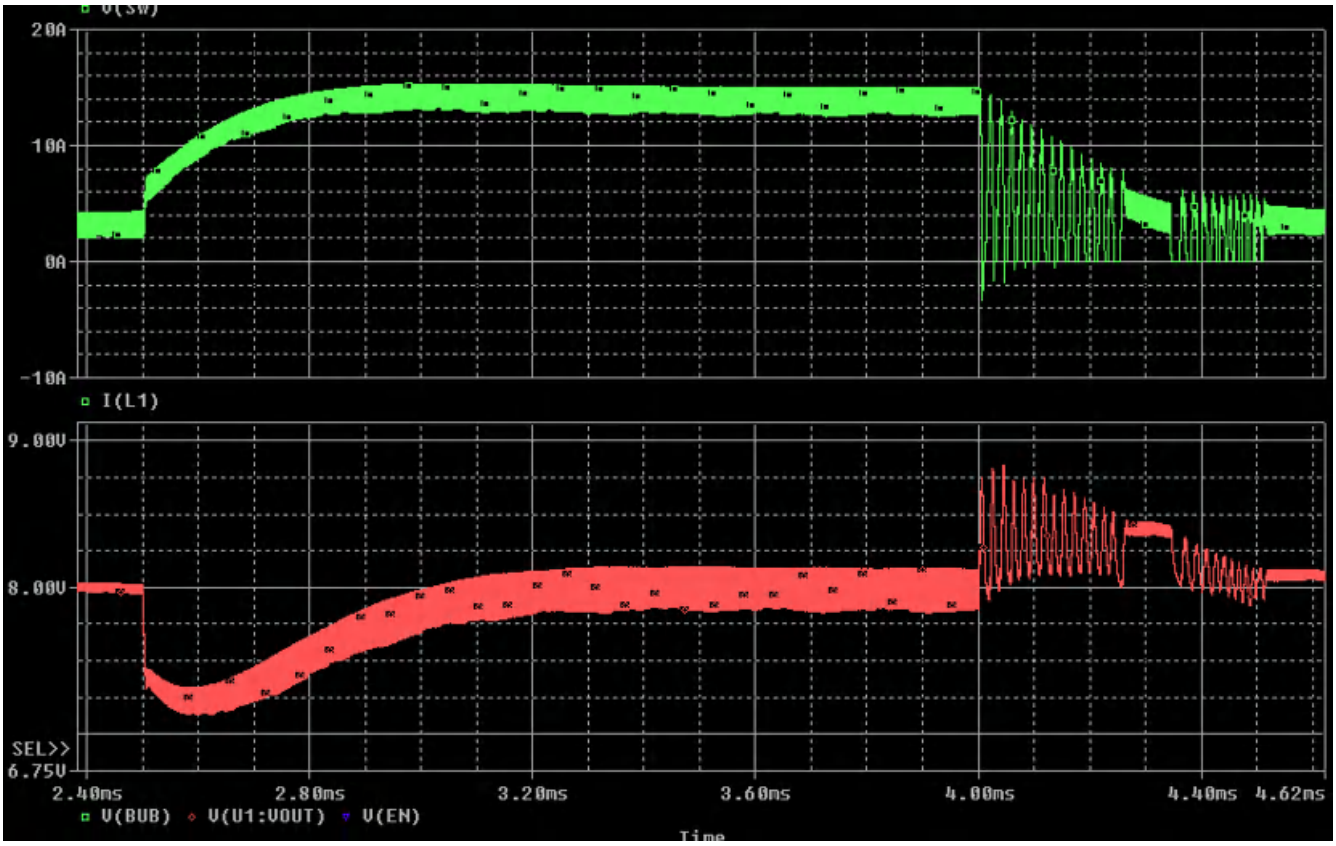


Figure 3-2. Bad Loop Compensation Cause Overshoot

In power supply design, the transfer function H(s) of the power stage is significantly affected by the equivalent series resistance (ESR) of the output capacitor. The impedance of the output capacitor can be expressed as $Z_C(s) = \frac{1}{sC} + R_{ESR}$, where $s = j\omega$ represents the complex frequency, C is the capacitance value, and R_{ESR} denotes the equivalent series resistance. At high frequencies where ω is large, the term $\frac{1}{sC}$ becomes negligibly small, such that $Z_C(s) \approx R_{ESR}$. Consequently, the ESR introduces a zero in the power stage transfer function at a frequency $\omega_Z = \frac{1}{R_{ESR}C_{OUT}}$. This zero induces a significant change in the system's phase margin. When R_{ESR} is relatively high, ω_Z decreases to a lower frequency. As illustrated in Figure 3-3, this implies that phase variation is introduced at low frequencies, thereby reducing the phase margin and potentially causing system instability phenomena such as oscillations.

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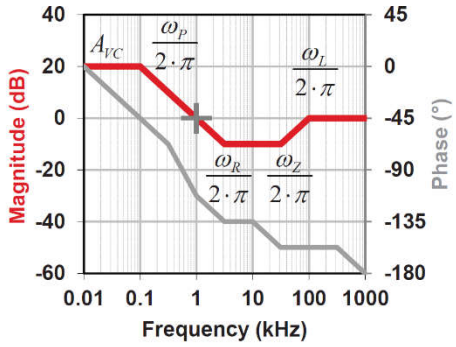


Figure 3-3. Pole-Zero of Power Stage

To mitigate transient overshoot, it is necessary to optimize the loop compensation design. The design objective is to ensure that the system maintains sufficient phase margin to preserve stability. Phase margin is defined as the difference between the phase of the open-loop transfer function at the gain crossover frequency (for example, the frequency where the gain equals 0 dB) and −180°. To compensate for the phase lag introduced by ESR, a compensation zero can be introduced by appropriately adjusting the compensation network. For instance, in the commonly employed Type II compensation network, the transfer function is expressed as $\frac{1+sR_2C_2}{sR_1\left(C_1\frac{1+R_2C_2}{sR_2C_1C_2}\right)}$, by judiciously selecting the values of R_1, R_2, C_1, and C_2, a high-frequency compensation zero $\omega_{HF}=\frac{1}{R_{COMP}C_{HF}}$ can be introduced to compensate for the phase variation caused by the ESR zero. This compensation mechanism effectively increases the phase margin and enhances the overall stability of the system.

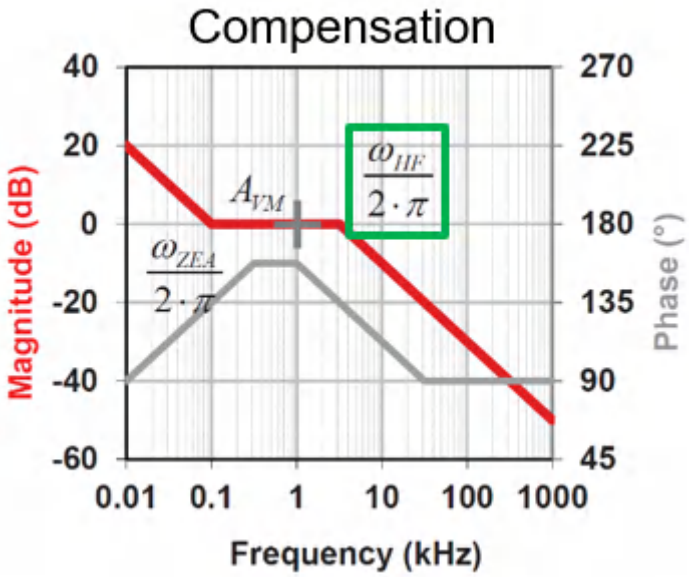


Figure 3-4. Pole-Zero of Compensation Circuit

3.3 TPS6138x-Q1 Layout Design Key Points

Regarding the layout of the driver circuit, as illustrated in Figure 3-5, when the IC enables the MOSFET, current flows from the VCC capacitor through the internal driver and gate resistor to charge the MOSFET's gate terminal. The return current flows from the MOSFET's source (PGND) through the circuit network back to the VCC capacitor's AGND. This current transient occurs within several nanoseconds with peak values reaching 2A. Consequently, judicious layout design that minimizes the current path length is of paramount importance to reduce loop inductance. Simultaneously, careful attention must be paid to the connection topology of PGND and AGND to ensure that the return current flows smoothly back to the VCC capacitor's AGND, avoiding excessive

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ground loops or multiple ground return paths. This prevents noise interference from ground potential differences, which could otherwise degrade the MOSFET's switching speed and efficiency as well as compromise the electromagnetic compatibility (EMC) of the entire circuit.

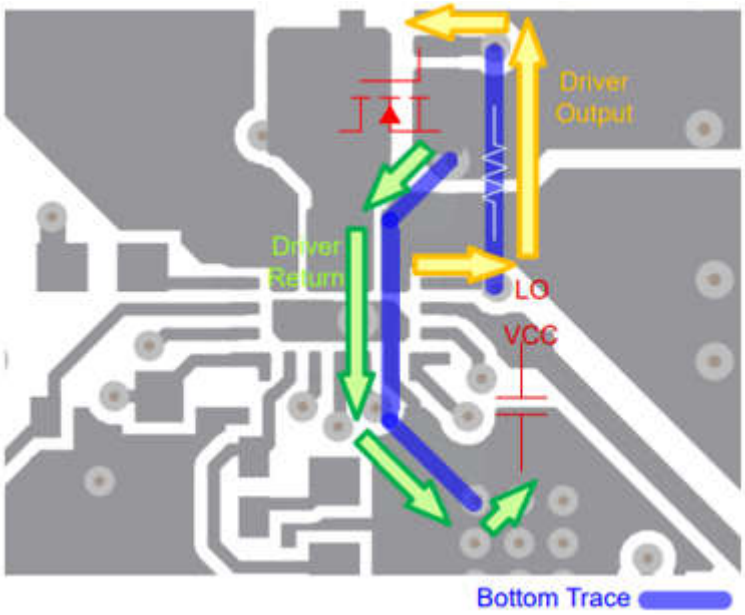


Figure 3-5. Driver Loop Layout

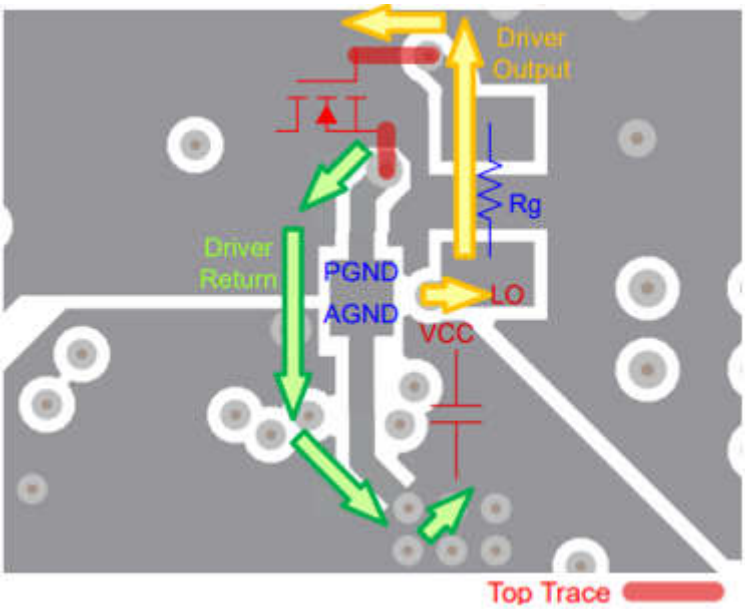


Figure 3-6. Title Here

The boost circuit layout also imposes stringent requirements, as shown in Figure 3-7. The boost current does not flow through the IC's GND pin or thermal pad. To minimize the current path length, multilayer ceramic capacitors (MLCCs) should be placed as close as possible to the VOUT pin (within 1 mm). The low-side MOSFET Q1 must also be positioned as proximate as possible to the SW pin. Additionally, it is recommended to place relatively small-value output capacitors (100 nF – 1 µF, 0603 package) near the VOUT pin to bypass high-frequency noise.

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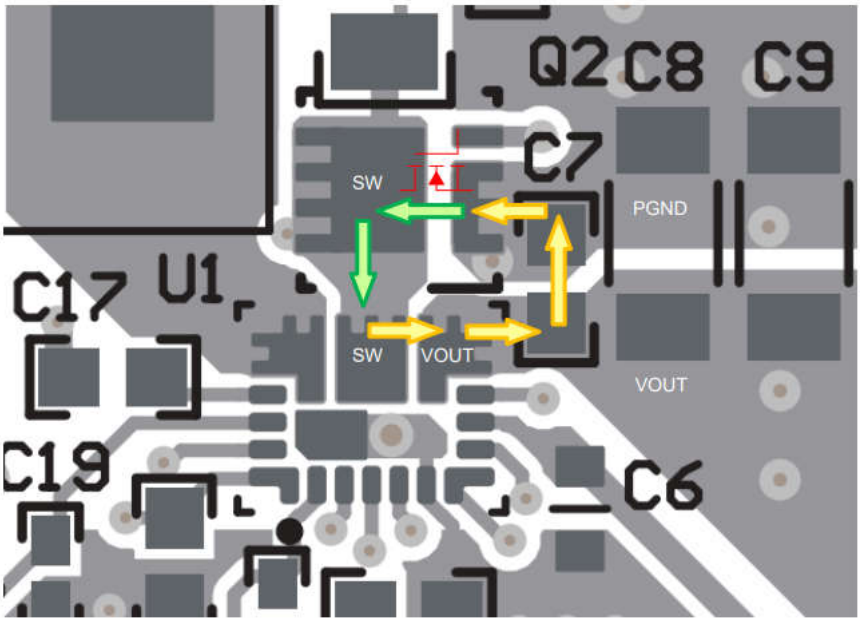


Figure 3-7. Boost Loop Layout

Figure 3-8 presents test results demonstrating noise coupling into the chip, wherein PGND noise is capacitively coupled to the control ground (AGND) through the thermal pad, affecting the bandgap reference voltage and subsequently degrading IC performance. The layout-level solution is to connect the thermal pad directly to AGND, thereby eliminating the readily conductive noise coupling path between PGND and the control ground AGND through the thermal pad.

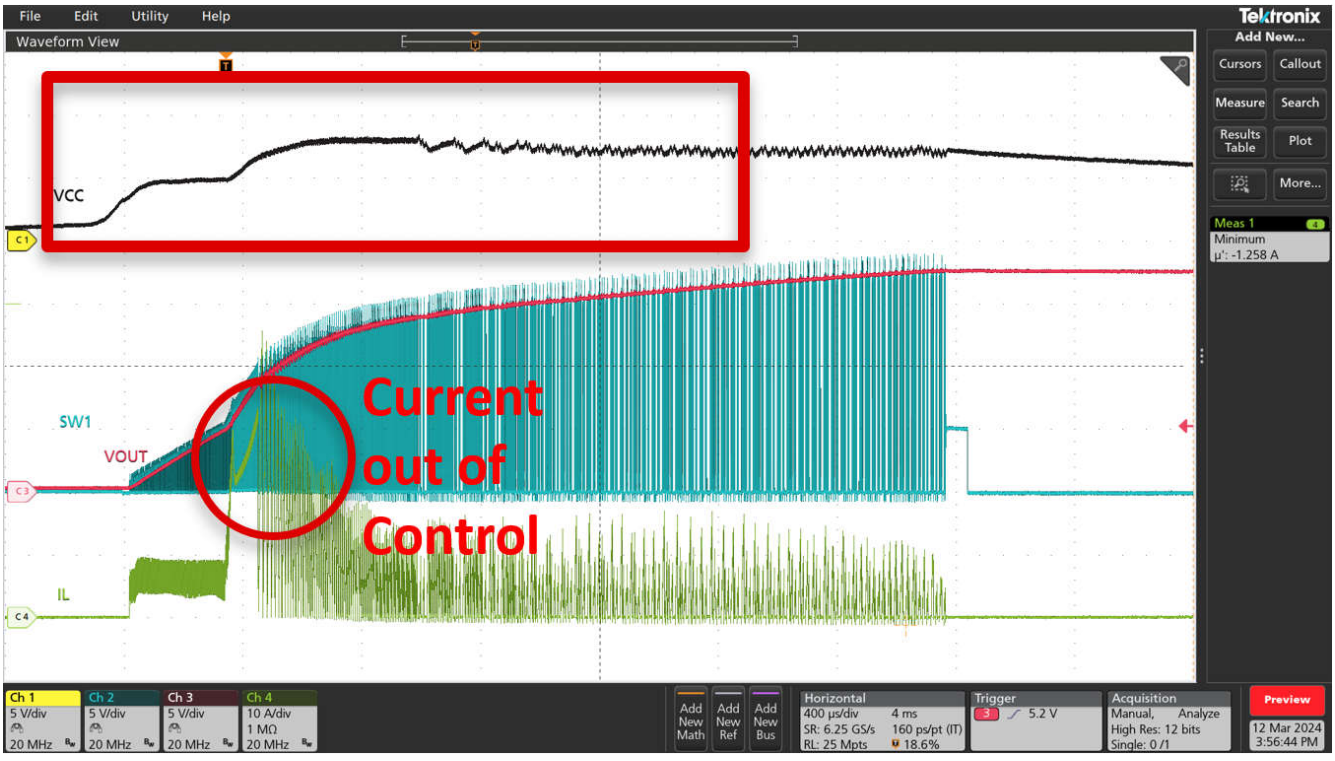


Figure 3-8. Noise Coupled Waveform

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4 Summary

As the T-BOX (telematics box) system is progressively integrated into intelligent cabin architectures, the backup battery management solution has undergone an evolutionary transition from a discrete architecture of discrete 'component stacking' toward a 'functional integration' paradigm. Texas Instruments' next-generation TPS6138x-Q1 series devices, built upon the foundation of addressing critical technical challenges including high-ESR capacitor stability, driver loop electromagnetic interference (EMI), and multilayer isolated grounding architecture, achieves remarkable optimization with a 20% reduction in bill of materials (BOM) cost and 30% reduction in printed circuit board (PCB) area. Concurrently, the device ensures ultra-fast 20 µs startup capability and multi-level reliability protection mechanisms, thereby providing a comprehensive and systematic engineering solution for backup power management integrated circuits in modern automotive applications.

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Texas Instruments, Automotive E-Latch Systems Design Guideline Using TPS61383

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