Application Note

Achieving Low Jitter With LMX2581 for GHz Clocking in Data Center Applications

Zach Xia, China DCP Team

Abstract

LMX2581 is a wideband frequency synthesizer, which can generate clocking signal up to 3.76GHz. In today's data center system, high-performance central processing units (CPU) and graphics processing units (GPU) running at several Gigahertz is common. At the same time, the jitter of the GHz clocking signal is critical for the stable operation of the CPU and GPU and maximize efficiency. When designing with clock generators like LMX2581 for data center applications, multiple careful considerations are needed to achieve the optimized jitter performance. This paper demonstrates the relationships between the significant factors through example schematic designs and board test results.

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1 Introduction

The key function block of the frequency synthesizer (or clock generator) is the phase locked loop (PLL). Figure 1-1 presents a simplified PLL structure, which is a reference-feedback-based close loop.

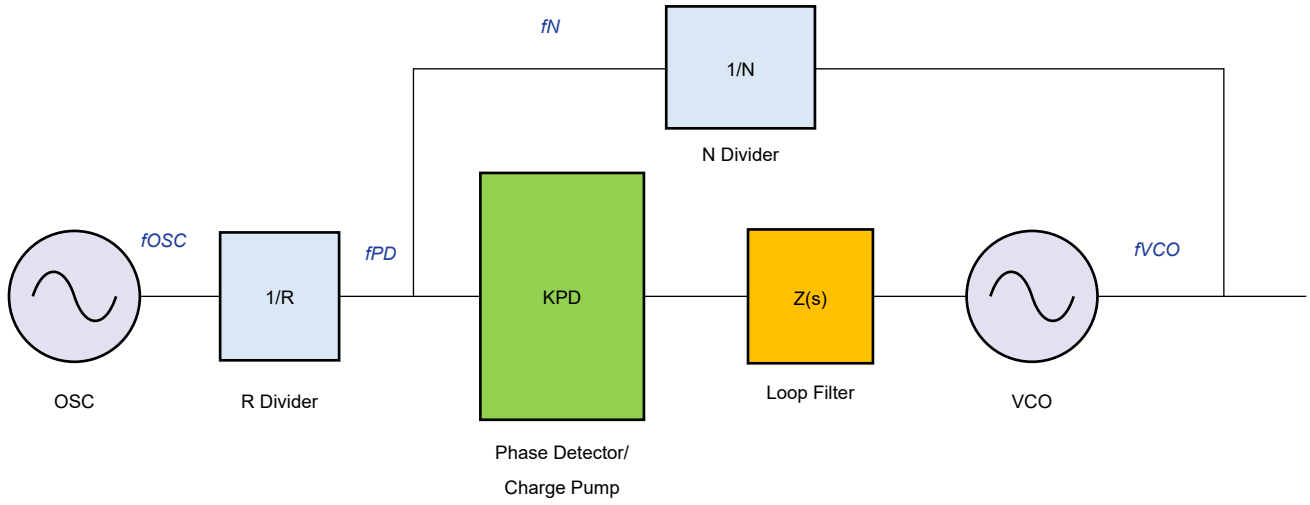


Figure 1-1. PLL Structure

Equation 1 calculates the target output frequency. However, optimizing the jitter requires multiple considerations.

$$f_{OUT} = \frac{f_{VCO}}{D} = \frac{N}{R \cdot D} \times f_{osc} \quad (1)$$

Clock jitter is an integration of phase noise in the frequency domain with a specified low and high frequency offset limit (like 12kHz-20MHz). Figure 1-2 demonstrates the dominance portion of phase noise across frequency. The PLL noise (phase detector noise, N divider noise) and VCO noise play key roles in the 12kHz-20MHz range.

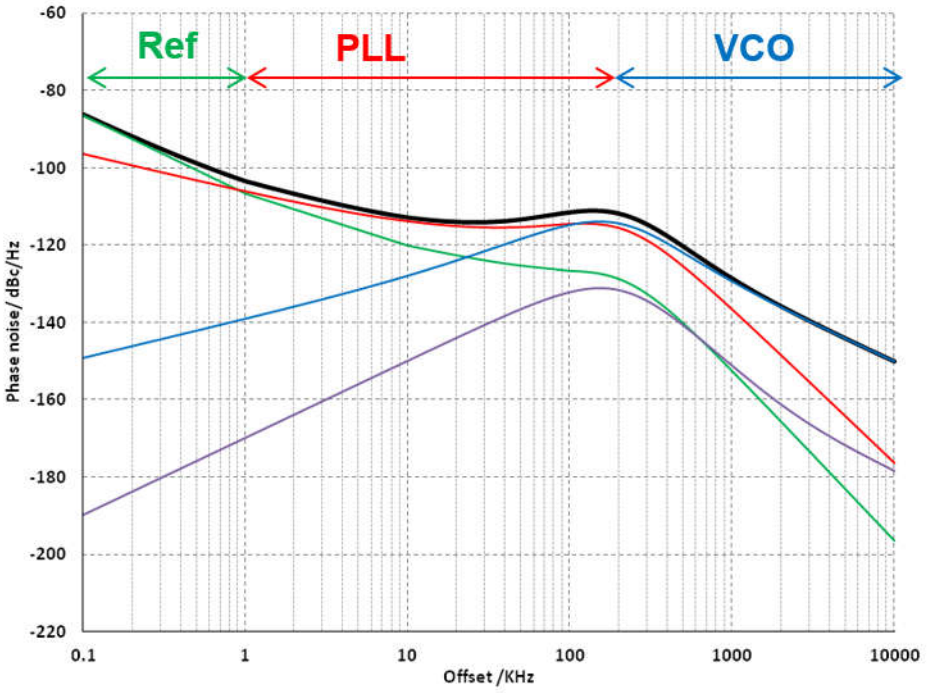


Figure 1-2. Phase Noise Curve

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Figure 1-3 shows the simplified internal blocks of the LMX2581 and external components. Multiple Core VCO are integrated, and the loop filter needs to be implemented externally. To optimize the jitter, make an effort to tune the loop filter components and configure the dividers, charging pump gain, and other components.

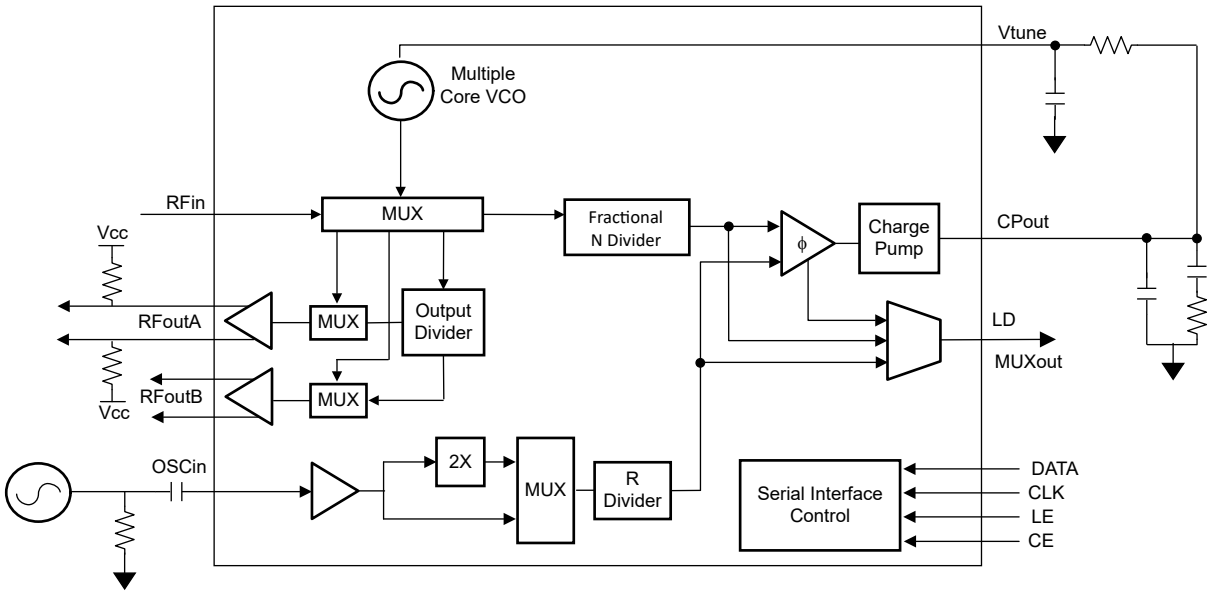


Figure 1-3. LMX2581 Simplified Schematic

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2 Hardware Design

Good schematic and layout are basis for better jitter performance, which happens before the loop filter component selection. In addition to the recommendations in the datasheet, other design practices include:

1. Use high PSRR and low noise LDO to power the LMX2581 and the XO which provides the input reference clock. In this case, TPS7A84 is used. When a single regulator is used, isolating different supply pins by adding ferrite bead and capacitor on each supply pin can be helpful.
2. Preserve at least 3rd-order loop filter like Figure 2-1. The filter can be degraded to a 2nd-order loop filter by removing C3_LF and short R3_LF.

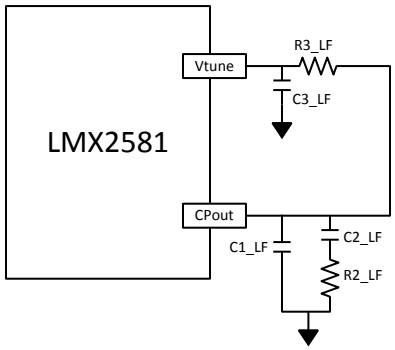


Figure 2-1. Typical Loop Filter

3. Place the C3_LF close to the Vtune pin on the same side of the device. The charge pump output and Vtune input are on opposite sides of the chip. In compact designs like a GPU card, the wire connection routes through internal layers then back to the surface. A close capacitor to the Vtune pin lowers the VCO noise. In 2nd-order filter design, the capacitance for C1_LF can be distributed between the normal spot and the spot of C3_LF. This arrangement can yield better performance as the footprint on the PCB for C3_LF is much closer to the VCO than the footprint for C1_LF.

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3 Loop Filter Components Selection

3.1 Design Example

The target output frequency (F_{out}) is 3250MHz, and the design goal is to minimize the jitter. To avoid fractional spur and integer boundary spurs (IBS), F_{osc} needs to be the integral divisor of F_{out}. In most circumstances, having an output frequency has only positive offset, including F_{osc} deviation, temperature, and other factors, is preferred. Choose a F_{osc} which has a smaller deviation than the divisor. Thus, the 62.501562MHz value that is chosen though the divisor is 62.5MHz.

3.2 Simulation in TI PLLatinum Sim

To get good jitter results, the loop filter RC components value cannot be chosen randomly. While calculation in theory requires fluent mathematical techniques, to try different RC value combinations on the real board takes more time and provides only limited indication. To aid the loop filter design, TI's PLLatinum™ Sim is a simulation software which simplifies the calculation process and only requires a few specification details. Figure 3-1 shows the user interface and some of the parameters.

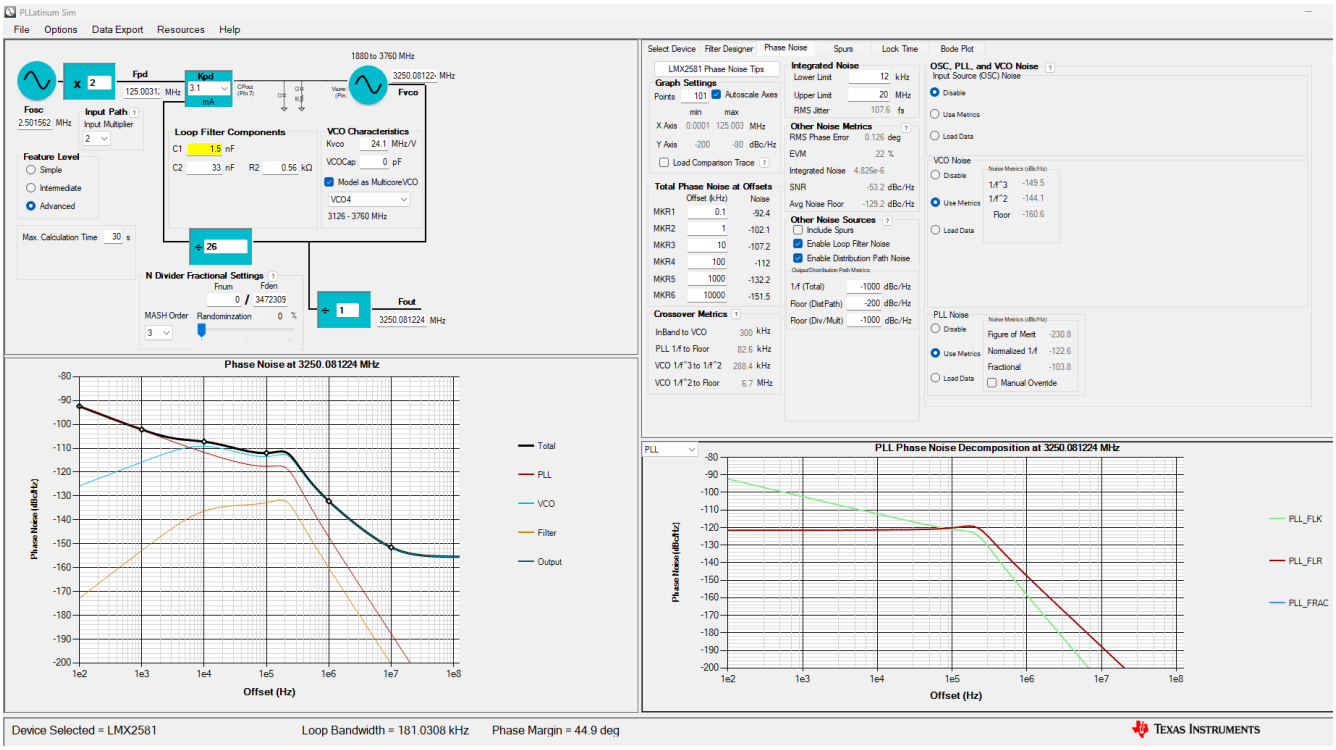


Figure 3-1. LMX2581 Page in TI PLLatinum Sim

When the integral feedback divisor is used, the 2nd-order filter can provide jitter result as good as 119fs. Further decreasing the C1 in the simulation results in lower RMS jitter. However, there is a note in the "LMX2581 Phase Noise Tips". This device has a minimum high order capacitance. What this means is that if the capacitor closest to the VCO is too small, there can be phase noise degradation in the 200kHz to 1MHz range. If this value is 3.3nF or larger, there is no degradation. If the value is 1.5nF, the degradation can be a few dB. Using a value less than 3.3nF can make sense if this requirement restricts the loop bandwidth, but using a value less than 1.5nF is not recommended.

This VCO phase noise degradation is mentioned in the *External Loop Filter* section of the datasheet as well, but not included in the simulation by "Use Metrics".

Change the Filter Order to 3rd Order and Auto Parameter Strategy to Optimize Jitter, and enter Min High Order Cap as 1500pF so that the VCO phase noise is not obviously degraded. Click "Calculate Loop Filter". The GUI calculates in backend and refreshes with the suggested results as shown in Figure 3-2.

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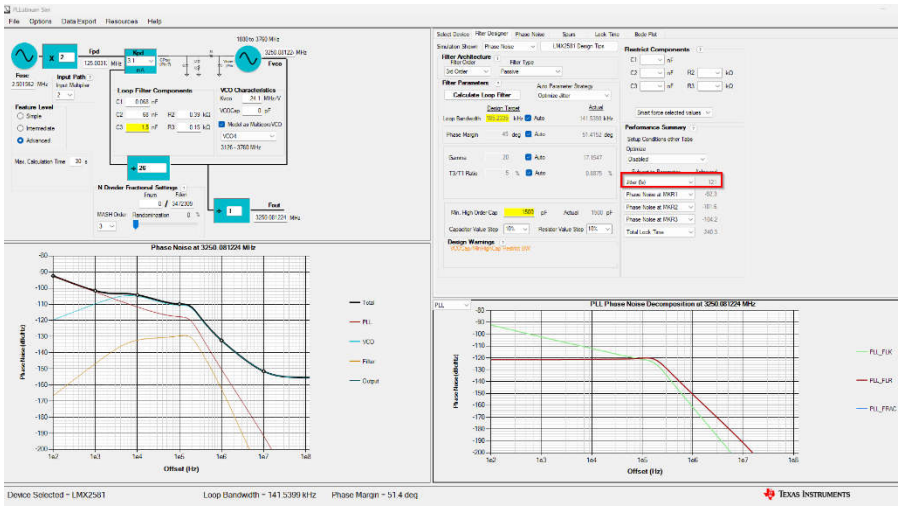


Figure 3-2. LMX2581 3rd Order Loop Filter Simulation

3.3 Test Verification

3.3.1 Setup

Typical test equipment for phase noise and jitter is Agilent E5052 and R&S FSPW. Figure 3-3 shows the preferred way to measure differential output phase noise for signals below 1GHz.

- Differential output: rejects common mode noise and provides a bigger signal swing.
- Balun: converts differential signals to single ended output to interface with the analyzer.
- AC-coupled, or so-called DC blocker: blocks any DC signal going into the equipment and prevents instrument damage. RF Instruments do not accept DC.

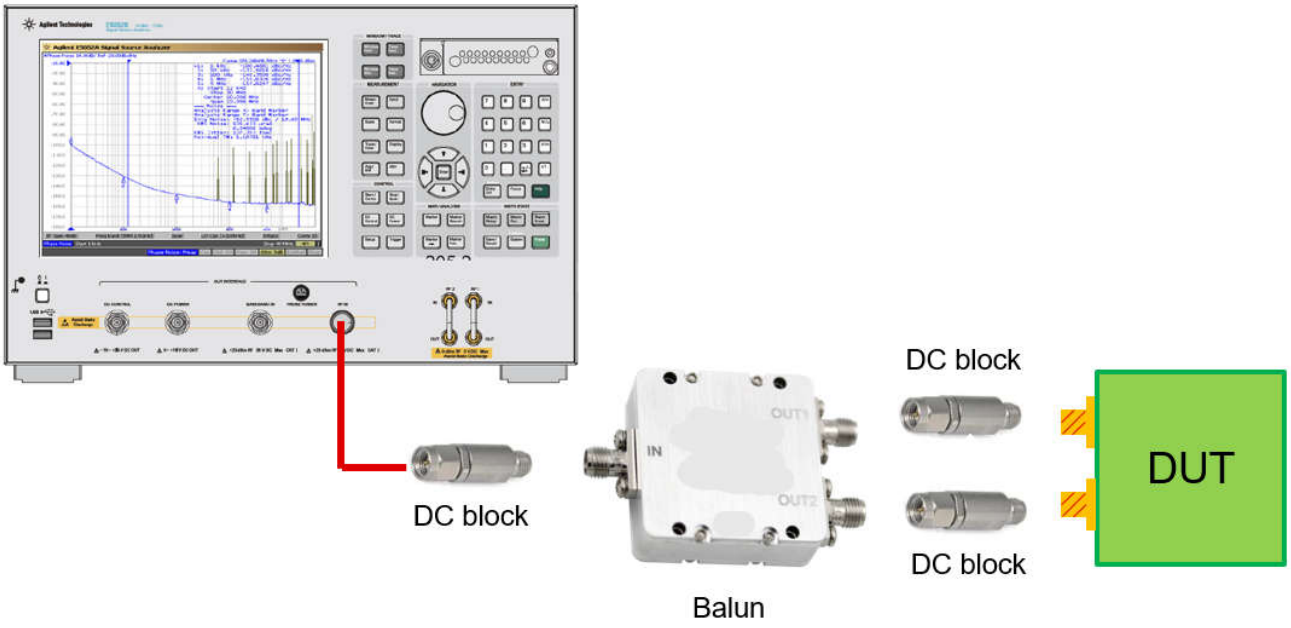


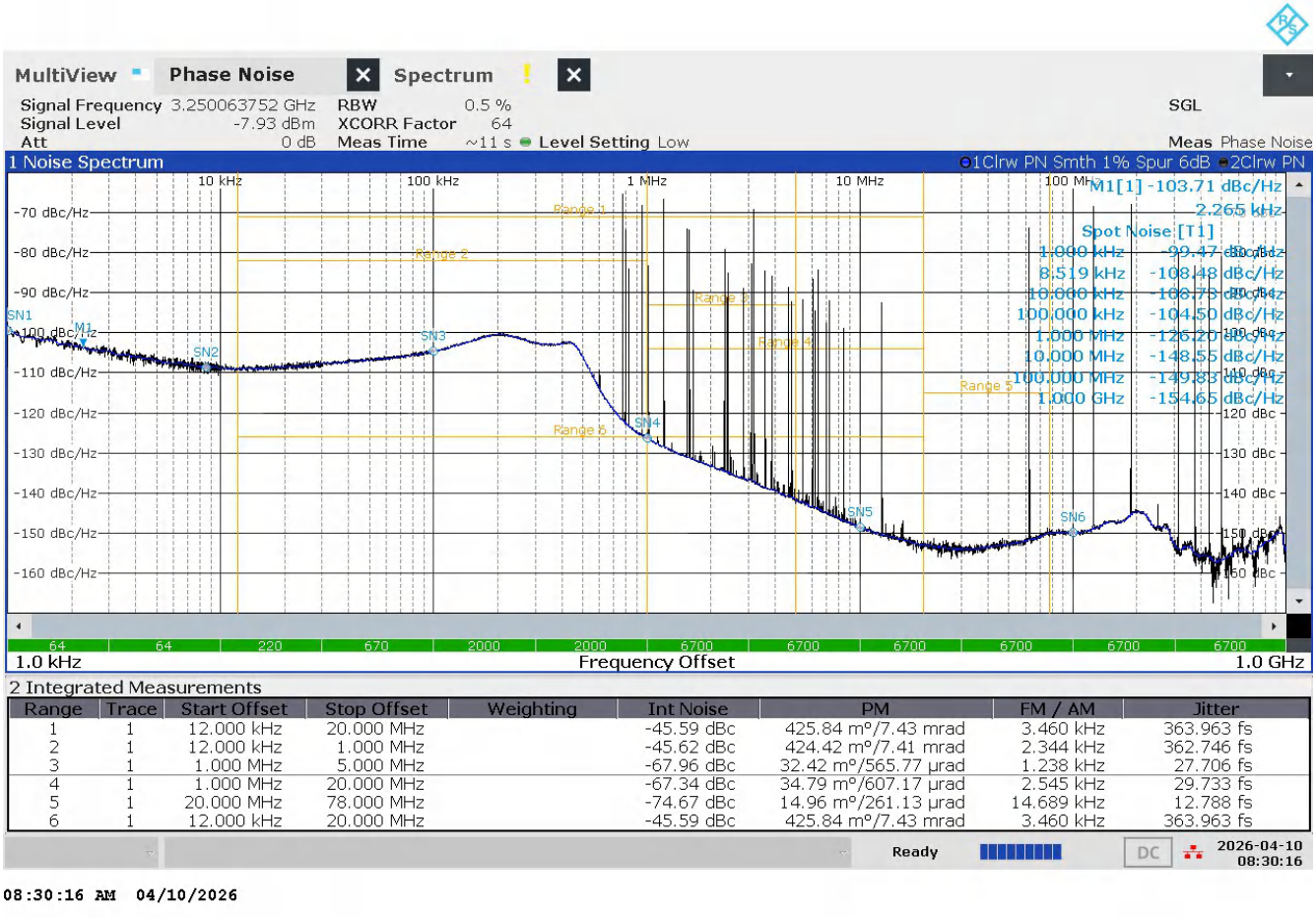
Figure 3-3. Differential Clocking Test Setup

However, for signals higher than 1GHz, balun is not required. Single-ended measurement is sufficient.

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3.3.2 Test Results

Figure 3-4 shows an example of a phase noise plot with an inappropriate loop filter. A 3rd order filter is used while a 100pF capacitor, which is far smaller than recommended, is placed near the Vtune pin C3. Therefore, the phase noise from 100kHz to 1MHz increases by approximately 10dBc, which leads to the RMS jitter (12kHz-20MHz) of 364fs.



Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	12.000 kHz	20.000 MHz		-45.59 dBc	425.84 m°/7.43 mrad	3.460 kHz	363.963 fs
2	1	12.000 kHz	1.000 MHz		-45.62 dBc	424.42 m°/7.41 mrad	2.344 kHz	362.746 fs
3	1	1.000 MHz	5.000 MHz		-67.96 dBc	32.42 m°/565.77 µrad	1.238 kHz	27.706 fs
4	1	1.000 MHz	20.000 MHz		-67.34 dBc	34.79 m°/607.17 µrad	2.545 kHz	29.733 fs
5	1	20.000 MHz	78.000 MHz		-74.67 dBc	14.96 m°/261.13 µrad	14.689 kHz	12.788 fs
6	1	12.000 kHz	20.000 MHz		-45.59 dBc	425.84 m°/7.43 mrad	3.460 kHz	363.963 fs

Figure 3-4. Phase Noise Plot With C3 = 100pF

Higher phase detector frequency and higher charge pump gain can reduce the jitter. This relationship is proven by adjusting the settings in TICS PRO. Loop filter components are C2 = 47nF, R2 = 357Ω, and C3 = 1.5nF (C1 is NC as C3 is close to Vtune pin). Table 3-1 shows the results of each test. Furthermore, the results indicate that the output power also influences the jitter performance, even though the output power needs to be selected based on the output swing and slew rate required by the receiver.

Table 3-1.

Test	Doubler	Kpd/uA	Output Pwr	Jitter/fs
1	2x	3100	25	137.4
2	1x	3100	25	188.7
3	2x	2500	25	151.1
4	2x	2100	25	168.6
5	2x	3100	30	137.7
6	2x	3100	20	139

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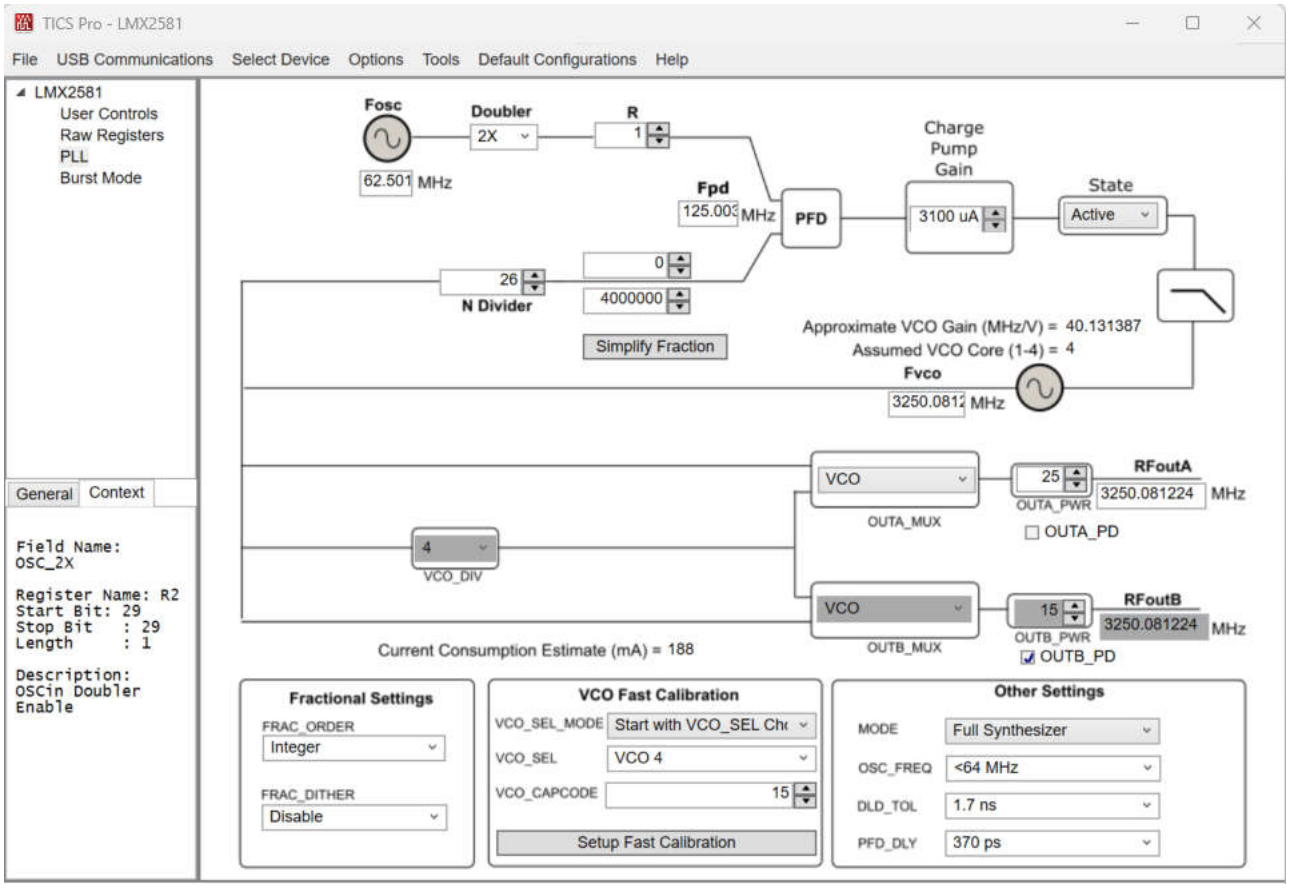


Figure 3-5. TICS PRO LMX2581 View

Different capacitance values for C2 and C3 have also been tried to figure out the best combinations. R2 is kept at 357Ohm for simplicity. The PLL setting is Doubler = 2x, Kpd = 3100uA, Output Pwr = 25. Along with the phase noise plot, the results prove that wider open loop bandwidth (smaller C3) helps suppress the VCO noise though the VCO phase noise can be slightly raised.

Test	C2/nF	C3/nF	Jitter/fs
1	47	3.3	159
2	47	2.2	147.8
3	47	1.5	137.4
4	15	1.5	143
5	68	1.5	138

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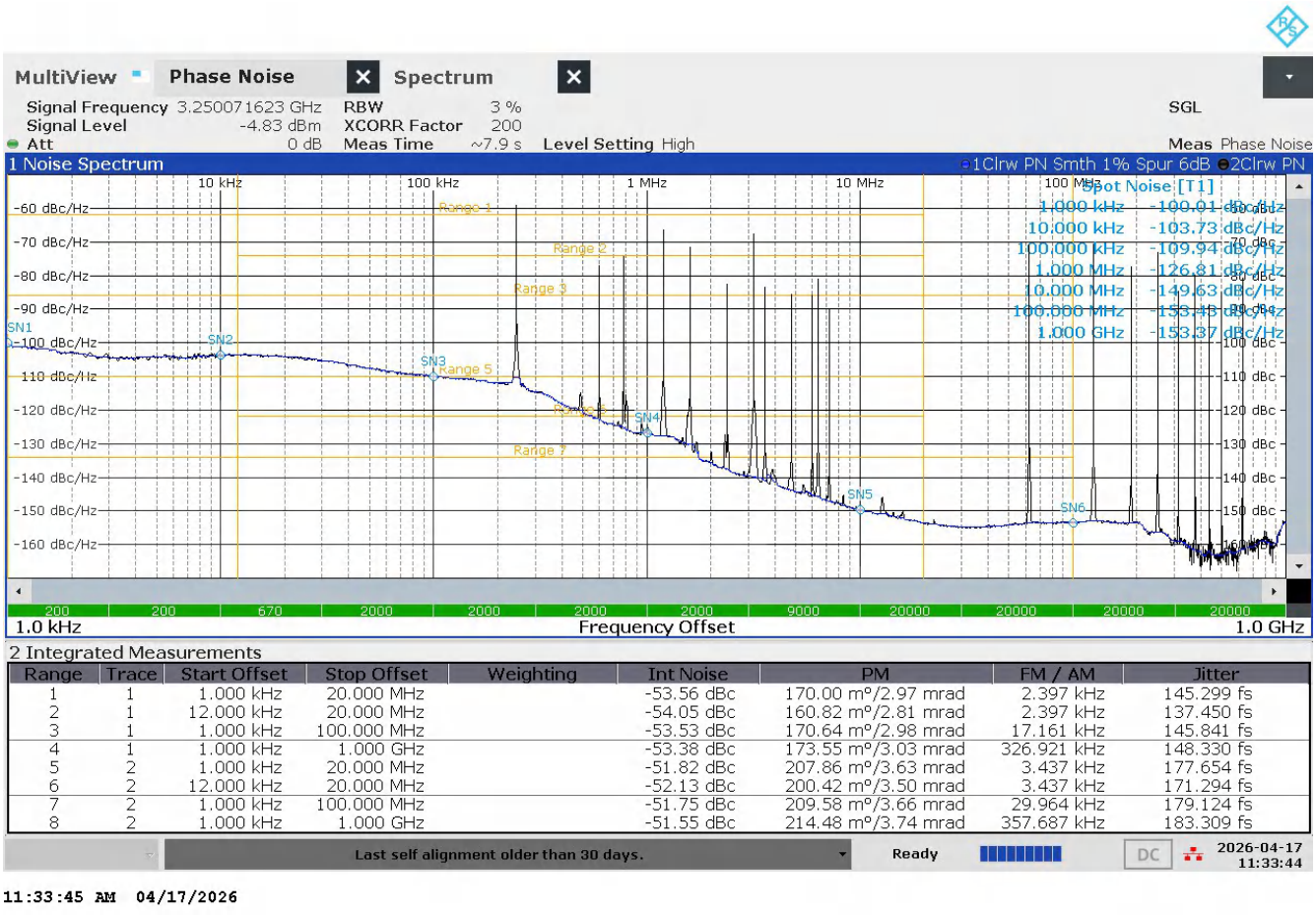


Figure 3-6. Phase Noise Plot With Optimized Loop Filter

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4 References

1. Texas Instruments, *LMX2581 Wideband Frequency Synthesizer with Integrated VCO* datasheet
2. Texas Instrument: *LMX2581EVM User's Guide*
3. Dean Banerjee (2017), *PLL Performance, Simulation, and Design*. Revision C, document number: SNAA106, request through a myTI™ account

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