

Functional Safety Information

LMR38015-Q1 and LMR38025-Q1

Functional Safety FIT Rate, FMD and Pin FMA



Table of Contents

1 Overview.....2

2 Functional Safety Failure In Time (FIT) Rates.....3

3 Failure Mode Distribution (FMD).....4

4 Pin Failure Mode Analysis (Pin FMA).....5

5 Revision History.....7

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for LMR38015-Q1 and LMR38025-Q1 (WSO (12) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

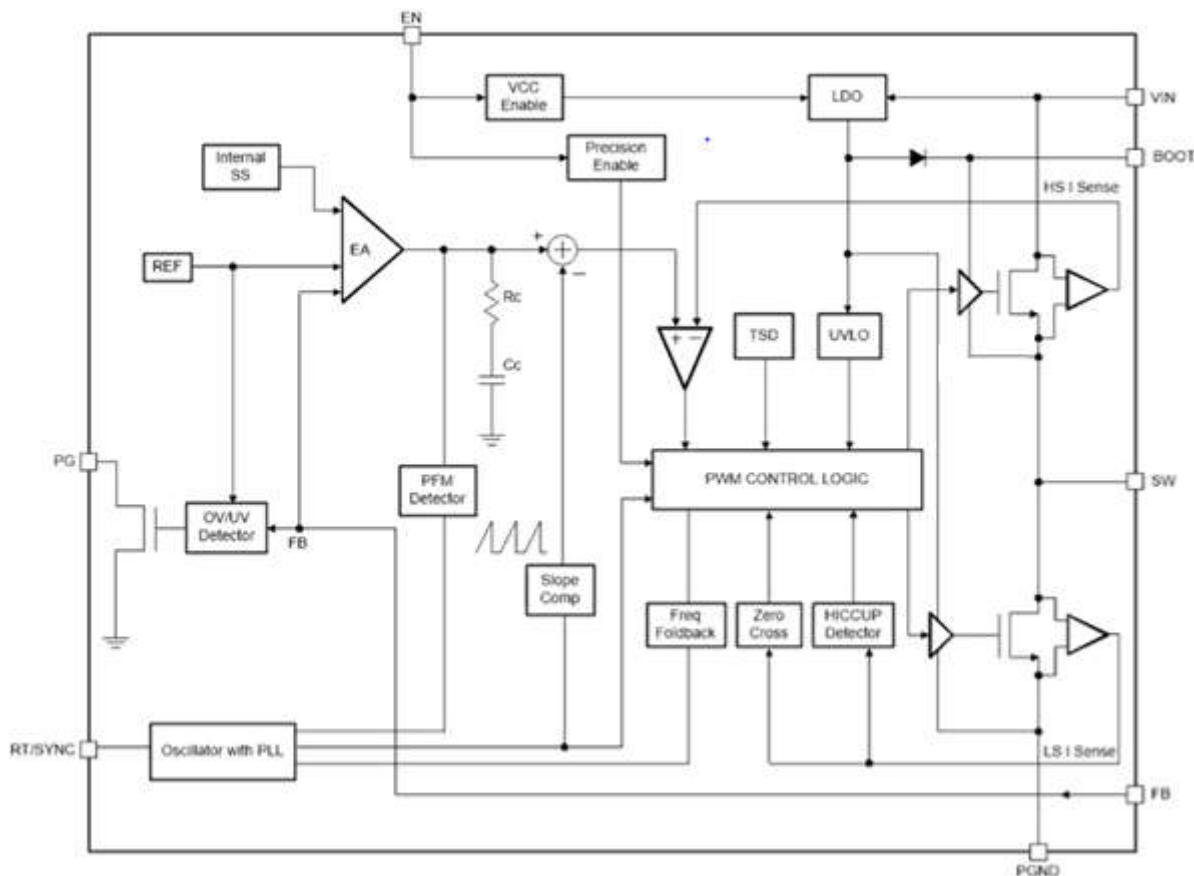


Figure 1-1. Functional Block Diagram

LMR38015-Q1 and LMR38025-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LMR38015-Q1 and LMR38025-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	10
Die FIT rate	5
Package FIT rate	5

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1000mW
- Climate type: World-wide table 8 or figure 13
- Package factor (λ_3): Table 17b or figure 15
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS ASICs analog and mixed HV >50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR38015-Q1 and LMR38025-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No SW output	50
SW output higher in specification – voltage or timing	20
SW output lower in specification – voltage or timing	20
SW power FET stuck on	5
PGOOD false trip, fails to trip	5

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMR38015-Q1 and LMR38025-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the LMR38015-Q1 and LMR38025-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMR38015-Q1 and LMR38025-Q1 datasheet.

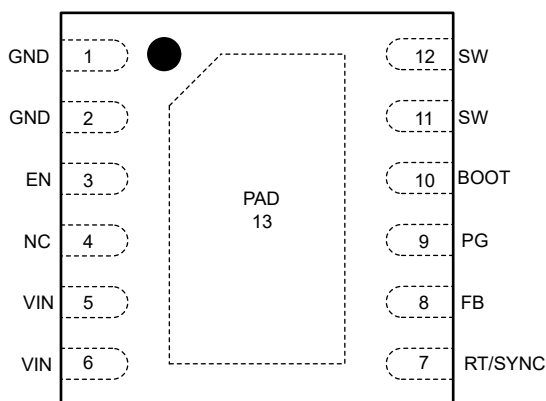


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the LMR38015-Q1 and LMR38025-Q1 datasheet

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
GND	1	The device operated as normal.	D
	2		
EN	3	VOUT = 0V.	B
VIN	5	VOUT = 0V.	B
	6		
RT/ SYNC	7	Switching frequency is greater than 3MHz.	C
FB	8	VOUT is greater than the programmed output voltage.	B
PG	9	There is no power good function.	B
BOOT	10	VOUT = 0V.	B
SW	11	There is damage to the high-side (HS) FET.	A
	12		

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
GND	1	VOUT is potentially abnormal due to switching noise on the analog circuits.	B
	2		
EN	3	The device can shut off.	B
VIN	5	The device can shut off.	B
	6		
RT/ SYNC	7	There is no Switching frequency.	B
FB	8	VOUT is greater than the programmed output voltage.	B
PG	9	There is no power good function.	B
BST	10	VOUT = 0V.	B
SW	11	VOUT = 0V.	B
	12		

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name 1	Pin Name 2	Description of Potential Failure Effects	Failure Effect Class
GND	EN	VOUT = 0V.	B
EN	VIN	VOUT operates as normal.	B
FB	PG	VOUT is less than the programmed output voltage.	B
PG	BOOT	The PG pin has ESD damage if the voltage of the BOOT pin is greater than 20V.	A
BOOT	SW	VOUT = 0V.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
GND	1	VOUT = 0V. Damage to other pins is referred to GND.	A
	2		
EN	3	The device is enabled.	D
VIN	5	The pin is in normal mode.	D
	6		

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
RT/ SYNC	7	There is ESD damage to the RT/SYNC pin if VIN > 5.5V.	A
FB	8	If VIN exceeds 5.5V, damage to the device occurs. VOUT = 0V.	A
PG	9	There is ESD damage to the PG pin if VIN > 20V.	B
BOOT	10	VOUT = 0V. The CBOOT ESD clamp runs the current to destruction.	A
SW	11	There is damage to the low-side (LS) FET.	A
	12		

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 6, 2023 to September 28, 2026 (from Revision * (November 2023) to Revision A (September 2026))

Page

- Updated the *Die Failure Modes and Distribution Table*..... 4

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025