Functional Safety Information

LMR38015 and LMR38025 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LMR38015 and LMR38025 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

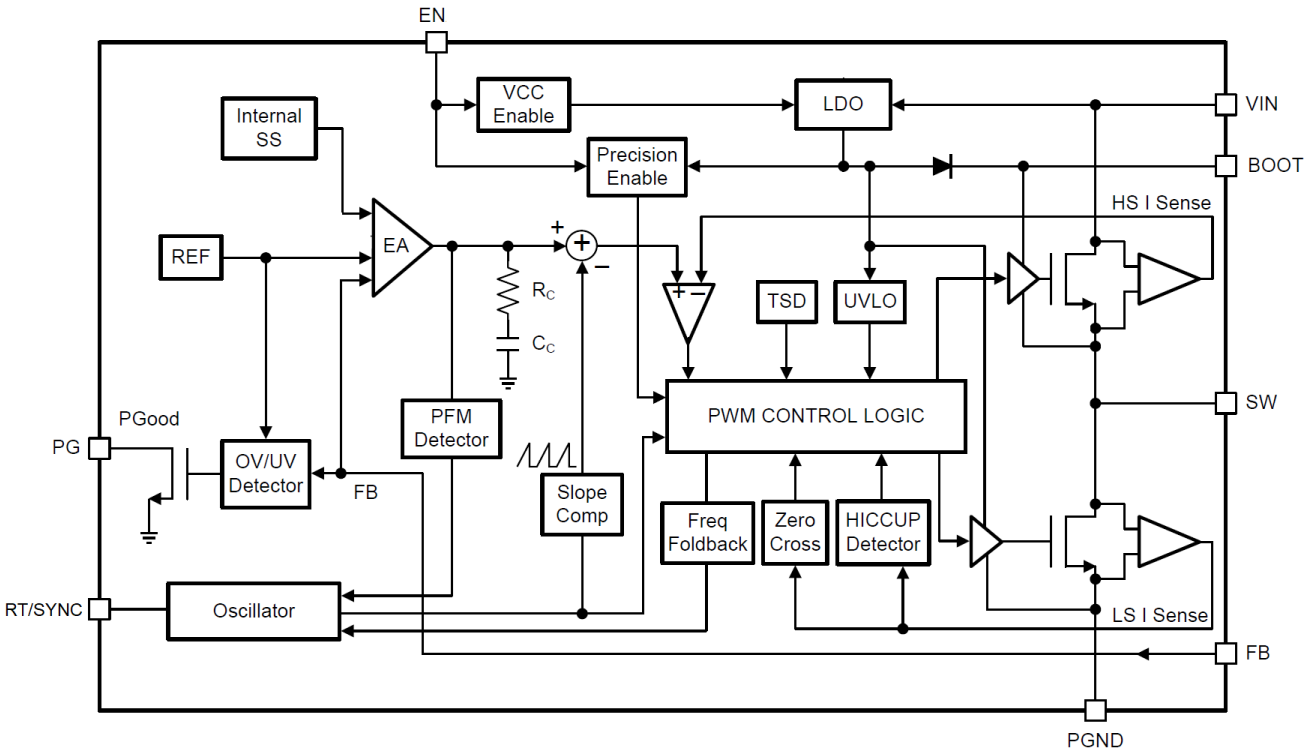

Figure 1-1. Functional Block Diagram

LMR38015 and LMR38025 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LMR38015 and LMR38025 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10
Die FIT rate	5
Package FIT rate	5

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1000mW
- Climate type: World-wide Table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed HV > 50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR38015 and LMR38025 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No SW output	50
SW output higher in specification – voltage or timing	20
SW output lower in specification – voltage or timing	20
SW power FET stuck on	5
PGOOD false trip, fails to trip	5

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMR38015 and LMR38025. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LMR38015 and LMR38025 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMR38015 and LMR38025 datasheet.

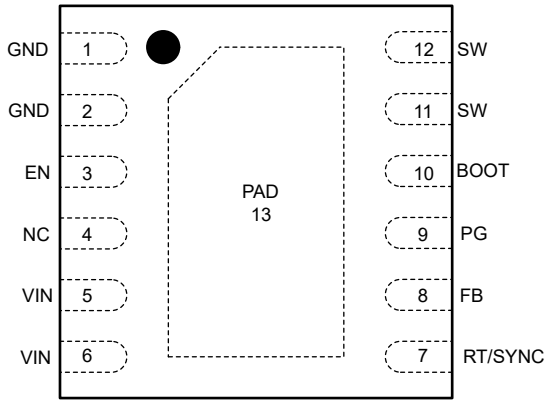

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the LMR38015 and LMR38025 datasheet

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
GND	1	The device operates as normal.	D
	2		
EN	3	VOUT = 0V.	B
VIN	5	VOUT = 0V.	B
	6		
RT/SYNC	7	The switching frequency is greater than 3MHz.	C
FB	8	VOUT is greater than the programmed output voltage.	B
PG	9	There is no power good (PG) function.	B
BOOT	10	VOUT = 0V.	B
SW	11	There is damage to the high-side (HS) FET.	A
	12		

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
GND	1	VOUT can be abnormal due to switching noise on analog circuits.	B
	2		
EN	3	The device can shut off.	B
VIN	5	The device can shut off.	B
	6		
RT/SYNC	7	There is no switching frequency.	B
FB	8	VOUT is greater than the programmed output voltage.	B
PG	9	There is no power good function.	B
BST	10	VOUT = 0V.	B
SW	11	VOUT = 0V.	B
	12		

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	EN	VOUT = 0V.	B
	2			
EN	3	VIN	The VOUT operation is normal.	B
FB	8	PG	VOUT is less than the programmed output voltage.	B
PG	9	BOOT	There is ESD damage to the PG pin if the voltage of the BOOT pin > 20V.	A
BOOT	10	SW	VOUT = 0V.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
GND	1	VOUT = 0V. There is damage to other pins that are referred to GND.	A
	2		
EN	3	The device is enabled.	D
VIN	5	Normal mode.	D
	6		

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
RT/ SYNC	7	There is ESD damage to the RT/SYNC pin if the voltage of VIN > 5.5V.	A
FB	8	If VIN exceeds 5.5V, damage occurs. VOUT = 0V.	A
PG	9	There is ESD damage to the PG pin if the voltage of VIN > 20V.	B
BOOT	10	VOUT = 0V. The CBOOT ESD clamp runs current to destruction.	A
SW	11	Therese is damage to the low-side (LS) FET.	A
	12		

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 7, 2024 to August 10, 2026 (from Revision * (February 2024) to Revision A (August 2026)) **Page**

- Updated the *Die Failure Modes and Distribution* table....4

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