

Functional Safety Information

TPS4816x-Q1

Functional Safety FIT Rate, FMD and Pin FMA



Table of Contents

1 Overview.....2

2 Functional Safety Failure In Time (FIT) Rates.....3

3 Failure Mode Distribution (FMD).....4

4 Pin Failure Mode Analysis (Pin FMA).....5

5 Revision History.....9

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1 Overview

This document contains information for TPS4816x-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

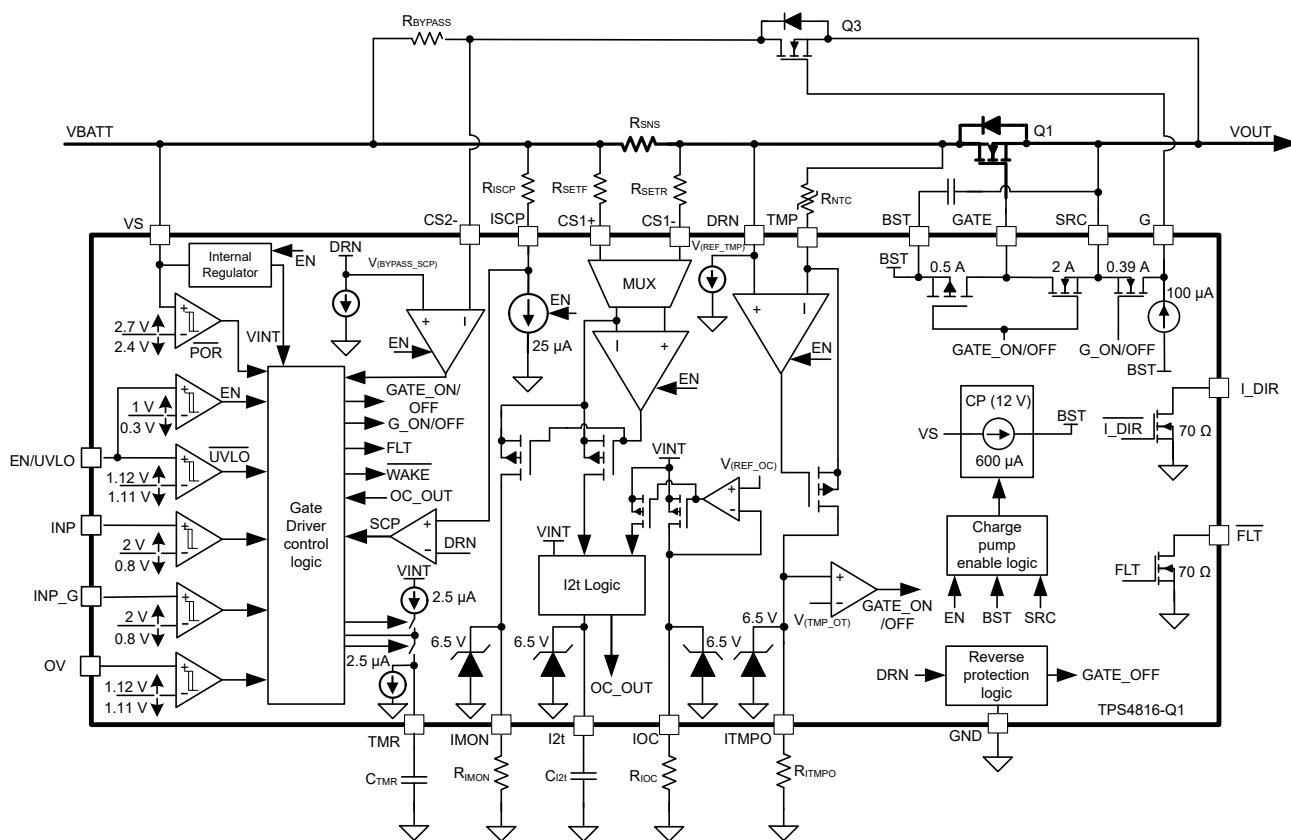


Figure 1-1. Functional Block Diagram

TPS4816x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS4816x-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	12
Die FIT rate	3
Package FIT rate	6

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 27mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS4816x-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Gate output stuck high	19
Gate output stuck low	34
Gate output functional, not in specification voltage or timing	27
Short circuit protection fails to trip or false trip	2
I _{2t} protection fails to trip or false trip	6
IMON not in specification – current or timing	3
ITMPO not in specification	4
Pin to pin short any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS4816x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the TPS4816x-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS4816x-Q1 datasheet.

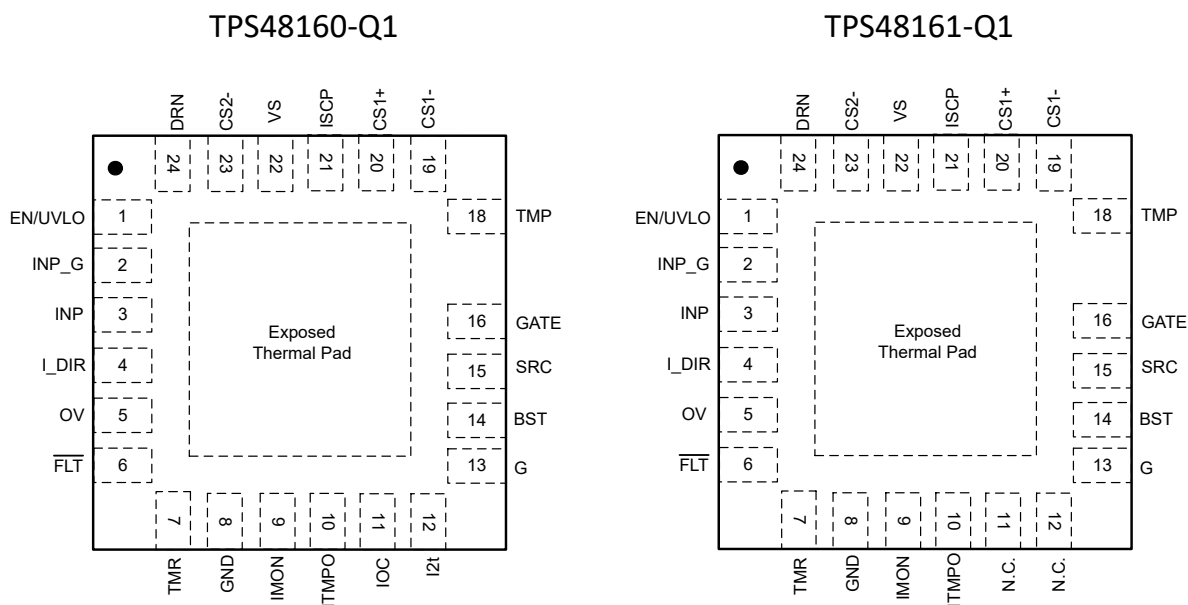


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follows the datasheet recommendations for operating conditions, external component selection, and PCB layout

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	The device operates normally. The device is disabled.	B
INP_G	2	The device operates normally. The G output is pulled to SRC and the bypass FET is off.	B
INP	3	The device operates normally. The GATE output is pulled to SRC and the main FET is off.	B
I_DIR	4	Current is limited by the external pullup resistor on the I_DIR pin. The functionality of the I_DIR pin is not available.	B
OV	5	Overvoltage protection is disabled. The device operates normally.	B
FLT	6	The I2t based overcurrent, short-circuit, and charge pump UVLO fault diagnostic cannot be reported.	D
TMR	7	The device is in latch off mode.	B
GND	8	The device operates normally.	D
IMON	9	IMON information is not available.	B
ITMPO	10	ITMPO information is not available.	B
IOC	11	I2t based overcurrent protection is not be available.	B
I2t	12	I2t based overcurrent protection is disabled.	B
G	13	With G grounded, if the pin voltage between SRC and G exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
BST	14	The gate driver supply does not come up. The gate drives (GATE and G) remain OFF.	B
SRC	15	The output short to GND protection begins.	B
GATE	16	With GATE grounded, if the pin voltage between SRC and GATE exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
TMP	18	With TMP grounded, if the pin voltage between TMP and SRC exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
CS1-	19	With CS1- grounded, if the pin voltage between CS1+ and CS1- exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
CS1+	20	With CS1+ grounded, if the pin voltage between CS1+ and CS1- exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
ISCP	21	With ISCP grounded, if the pin voltage between ISCP and CS1- exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
VS	22	The supply of the device is grounded. The device does not power up. With VS grounded, if the pin voltage between VS and SRC exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
CS2-	23	A false load wake up triggers.	B
DRN	24	With DRN grounded, if the pin voltage between DRN and SRC exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	Internal pulldown brings EN/UVLO to low, disabling the device.	B
INP_G	2	Internal pulldown brings INP_G to low, pulling G output low.	B
INP	3	Internal pulldown brings INP to low, pulling GATE output low.	B
I_DIR	4	I_DIR functionality is not be available.	B
OV	5	Internal pulldown brings OV to disabling overvoltage protection.	B
FLT	6	I2t based overcurrent, short-circuit, and charge pump UVLO fault diagnostic cannot be reported.	B
TMR	7	The device goes to automatic retry mode after an overcurrent fault, with the minimum automatic retry time based on the parasitic capacitor on the TMR pin.	B
GND	8	The device does not power up and is disabled.	B
IMON	9	I2t based overcurrent protection is disabled.	B
ITMPO	10	The device operates normally.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IOC	11	The minimum I2t start threshold OCP threshold is set. I2t based overcurrent protection is incorrect. The device powers up but the main path (GATE) turns OFF based on the C_{I2t} .	B
I2t	12	I2t based overcurrent protection is incorrect.	B
G	13	The G output is not controlled. The bypass path remains OFF.	B
BST	14	The external FET is turned ON and OFF repetitively due to no capacitor connection at the BST pin.	B
SRC	15	The external FET does not turn OFF as the FET source disconnects from the internal pulldown driver.	B
GATE	16	The external FET does not turn OFF as the FET GATE disconnects from the internal pulldown driver.	B
TMP	18	ITMPO is unavailable.	B
CS1-	19	CS1- is internally clamped to CS1+ minus two diode drops. The device detects a false short-circuit fault. IMON and I2t protection are unavailable.	B
CS1+	20	The device detects a false short-circuit fault. IMON and I2t protection are unavailable.	B
ISCP	21	The short-circuit protection feature becomes disabled.	B
VS	22	The device does not power up and is disabled.	B
CS2-	23	The device detects a false load wake-up event.	B
DRN	24	The device is damaged.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	2 (INP_G)	When EN/UVLO is driven high, then based on the EN/UVLO level, INP_G can get detected high and G can go high turning ON the external bypass FET.	B
INP_G	2	3 (INP)	Both the gate drive GATE and G are pulled high and low together.	B
INP	3	4 (I_DIR)	The functionality of I_DIR is not available.	B
I_DIR	4	5 (OV)	If I_DIR is high, then OV is pulled high, pulling both gate drives GATE and G low. If I_DIR is pulled low, then overvoltage protection is disabled.	B
OV	5	6 (FLT)	If FLT is high, then OV is pulled high, pulling both gate drives GATE and G low. If FLT is pulled low then overvoltage protection is disabled.	B
TMR	7	8 (GND)	The device is set to latch-off mode if an overcurrent fault is detected.	B
GND	8	9 (IMON)	The IMON output is not reported.	B
IMON	9	9 (ITMPO)	The IMON and ITMPO outputs are not reported.	B
ITMPO	10	11 (IOC)	The device can detect a false I2t based overcurrent, and the ITMPO output is not reported.	B
IOC	11	12 (I2t)	The device can detect a false I2t based overcurrent.	B
G	13	14 (BST)	The BST capacitor can discharge through the pulldown on the G pin. The bypass path (G) is not able to turn ON if the $V_{GS(th)}$ of the bypass FET is $> 2V$.	B
BST	14	15 (SRC)	The gate drive supply is shorted, and the external FETs do not turn ON.	B
SRC	15	16 (GATE)	There is a short of the pulldown switch (between GATE and SRC) of the internal gate driver. The external FET remains OFF.	B
CS1-	19	20 (CS1+)	Bypasses the external current sense resistor. The IMON OCP features becomes disabled.	B
CS1+	20	21 (ISCP)	IMON information is not available. A false SCP can trigger.	B
ISCP	21	22 (VS)	The short-circuit protection gets set to a minimum setting of 2mV.	C
VS	22	23 (CS2-)	The load wake-up functionality is unavailable.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
CS2-	23	24 (DRN)	The load wake-up functionality is unavailable.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	1	The device remains enabled. If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
INP_G	2	The bypass path (G) remains ON in active mode. If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
INP	3	The Mmain path (GATE) remains ON in active mode. If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
I_DIR	4	The functionality of I_DIR is not available. If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
OV	5	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
FLT	6	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
TMR	7	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
GND	8	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
IMON	9	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
ITMPO	10	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
IOC	11	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
I2t	12	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
G	13	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
BST	14	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on the ESD circuit.	A
SRC	15	The output is stuck on to supply.	B
GATE	16	In the application, the external sense resistor gets bypassed, and the IMON overcurrent and short circuit protection does not work.	A
TMP	18	If pin voltage exceeds the pin datasheet range, the voltage can cause device damage due to voltage breakdown on ESD circuit.	A
CS1-	19	In the application, the external sense resistor is bypassed, and the IMON I2t based overcurrent and short circuit protection does not work.	B
CS1+	20	The IMON and I2t outputs are saturated. The external FET (GATE) turns OFF due to a false overcurrent event.	B
ISCP	21	The short-circuit protection gets set to a minimum setting of 2mV.	C
VS	22	The device operates normally.	D
CS2-	23	The load wake-up functionality is disabled.	B
DRN	24	The device operates normally.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

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