Functional Safety Information

CSD967201
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the CSD967201 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

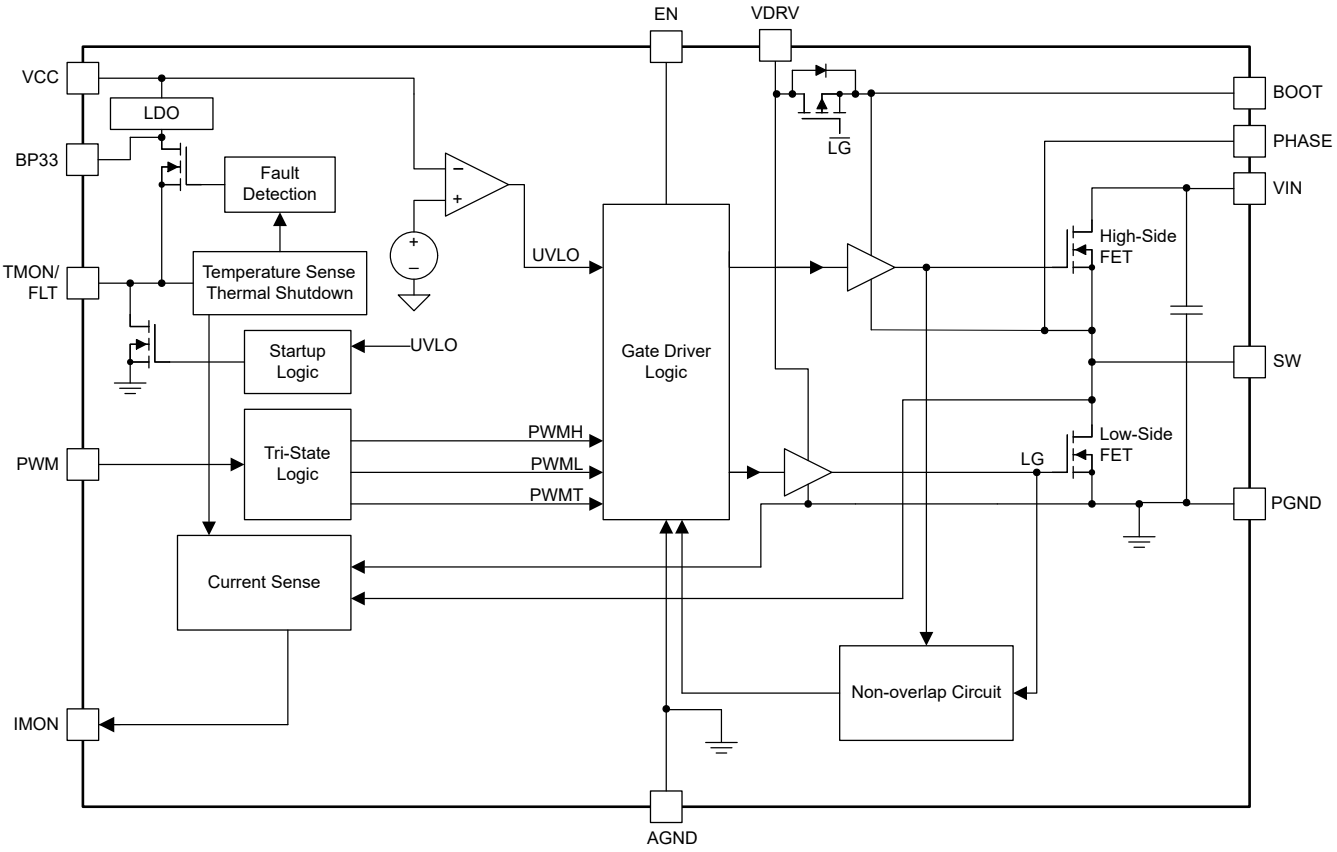

Figure 1-1. Functional Block Diagram

The CSD967201 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the CSD967201 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)		
Power dissipation	4W	2.7W	1.56W
Total component FIT rate	37	27	20
Die FIT rate	19	10	5
Package FIT rate	18	17	15

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Automotive control from table 11 or figure 16
- Power dissipation: See Table 2-1
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the CSD967201 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Power FET damage	48
SW output not in specification – voltage or timing	27
SW power HS or LS FET stuck on	17
IMON output not in specification	5
EN fails or false enable	3

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the CSD967201. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (VIN and VDRV, or VCC) (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the CSD967201 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the CSD967201 data sheet.

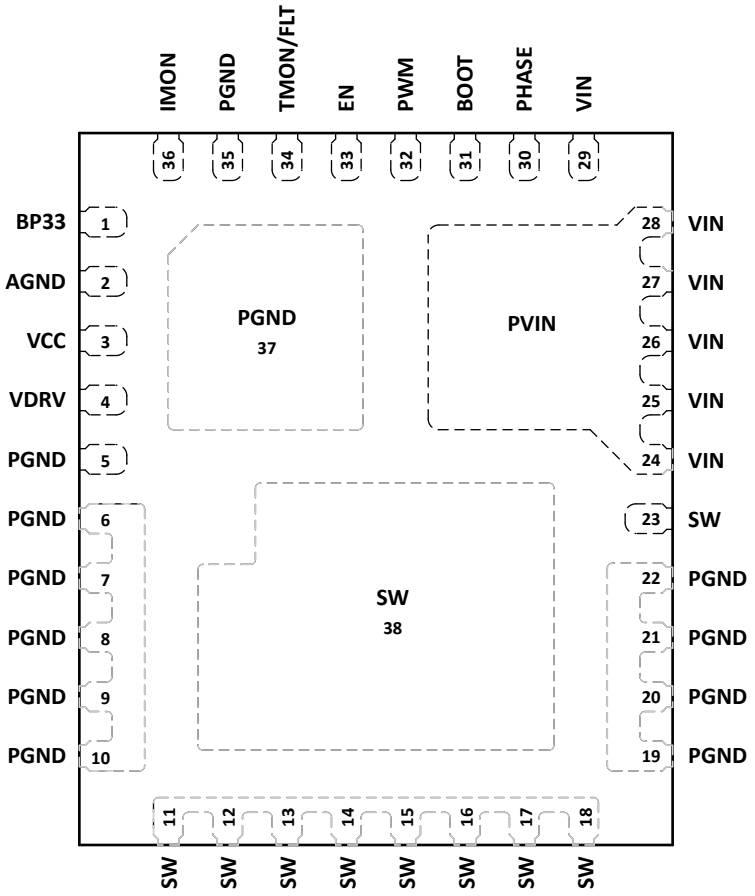

Figure 4-1. Pin Diagram (Top View)

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The VIN and VDRV supplies are within the recommended operating conditions.
- The external components on the pins are within the recommended passive component tolerance.
- The board conditions are within the recommended board level parasitic tolerance.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin No.	Pin Name	Description of Potential Failure Effects	Failure Effect Class
1	BP33	The device does not allow PWM switching and remains in tri-state mode.	B
2	AGND	The device continues to operate, but the AGND pin potentially experiences more disturbance to the transient ground. The PWM and interface parametrical are potentially skewed.	C
3	VCC	The device remains in a POR state. The device does not power on and remains in reset.	B
4	VDRV	The device remains in a POR state. The device does not power on and remains in reset.	B
5-10	PGND	The device operates as normal with full functionality.	D
19-22			
35			
37			
11-18	SW	The device is not functional and the power stage is not able to control VOUT. The peak current limit is used to limit the current of the high-side FET. The SW pin to ground causes the system regulation to drop to 0V. If there is a hard 0Ω short, there is potential damage to the internal high-side FET.	A
23			
38			
24-29	VIN	The device does not allow the power stage or IMON to function, and the device remains in a non-switching mode.	B
30	PHASE	The device is not functional and the power stage is not able to control VOUT. The peak current limit is used to limit the current of the high-side FET. The SW pin to ground causes the system regulation to drop to 0V. If there is a hard 0Ω short, there is potential damage to the internal high-side FET.	A
31	BOOT	The boot cap cannot charge, and the device does not have a floating supply for the boot domain. The boot UV detection does not allow the high-side FET to turn on, potentially causing a loss of regulation in the system.	B
32	PWM	There is a loss of functionality, with the low-side FET staying on after start-up.	B
33	EN	The device does not allow for PWM switching.	A
34	TMON/FLT	There is excessive current on the VDRV pin, with no TMON signal for all power stages in the system.	B
36	IMON	The controller sources large current from CSBIAS across the internal or external 1kΩ resistor in the system. Faults potentially do not trigger correctly.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin No.	Pin Name	Description of Potential Failure Effects	Failure Effect Class
1	BP33	If no cap is connected, the LDO is unstable. The PWM is potentially falsely detected, and TMON potentially experiences small oscillations.	C
2	AGND	The device does not interpret the PWM signal correctly and potentially does not turn on.	C
3	VCC	The device remains in a POR state. The device does not power on and remains in reset.	B
4	VDRV	The device remains in a POR state. The device does not power on and remains in reset.	B
5-10	PGND	GND is still present due to multiple PGND pins. The full functionality of the device is maintained.	D
19-22			
35			
37			
11-18	SW	The device is not functional and output regulation cannot be controlled by the power stage.	B
23			
38			
24-29	VIN	The device does not allow the power stage or IMON to function, and the device remains in a non-switching mode.	B
30	PHASE	The device is not functional, and output regulation cannot be controlled by the power stage.	B
31	BOOT	The boot cap cannot charge, and the device does not have a floating supply for the boot domain. The boot UV detection does not allow the high-side FET to turn on, potentially causing a loss of regulation in the system.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin No.	Pin Name	Description of Potential Failure Effects	Failure Effect Class
32	PWM	The device detects this pin as a PWM tri-state input and both the low-side and high-side FETs remain off.	B
33	EN	The device pulls down internally and does not allow the PWM input to turn the power stage on or off.	B
34	TMON/FLT	The TMON output does not report for the power stage.	B
36	IMON	The controller sources large current from CSBIAS across the internal or external 1kΩ resistor in the system. Faults potentially do not trigger correctly.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin No.	Pin Name	Shorted to	Description of Potential Failure Effects	Failure Effect Class
1	BP33	IMON	Depending on the strength of the IMON drive, the BP33 pin is likely to dominate. The BP33 pin potentially rises to VCC.	B
		AGND	The device does not allow PWM switching and remains in tri-state mode.	B
2	AGND	BP33	The device does not allow PWM switching and remains in tri-state mode.	B
		VCC	The device remains in a POR state. The device does not power on and remains in reset.	B
3	VCC	AGND	The device remains in a POR state. The device does not power on and remains in reset.	B
		VDRV	The device functions. There is no filter between the VCC and VDRV pins. The system potentially has more jitter.	C
4	VDRV	VCC	The device functions. There is no filter between the VCC and VDRV pins. The system potentially has more jitter.	C
		PGND	The device remains in a POR state. The device does not power on and remains in reset.	B
5-10	PGND	VDRV	The device remains in a POR state. The device does not power on and remains in reset.	B
19-22		IMON	The controller sources large current from CSBIAS across the internal or external 1kΩ resistor in the system. Faults potentially do not trigger correctly.	A
35		TMON/FLT	There is excessive current on the VDRV pin, with no TMON signal for all power stages in the system.	B
37		VIN	The device does not allow the power stage or IMON to function, and the device remains in a non-switching mode.	B
		SW	The device is not functional and the power stage is not able to control VOUT. The peak current limit is used to limit the current of the high-side FET. The SW pin to ground causes the system regulation to drop to 0V. If there is a hard 0Ω short, there is potential damage to the internal high-side FET.	A
11-18	SW	PGND	The device is not functional and the power stage is not able to control VOUT. The peak current limit is used to limit the current of the high-side FET. The SW pin to ground causes the system regulation to drop to 0V. If there is a hard 0Ω short, there is potential damage to the internal high-side FET.	A
23				
38		VIN	This is equivalent to a high-side FET short. The high-side short protection turns on the low-side FET and potentially damages the FET.	A
24-29	VIN	SW	This is equivalent to a high-side FET short. The high-side short protection turns on the low-side FET and potentially damages the FET.	A
		PHASE	This is equivalent to a high-side FET short. The high-side short protection turns on the low-side FET and potentially damages the FET.	A
30	PHASE	VIN	This is equivalent to a high-side FET short. The high-side short protection turns on the low-side FET and potentially damages the FET.	A
		BOOT	The boot cap does not have a floating supply for the boot domain. The boot UV detection does not allow the high-side FET to turn on, potentially causing a loss of regulation in the system.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin No.	Pin Name	Shorted to	Description of Potential Failure Effects	Failure Effect Class
31	BOOT	PHASE	The boot cap does not have a floating supply for the boot domain. The boot UV detection does not allow the high-side FET to turn on, potentially causing a loss of regulation in the system.	B
		PWM	The boot cap does not have a floating supply for the boot domain. The boot UV detection does not allow the high-side FET to turn on, potentially causing a loss of regulation in the system. If the BOOT pin is higher than the VCC supply, damage can occur to the PWM input.	B
32	PWM	BOOT	The boot cap does not have a floating supply for the boot domain. The boot UV detection does not allow the high-side FET to turn on, potentially causing a loss of regulation in the system. If the BOOT pin is higher than the VCC supply, damage can occur to the PWM input.	B
		EN	If EN = VCC, the high-side FET remains on.	B
33	EN	PWM	If EN = VCC, the high-side FET remains on.	B
		TMON/FLT	There is a loss of TMON and FAULT detection. TMON does not function.	B
34	TMON/FLT	EN	There is a loss of TMON and FAULT detection. TMON does not function.	B
		VIN	There is damage to the internal, 5V-rated circuitry. If VIN > 8V, there is potential damage to the device.	A
36	IMON	VIN	There is damage to the internal, 5V-rated circuitry. If VIN > 8V, there is potential damage to the device.	A
		BP33	The controller sinks large current from the BP33 pin across the internal or external 1kΩ resistor in the system. Faults potentially do not trigger correctly.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin No.	Pin Name	Description of Potential Failure Effects	Failure Effect Class
1	BP33	There is damage to the internal, 5V-rated circuitry. If VIN > 8V, there is potential damage to the device.	A
2	AGND	The power supply is missing. The device does not power up, with a large uncontrolled VIN input current, which potentially causes damage to the device.	A
3	VCC	There is damage to the internal, 5V-rated circuitry. If VIN > 8V, there is potential damage to the device.	A
4	VDRV	There is damage to the internal, 5V-rated circuitry. If VIN > 8V, there is potential damage to the device.	A
5-10	PGND	The power supply is missing. The device does not power up, with a large uncontrolled VIN input current, which potentially causes damage to the device.	A
19-22			
35			
37			
11-18	SW	There is potential damage to the low-side FET. The high-side short detection forces the low-side FET to turn on if EN = 1.	A
23			
38			
30	PHASE	There is potential damage to the low-side FET. The high-side short detection forces the low-side FET to turn on if EN = 1.	A
31	BOOT	There is potential damage to the low-side FET. The high-side short detection forces the low-side FET to turn on if EN = 1.	A
32	PWM	There is damage to the internal, 5V-rated circuitry. If VIN > 8V, there is potential damage to the device.	A
33	EN	There is damage to the internal, 5V-rated circuitry. If VIN > 8V, there is potential damage to the device.	A
34	TMON/FLT	There is damage to the internal, 5V-rated circuitry. If VIN > 8V, there is potential damage to the device.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN (continued)

Pin No.	Pin Name	Description of Potential Failure Effects	Failure Effect Class
36	IMON	There is damage to the internal, 5V-rated circuitry. If VIN > 8V, there is potential damage to the device. Faults potentially do not trigger correctly.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 14, 2025 to December 18, 2025 (from Revision * (November 2025) to Revision A (December 2025)) **Page**

- Updated the failure effect description and class for all instances of pin 36 (IMON) in all tables..... 5

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