Functional Safety Information

INA187-Q1 and INA299-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for INA187-Q1 and INA299-Q1 (SC70-6 package) to aid in a functional safety system design. This document applies to the following devices:

- INA187-Q1
- INA299-Q1

Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

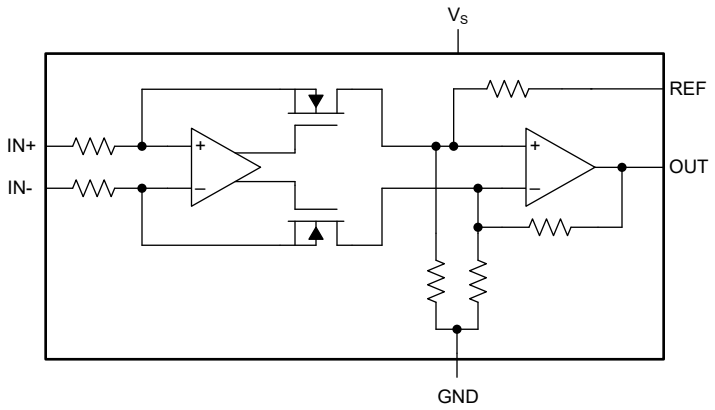

Figure 1-1. Functional Block Diagram

INA187-Q1 and INA299-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for INA187-Q1 and INA299-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	5
Die FIT rate	3
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 14.4mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	CMOS Op amp, comparators, voltage monitors	8 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA187-Q1 and INA299-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	10
VOUT stuck (Hi or Low)	45
VOUT functional, not in specification	45

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the INA187-Q1 and INA299-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to Vs (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the INA187-Q1 and INA299-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA187-Q1 and INA299-Q1 data sheets.

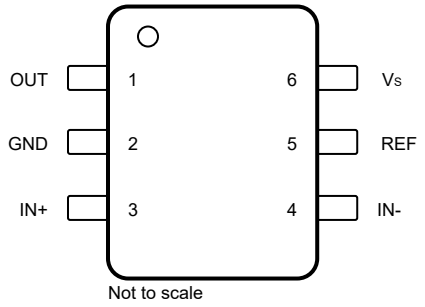

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_s = 5V
- V_{IN+} = 48V
- V_{REF} = V_{s+} / 2

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Output is pulled down to GND and output current is short-circuit limited. When left in this configuration for a long time, under high supplies, self-heating can cause the die junction temperature to exceed 150°C.	B
GND	2	Normal operation.	D
IN+	3	In a high-side configuration, a short from the bus supply to GND occurs.	B
IN-	4	In a high-side configuration, a short from the bus supply to GND occurs (through RSHUNT). High current flows from the bus supply to GND. The shunt can be damaged. In a low-side configuration, normal operation.	B for high-side D for low-side
REF	5	Normal operation if the REF pin is at GND potential by design; otherwise, the system measurement is incorrect.	D if REF = GND by design C otherwise
VS	6	Power supply shorted to GND.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Output can be left open. There is no effect on the device, but the output is not measured.	C
GND	2	No power to the device. The device can be biased through inputs. Output is no longer referenced to GND.	B
IN+	3	The shunt resistor is not connected to the amplifier. The IN+ pin can float to an unknown value. Output goes to an unknown value, not to exceed Vs or GND.	B
IN-	4	The shunt resistor is not connected to the amplifier. The IN- pin can float to an unknown value. Output goes to an unknown value, not to exceed Vs or GND.	B
REF	5	Output common-mode voltage is not defined. Output does not maintain a linear relationship with differential input voltage.	C
VS	6	No power to device. Device can be biased through inputs. Output is incorrect and close to GND.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	2 - GND	Output is pulled down to GND and output current is short-circuit limited. When left in this configuration for a long time, under high supplies, self-heating can cause the die junction temperature to exceed 150°C.	B
GND	2	3 - IN+	Power supply is shorted to GND.	B
IN+	3	4 - IN-	Inputs are shorted together, so no sense voltage is applied. Output stays close to REF potential.	B
IN-	4	5 - REF	In a high-side configuration, REF is shorted to the bus supply (through Rshunt). High current flows from the bus supply to GND, shunt can be damaged. In a low-side configuration, normal operation (if REF is at GND potential by design)	B for high-side C for low-side D if REF = GND by design
REF	5	6 - VS	Normal operation if the REF pin is at Vs potential by design; otherwise, the system measurement is incorrect.	D if REF=Vs by design C otherwise
VS	6	1 - OUT	Output is pulled to Vs and the output current is short-circuit limited. When left in this configuration for a long time, under high supplies, self-heating can cause the die junction temperature to exceed 150°C.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Vs

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Output is pulled to Vs and the output current is short-circuit limited. When left in this configuration for a long time, under high supplies, self-heating can cause the die junction temperature to exceed 150°C.	B
GND	2	Power supply is shorted to GND.	B
IN+	3	In a high-side configuration, the device power supply is shorted to the bus supply (through RSHUNT). In a low-side configuration, the device power supply is shorted to GND.	B
IN-	4	In a high-side configuration, the device power supply is shorted to the bus supply. In a low-side configuration, the device power supply is shorted to GND (through RSHUNT).	B
REF	5	Normal operation if the REF pin is at Vs potential by design; otherwise, the system measurement is incorrect.	D if REF=Vs by design C otherwise
VS	6	Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2025	*	Initial Release

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