

Functional Safety Information

**UCC27289**

**Functional Safety FIT Rate, FMD and Pin FMA**

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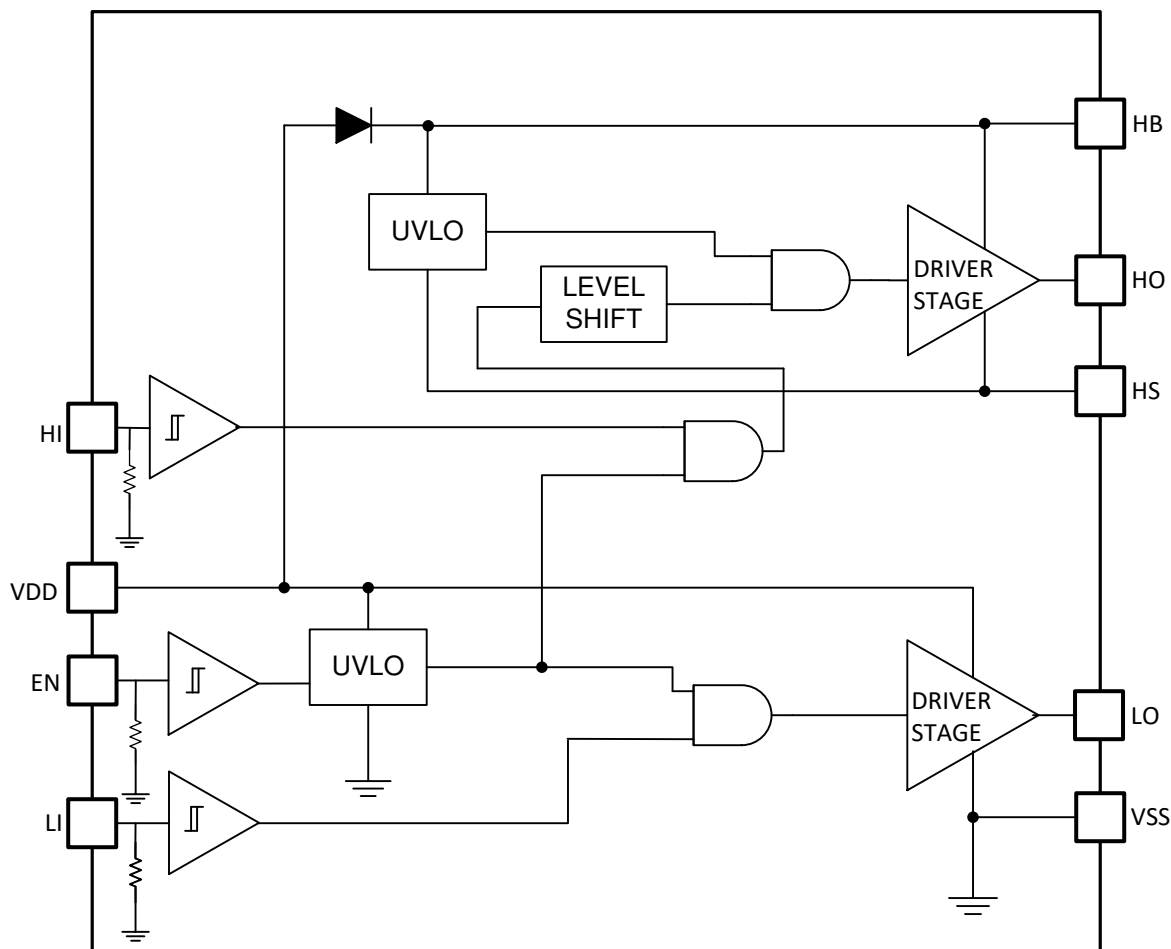
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## 1 Overview

This document contains information for the UCC27289 (SOIC and VSON packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



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**Figure 1-1. Functional Block Diagram**

The UCC27289 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

### 2.1 SOIC Package

This section provides functional safety failure in time (FIT) rates for the SOIC package of UCC27289 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | Power Dissipation (mW) | FIT (Failures Per 10 <sup>9</sup> Hours) |
|------------------------------|------------------------|------------------------------------------|
| Total component FIT rate     | 10                     | 13                                       |
|                              | 100                    | 14                                       |
|                              | 500                    | 28                                       |
| Die FIT rate                 | 10                     | 2                                        |
|                              | 100                    | 3                                        |
|                              | 500                    | 14                                       |
| Package FIT rate             | 10                     | 11                                       |
|                              | 100                    | 11                                       |
|                              | 500                    | 14                                       |

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 10mW, 100mW, and 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor ( $\lambda_3$ ): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category                                   | Reference FIT Rate | Reference Virtual T <sub>J</sub> |
|-------|--------------------------------------------|--------------------|----------------------------------|
| 5     | CMOS, BICMOS,<br>Digital, analog, or mixed | 20 FIT             | 55°C                             |

The reference FIT rate and reference virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

## 2.2 VSON Package

This section provides functional safety failure in time (FIT) rates for the VSON package of UCC27289 based on two different industry-wide used reliability standards:

- [Table 2-3](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-4](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | Power Dissipation (mW) | FIT (Failures Per 10 <sup>9</sup> Hours) |
|------------------------------|------------------------|------------------------------------------|
| Total component FIT rate     | 10                     | 10                                       |
|                              | 100                    | 12                                       |
|                              | 500                    | 25                                       |
| Die FIT rate                 | 10                     | 2                                        |
|                              | 100                    | 3                                        |
|                              | 500                    | 14                                       |
| Package FIT rate             | 10                     | 8                                        |
|                              | 100                    | 9                                        |
|                              | 500                    | 11                                       |

The failure rate and mission profile information in [Table 2-3](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 10mW, 100mW, and 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category                                   | Reference FIT Rate | Reference Virtual T <sub>J</sub> |
|-------|--------------------------------------------|--------------------|----------------------------------|
| 5     | CMOS, BICMOS,<br>Digital, analog, or mixed | 20 FIT             | 55°C                             |

The reference FIT rate and reference virtual T<sub>J</sub> (junction temperature) in [Table 2-4](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

## 3 Failure Mode Distribution (FMD)

### 3.1 SOIC Package

The failure mode distribution estimation for UCC27289 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes                 | Failure Mode Distribution (%) |
|-----------------------------------|-------------------------------|
|                                   | UCC27289                      |
| HO stuck high                     | 16.5                          |
| HO stuck low                      | 16.5                          |
| HO voltage out of specified range | 16.5                          |
| LO stuck high                     | 16.5                          |
| LO stuck low                      | 16.5                          |
| LO voltage out of specified range | 16.5                          |
| UVLO not functional               | 1                             |

### 3.2 VSON Package

The failure mode distribution estimation for UCC27289 in [Table 3-2](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-2. Die Failure Modes and Distribution**

| Die Failure Modes                 | Failure Mode Distribution (%) |
|-----------------------------------|-------------------------------|
| HO stuck high                     | 16.5                          |
| HO stuck low                      | 16.5                          |
| HO voltage out of specified range | 16.5                          |
| LO stuck high                     | 16.5                          |
| LO stuck low                      | 16.5                          |
| LO voltage out of specified range | 16.5                          |
| UVLO not functional               | 1                             |

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC27289 (SOIC and VSON packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#) and [Table 4-6](#))
- Pin open-circuited (see [Table 4-3](#) and [Table 4-7](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#) and [Table 4-8](#))
- Pin short-circuited to supply (see [Table 4-5](#) and [Table 4-9](#))

[Table 4-2](#) through [Table 4-9](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects                                              |
|-------|--------------------------------------------------------------|
| A     | Potential device damage that affects functionality.          |
| B     | No device damage, but loss of functionality.                 |
| C     | No device damage, but performance degradation.               |
| D     | No device damage, no impact to functionality or performance. |

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- SOIC: Pins 1-4, short to VDD is considered
- SOIC: Pins 5-6, short to 5V, such as, MCU or controller I/O supply is considered
- SOIC: VSS is assumed to be a ground plane
- VSON: Pins 1-5 and 10, short to VDD is considered
- VSON: Pins 6-8, short to 5V, such as, MCU or controller I/O supply is considered
- VSON: VSS is assumed to be a ground plane

## 4.1 SOIC Package

Figure 4-1 shows the UCC27289 pin diagram for the SOIC package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC27289 data sheet.

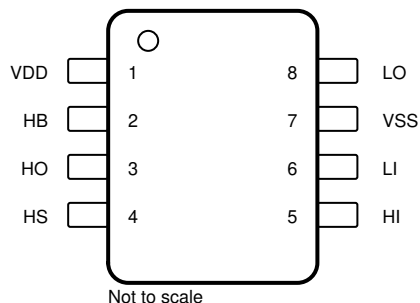


**Figure 4-1. Pin Diagram (SOIC Package)**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effects           | Failure Effect Class |
|----------|---------|----------------------------------------------------|----------------------|
| VDD      | 1       | LO remains low. HO remains low.                    | B                    |
| HB       | 2       | Device can be damaged with unknown LO or HO state. | A                    |
| HO       | 3       | Device can be damaged with unknown LO or HO state. | A                    |
| HS       | 4       | Device can be damaged with unknown LO or HO state. | A                    |
| HI       | 5       | HO is in a low state.                              | B                    |
| LI       | 6       | LO is in a low state.                              | B                    |
| VSS      | 7       | N/A                                                | D                    |
| LO       | 8       | Device can be damaged with unknown LO or HO state. | A                    |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effects    | Failure Effect Class |
|----------|---------|---------------------------------------------|----------------------|
| VDD      | 1       | LO remains low. HO remains low.             | B                    |
| HB       | 2       | HO is pulled to HS potential.               | B                    |
| HO       | 3       | HO terminal is not connected to the system. | D                    |
| HS       | 4       | HO is pulled to HB potential.               | B                    |
| HI       | 5       | HO is in a low state.                       | B                    |
| LI       | 6       | LO is in a low state.                       | B                    |
| VSS      | 7       | HO is in a low state. LO is pulled to VDD.  | B                    |
| LO       | 8       | LO terminal is not connected to the system. | D                    |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to (Pin Number +1) | Description of Potential Failure Effects                           | Failure Effect Class |
|----------|---------|----------------------------|--------------------------------------------------------------------|----------------------|
| VDD      | 1       | HB                         | Device can be damaged. LO or HO can be damaged with unknown state. | A                    |
| HB       | 2       | HO                         | Device can be damaged with unknown HO state.                       | A                    |
| HO       | 3       | HS                         | Device can be damaged with unknown LO or HO state.                 | A                    |
| HS       | 4       | N/A                        | N/A                                                                | N/A                  |
| HI       | 5       | LI                         | HO or LO is in a low state.                                        | B                    |
| LI       | 6       | VSS                        | LO is in a low state.                                              | B                    |
| VSS      | 7       | LO                         | Device can be damaged with unknown LO or HO state.                 | A                    |
| LO       | 8       | N/A                        | N/A                                                                | N/A                  |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply**

| Pin Name | Pin No. | Description of Potential Failure Effects                                                                | Failure Effect Class |
|----------|---------|---------------------------------------------------------------------------------------------------------|----------------------|
| VDD      | 1       | No effect.                                                                                              | D                    |
| HB       | 2       | Device can be damaged with unknown LO or HO state.                                                      | A                    |
| HO       | 3       | Device can be damaged with unknown LO or HO state.                                                      | A                    |
| HS       | 4       | Device can be damaged with unknown LO or HO state.                                                      | A                    |
| HI       | 5       | Short to 5V (for example, power supply of the microcontroller). LO or HO follows the HI,LI truth table. | B                    |
| LI       | 6       | Short to 5V (for example, power supply of the microcontroller). LO or HO follows the HI,LI truth table. | B                    |
| VSS      | 7       | HO is in a low state. LO is pulled to VDD.                                                              | B                    |
| LO       | 8       | Device can be damaged with unknown LO or HO state.                                                      | A                    |

## 4.2 VSON Package

Figure 4-2 shows the UCC27289 pin diagram for the VSON package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC27289 data sheet.

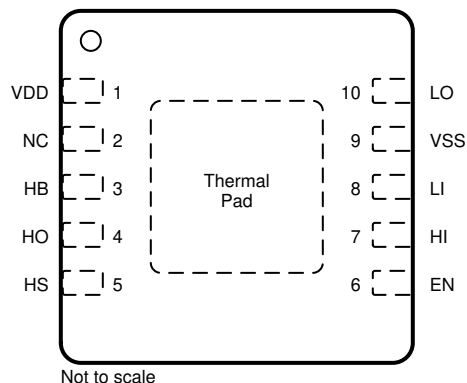


**Figure 4-2. Pin Diagram (VSON Package)**

**Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effects           | Failure Effect Class |
|----------|---------|----------------------------------------------------|----------------------|
| VDD      | 1       | LO remains low. HO remains low.                    | B                    |
| NC       | 2       | No effect.                                         | D                    |
| HB       | 3       | Device can be damaged with unknown LO or HO state. | A                    |
| HO       | 4       | Device can be damaged with unknown LO or HO state. | A                    |
| HS       | 5       | Device can be damaged with unknown LO or HO state. | A                    |
| EN       | 6       | LO remains low. HO remains low.                    | B                    |
| HI       | 7       | HO is in a low state.                              | B                    |
| LI       | 8       | LO is in a low state.                              | B                    |
| VSS      | 9       | No effect.                                         | D                    |
| LO       | 10      | Device can be damaged with unknown LO or HO state. | A                    |

**Table 4-7. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effects    | Failure Effect Class |
|----------|---------|---------------------------------------------|----------------------|
| VDD      | 1       | LO remains low. HO remains low.             | B                    |
| NC       | 2       | No effect.                                  | D                    |
| HB       | 3       | HO is pulled to HS potential.               | B                    |
| HO       | 4       | HO terminal is not connected to the system. | D                    |
| HS       | 5       | HO is pulled to HB potential.               | B                    |
| EN       | 6       | LO remains low. HO remains low.             | B                    |
| HI       | 7       | HO is in a low state.                       | B                    |
| LI       | 8       | LO is in a low state.                       | B                    |
| VSS      | 9       | HO is in a low state LO is pulled to VDD.   | B                    |
| LO       | 10      | LO terminal is not connected to the system. | D                    |

**Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to (Pin Number +1) | Description of Potential Failure Effects                                                           | Failure Effect Class |
|----------|---------|----------------------------|----------------------------------------------------------------------------------------------------|----------------------|
| VDD      | 1       | NC                         | No effect.                                                                                         | D                    |
| NC       | 2       | HB                         | No effect.                                                                                         | D                    |
| HB       | 3       | HO                         | Device can be damaged with unknown HO state.                                                       | A                    |
| HO       | 4       | HS                         | Device can be damaged with unknown LO or HO state.                                                 | A                    |
| HS       | 5       | N/A                        | N/A                                                                                                | N/A                  |
| EN       | 6       | HI                         | LO or HO follows the logic truth table, per the data sheet, with EN in the same logic state as HI. | B                    |
| HI       | 7       | LI                         | HO or LO is in a low state.                                                                        | B                    |
| LI       | 8       | VSS                        | LO is in a low state.                                                                              | B                    |
| VSS      | 9       | LO                         | Device can be damaged with unknown LO or HO state.                                                 | A                    |
| LO       | 10      | N/A                        | N/A                                                                                                | N/A                  |

**Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply**

| Pin Name | Pin No. | Description of Potential Failure Effects                                                                                                                  | Failure Effect Class |
|----------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| VDD      | 1       | No effect.                                                                                                                                                | D                    |
| NC       | 2       | No effect.                                                                                                                                                | D                    |
| HB       | 3       | Device can be damaged with unknown LO or HO state.                                                                                                        | A                    |
| HO       | 4       | Device can be damaged with unknown LO or HO state.                                                                                                        | A                    |
| HS       | 5       | Device can be damaged with unknown LO or HO state.                                                                                                        | A                    |
| EN       | 6       | Short to 5V (for example, power supply of the microcontroller). LO or HO follows the logic truth table, per data sheet, with EN is stuck in a high state. | B                    |
| HI       | 7       | Short to 5V (for example, power supply of the microcontroller). LO or HO follows the HI,LI truth table.                                                   | B                    |
| LI       | 8       | Short to 5V (for example, power supply of the microcontroller). LO or HO follows the HI,LI truth table.                                                   | B                    |
| VSS      | 9       | HO is in a low state, LO is pulled to VDD.                                                                                                                | B                    |
| LO       | 10      | Device can be damaged with unknown LO or HO state.                                                                                                        | A                    |

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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**Changes from June 19, 2025 to September 26, 2025 (from Revision \* (June 2025) to Revision A  
(September 2025))**

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- Updated failure mode distribution.....5
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